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Simulation of Qpsk Modulator to Generate Real and Imaginary Channel

Tushar V. Kafare[*1], Prof .Col.Vijay Joshi[*2],
**1(E &TC department, GHRCEM Pune, India.)*
**2(Head of E&TC Department, GHRCEM Pune, India)*

Abstract
In this paper we present a theoretical background of the digital communication systems and the QPSK modulation. The main purpose is to design the QPSK system on FPGA. The simulation of a QPSK Modulator to generate the real and imaginary channel is done using Xilinx ISE9.2 .the modulator algorithm has been implemented using the VHDL language on Xilinx ISE 9.2.The modulated signal obtained in the form of I and Q channel. Simulation is checked by applying different data stream at input and observing the real and imaginary part.
Keywords: Modulation, Simulation, FPGA, QPSK.

I. INTRODUCTION

Digital modulation is the process by which digital symbols are transmitted into waveforms that are compatible with the characteristics of the channel. The modulation process converts the signal in order to be compatible with available transmission facilities. At the receiver end, demodulation must be accomplished by recognizing the signals.The DQPSK (Differential Quadrature Phase Shift Keying) is one of the basic binary modulation technique .It has as a result only two phases of the carrier, at the same frequency ,but separated by 90º . The QPSK uses four points on the constellation diagram, equi spaced around circle .With four phases, QPSK can encode two bits per symbol, given with gray coding to minimize the bit error rate (BER).Sometimes misperceived as twice the BPSK.

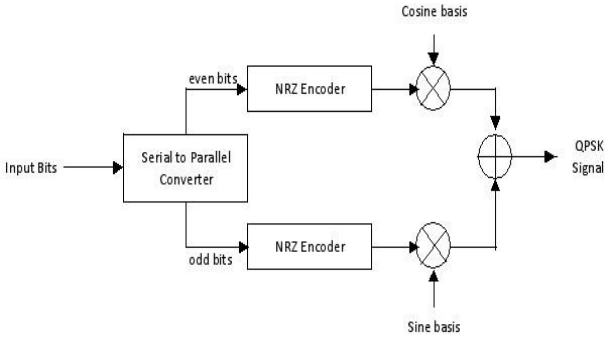

Fig 1.1 QPSK generation

The QPSK can be used either to double the data rate compared with BPSK system while maintaining the same bandwidth of the signal. To maintain the data rate of BPSK but having the bandwidth needed in this latter case the BER of BPSK is same as that of BER of QPSK. The implementation of QPSK is more general than that of BPSK and also indicates the implementation of higher-order PSK. Writing the symbols in the constellation diagram in terms of the sine and cosine waves used to transmit them. The implementation of QPSK involves changing the phase of the transmitted waveform. QPSK is one of the most popular digital modulation techniques used for Satellite communication and sending data over cable networks. Its popularity comes from both its easy implementation and pliability to noise. Each finite phase change representing unique digital data. A phase modulated waveform can be generated by using the digital data to change the phase of a signal while its frequency and amplitude stay constant.

The paper is organized into 4 sections .Introduction which represents section 1 describes basics of the QPSK Modulation. In section 2, I offer information about the software tools used and simulation techniques of QPSK Modulator in Xilinx a section 3 is dedicated to the result. The final section 4 Presents conclusion and future work.

II. QPSK IN XILINX ISE SIMULATOR

Here, I have written VHDL code for the QPSK generation using Xilinx Simulator. The real channel generated by passing all incoming even part to it. And imaginary part is generated by passing all odd part to the channel .I am going to implement QPSK generation on the Spartan 3 kit by Xilinx the adder can be implement in the hardware of FPGA so that it can take less power to operate. Here sin and cos signals are generated by dividing the clock and provided the phase difference between both.

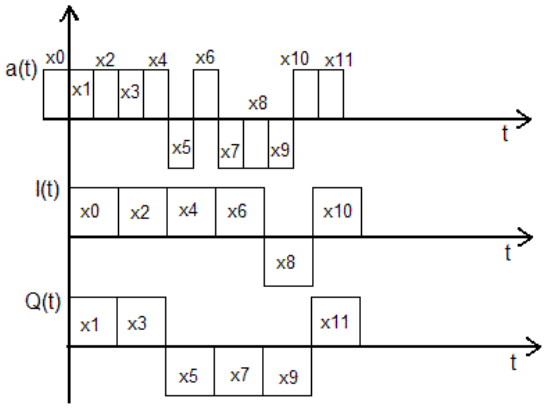

Fig.2.1: Generation of I &Q channel

The high frequency clock is reserved for Spartan 3 kit implementation and the divided clock is used to generate the I & Q signals. If we divide the clock in higher amount then the incoming signals can be separated fastly. Enable input is provided to start the separation of input bit and clock edge decides the speed . the next chapter describes the result of simulation of QPSK generation in Xilinx.

III. SIMULATION RESULT

Fig 3.1 specifies the RTL schematic of the design which gives the port map i.e. inputs the system and outputs from the system.

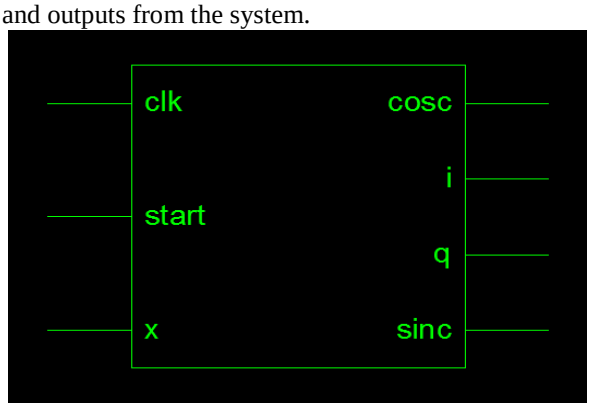

Fig 3.1 RTL schematic in simulator

Fig 4.2 gives the detailed description of the interconnection between input and output.

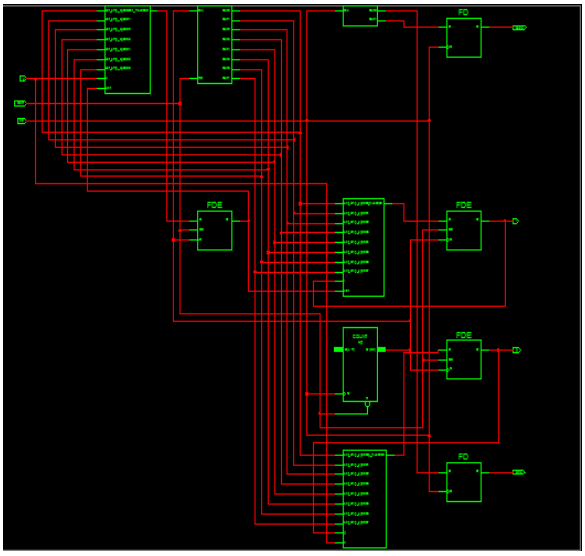

Fig 3.2 Interconnection Diagram

The following figure indicates the possible combination of inputs that can be given the the simulation of QPSK modulation. The clock signal must have high frequency so that the information send is maximum. The actual conversion start when enable signal is provided.

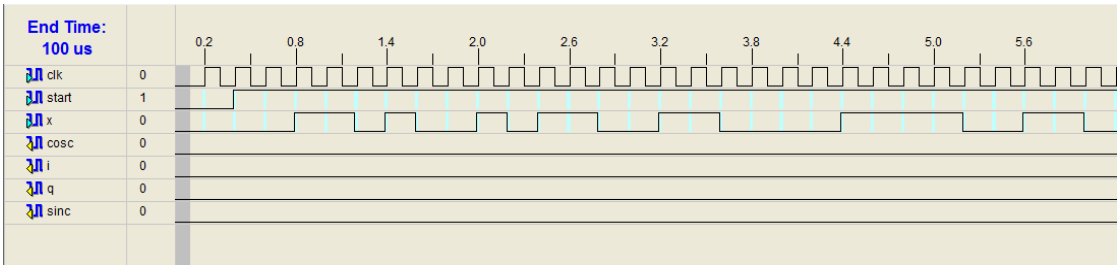

Fig 3.3 Test input

According the given input combination we can obtain the simulation result that is specified in next diagram all the signals i.e. divided clock, counter, input data stream sin and cos also I and Q channels.

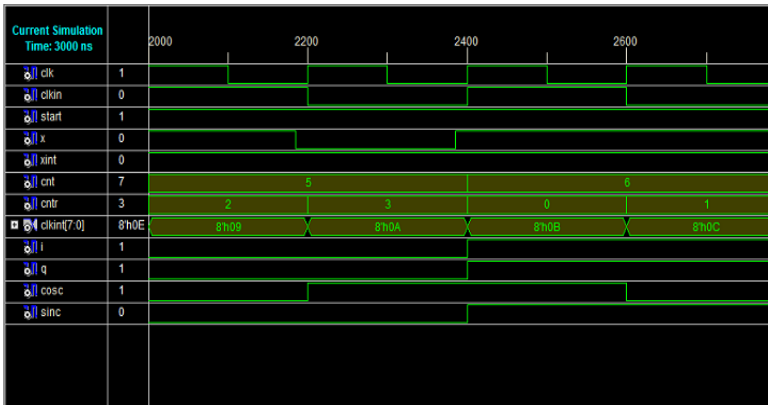

Fig 3.4 I&Q channel Generation by simulation

The device utilization is provided in the last diagram i.e. no of flip flops , IOBs ,LUTs and GLCKs .The device utilization gives the part of Spartan 3 kit and FPGA so that we can calculate the total power required. Device utilization summary gives the information related to the QPSK can be implementated in fast mode to enhance data rates also it will gives idea about system integrity.

If the used blocks of the fpga are less in number then power saving is done.

QWQW Project Status

Project File:	qwqw.ise	Current State:	Synthesized
Module Name:	modulation	• Errors:	No Errors
Target Device:	xc3s400-5pq208	• Warnings:	2 Warnings
Product Version:	ISE 9.2i	• Updated:	Tue 24 Sep 10:47:35 2013

QWQW Partition Summary

No partition information was found.

Device Utilization Summary (estimated values)

Logic Utilization	Used	Available	Utilization
Number of Slices	7	3584	0%
Number of Slice Flip Flops	11	7168	0%
Number of 4 input LUTs	8	7168	0%
Number of bonded IOBs	7	141	4%
Number of GCLKs	1	8	12%

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Wed 21. Aug 15:19:25 2013	0	2 Warnings	0

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Fig 3.5 device utilization summary

Field-programmable gate arrays are re programmable hardware chips for digital logic design. FPGAs are an array of logic gates that can be configured to construct arbitrary digital circuits. These circuits are specified using either circuit schematics or hardware description languages such as Verilog or VHDL. A logic design on an FPGA is also referred to as a soft intellectual property core (IP-core). Existing commercial libraries provide a wide range of predesigned cores, including those of complete CPUs. Such a More than one soft IP-core can be placed onto an FPGA chip.

IV. CONCLUSION AND FUTURE WORK

The purpose of this work is to develop a system to modulate the data using FPGA so that we can provide the security to the data as well as to enhance the data rate of the communication. The real and imaginary part of QPSK signal is generated by fpga and it can add externally to get QPSK signal.

The Main aim of project is to implement this communication system on the tool Spartan 3 provided by Xilinx so that we can minimize the power require. Also we can speed up the communication because FPGA implementation provides the high speed operation.

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