RESEARCH ARTICLE OPEN ACCESS

Compressor Based Area-Efficient Low-Power 8x8 Vedic Multiplier

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Abstract
Multipliers are the integral components in the design of many high performance FIR filters, image and digital signal processors. Multipliers being the most area and power consuming elements of a design, area-efficient low-power multiplier architectures are in demand. In this paper, multiplier based on ancient Vedic mathematics technique has been proposed which employs 4:3, 5:3, 6:3 and 7:3 compressors for addition of partial products. Combining the Vedic Sutra- Urdhwa Tiryakbhyam and efficient compressors, a robust area and power efficient multiplier architecture has been achieved. The designs were synthesized and analysed in Cadence RTL compiler in 180 nm technology. When compared with previous compressor based multiplier, the proposed design achieves 30.5% and 25.8% reduction in power and area respectively.
Keywords: Vedic multiplier**,** Urdhwa Tiryakbhyam Sutra, compressor, low-power

I. INTRODUCTION

Multipliers are the key components of all the digital signal processors (DSPs), FIR filters and image processors and the performance of these processors is largely determined by the kind of multipliers used. They are generally the most area consuming and hence power consuming units in the design. Therefore, optimizing the area and power of the multiplier is a major design issue..

Several multipliers have been proposed and designed over past few decades [1]. In these algorithms, the multiplication process requires several intermediate stages to get the final result due to which critical path gets lengthened. Also, these intermediate stages require additional hardware which leads to increase in area and power consumption.

To overcome these disadvantages, multipliers based on Vedic Mathematics technique have been proposed in [2] and [3] where all the partial products are obtained well in advance much before the actual operation of multiplication begins, which results in a high speed design.

A compressor based multiplier has also been in proposed in [4] which utilises 4:2 and 7:2 compressors to reduce the intermediate stages.

In this paper, novel multiplier architecture is proposed which can efficiently reduce the intermediate stages as compared to compressor based multiplier, by using high order compressors such as 4:3, 5:3, 6:3, 7:3 compressors [5]

Section II describes Urdhwa Tiryakbhyam Sutra for 8-bit multiplication. Section III explains the high order compressors used in this paper. Section IV describes the proposed multiplier. Section V and Section VI discusses the comparative results and conclusions.

II. VEDIC SUTRA - URDHWA TIRYAKBHYAM

The 16 Vedic Sutras apply to and cover almost every branch of Mathematics. They apply even to complex problems involving a large number of mathematical operations. Among these sutras, Urdhwa Tiryakbhyam Sutra is the most efficient for performing multiplication.

The use of this sutra can be extended to binary multiplication as well .This Sutra translates to "Vertical and crosswise". It utilizes only logical AND operation, half adders and full adders to perform multiplication where the partial products are generated prior to actual multiplication. This saves a considerable amount of processing time. Moreover it is a robust method of multiplication.

Consider two 8-bit numbers, a (a_8-a_1) and b (b_8-b_1) where 1 to 8 represents bits from the least significant bit to the most significant bit. The final product is represented by P (P_{16}-P_1). In Fig.1, the step by step method of multiplication of two 8-bit numbers using Urdhwa Tiryakbhyam Sutra is illustrated. The bits of the multiplier and multiplicand are represented by dots and the two way arrow represents the logical AND operation between the bits which gives the partial product terms.

In the conventional design of Urdhwa Tiryakbhyam sutra based multiplier, only full-adders and half-adders are used for addition of the partial products. But, the capability of full-adder is limited to addition of only 3 bits at a time.

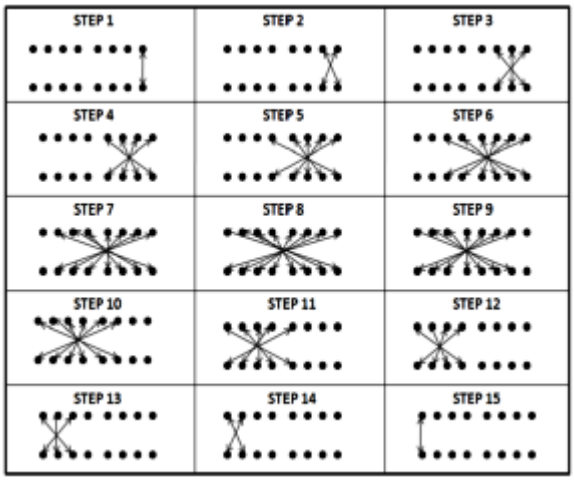

Fig.1. 8-bit binary multiplication using Urdhwa Tiryakbhyam Sutra

So, a large number of stages are required to get the final product. Higher order compressors discussed in next section can be employed to add more than 3 bits at a time (upto 7 bits) and hence can reduce the intermediate stages.

III. HIGHER-ORDER COMPRESSORS

Several 4-2 and 5-2 compressor architectures have been reported so far [5], [6]. The main drawback associated with these conventional compressors is that the result generated is not in proper binary form and one more half adder/ full adder is required to get the final results, thereby increasing the area and power dissipation. Moreover, due to uneven delay profiles of the outputs arriving from different input paths, a lot of glitches are generated.

To overcome these problems associated with the conventional compressors, higher order compressors proposed in [7] have been used in the design. These compressors have been designed as counter of '1's at the input bits. Full adder itself is a counter of 1's at its input as illustrated in Table I. Therefore, full adder acts as 3-2 compressor. The similar logic can be used to design the higher order compressor circuits.

Table I
Full adder as a counter

Number of 1's at the input	Output		Equivalent decimal value
	Carry	Sum	
Zero	0	0	0
One	0	1	1
Two	1	0	2
Three	1	1	3

The concept of the 4-3 compressor as counter is shown in Table II. Similarly 5-3, 6-3 and 7-3 compressors can be obtained.

Table II
4-3 compressor as a counter

Number of 1's at the input	Output			Equivalent decimal value
	C3	C2	C1	
Zero	0	0	0	0
One	0	0	1	1
Two	0	1	0	2
Three	0	1	1	3
Four	1	0	0	4

The block diagram of 4-3, 5-3, 6-3 and 7-3 compressors are shown in Fig. 2, 3, 4, and 5 respectively.

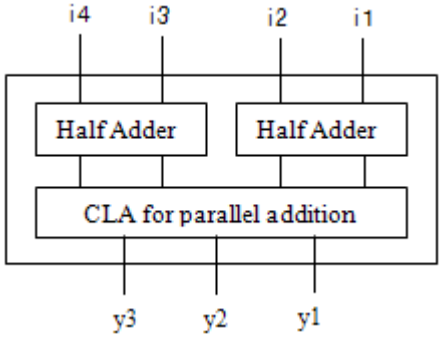

Fig.2. Block diagram of a 4-3 Compressor

The block diagrams of 4-3, 5-3 and 6-3 compressor contains three sub-units: two adder units and a Carry Look Ahead adder (CLA) unit for parallel addition of the outputs of the adder units. The 7-3 compressor is implemented using 4-3 compressor, a full adder and a CLA unit.

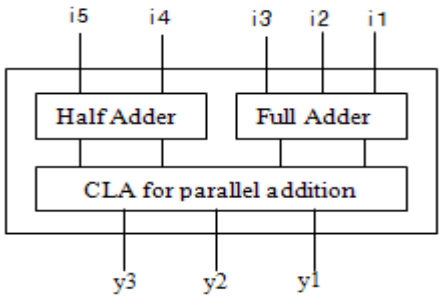

Fig.3. Block diagram of a 5-3 Compressor

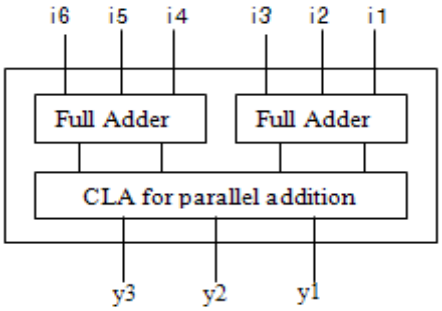

Fig.4. Block diagram of a 6-3 Compressor

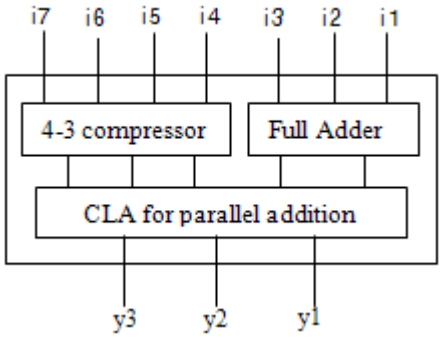

Fig.5. Block diagram of a 7-3 Compressor

IV. HIGHER-ORDER COMPRESSOR BASED VEDIC MULTIPLIER

In the earlier compressor based Vedic Multiplier [4], a large number of stages are required to add the partial products to obtain the final results. The 4-2 and 7-2 compressors are utilized only in the first two stages of the multiplier while the following eleven stages employ only full adder and half adder thereby increasing the reduction stages to thirteen .This leads to increased area and power consumption.

In the proposed multiplier architecture, the higher order compressors have been used intelligently so that the partial products are added in only two stages to obtain the final result and hence giving an area efficient and low power consuming design. Also, compressors and adders are employed such that minimum number of outputs is generated. For example in column 5, there are 7 partial products to be added. These could be added using a 4-3 compressor and a full adder thereby generating five output bits. But instead of this a 7-3 compressor has been used which will generate only 3 output bits. The same approach has been utilized for other columns as well. The dot diagram of the proposed multiplier is shown in Fig.6.

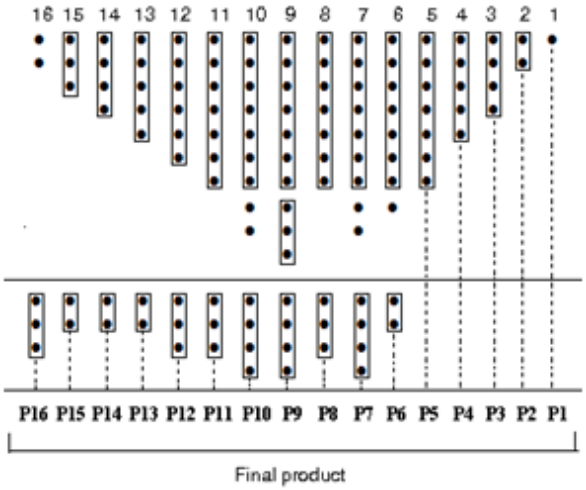

Fig.6. Dot Diagram of proposed 8X8 multiplier

V. MULTIPLIER PERFORMANCE AND COMPARISION

For performance comparison, various multipliers- Urdhwa Tiryakbhyam based Vedic multiplier, conventional compressor based Vedic multiplier and the proposed higher order compressor based Vedic multiplier, have been implemented in VHDL.

The design of 8x8 multiplier for each of these architectures was simulated and synthesized in Cadence RTL Compiler for 180 nm technology. The unoptimized gate count, area and power have been compared. The standard cell based fast library was used for synthesis. Fig. 7, 8 and 9 illustrates the comparative performance of the three multipliers in terms of gate count, area and power dissipation. It can be observed that the proposed multiplier uses 6.3% and

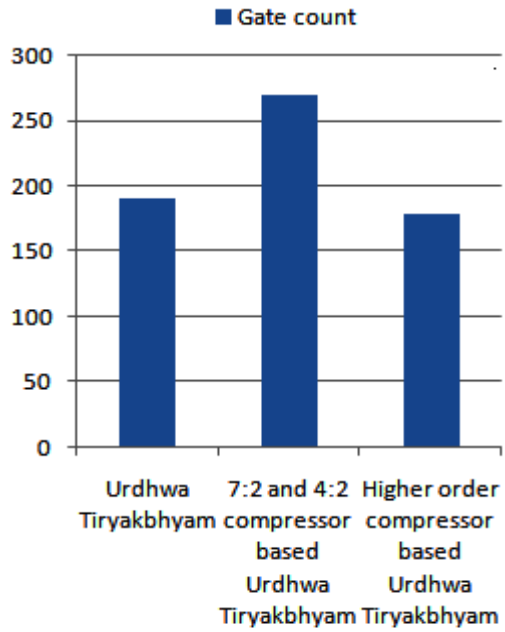

Fig.7. Gate count comparison for 8x8 multipliers

33.7% less gates and 12.9% and 25.8% less area in comparison to Urdhwa Tiryakbhyam based Vedic multiplier and conventional compressor based Vedic multiplier respectively.

The leakage power, dynamic power and total power dissipation for the three multipliers has been tabulated in Table III. It can be observed that the proposed multiplier dissipates 27.8% and 30.5% less total power than Urdhwa Tiryakbhyam based Vedic multiplier and conventional compressor based Vedic multiplier respectively as illustrated in Fig. 9.

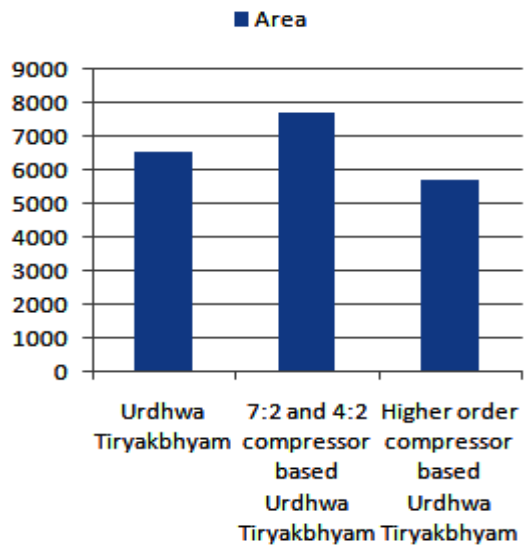

Fig.8. Area comparison for 8x8 multipliers

Table III
Power Dissipation Comparison

Type of Multiplier	Leakage Power (mW)	Dynamic Power (mW)	Total Power (mW)
Urdhwa Tiryakbhyam	0.234	811.634	811.868
Conventional compressor based Urdhwa Tiryakbhyam	0.284	842.715	842.999
Higher order compressor based Urdhwa Tiryakbhyam	0.198	585.753	585.951

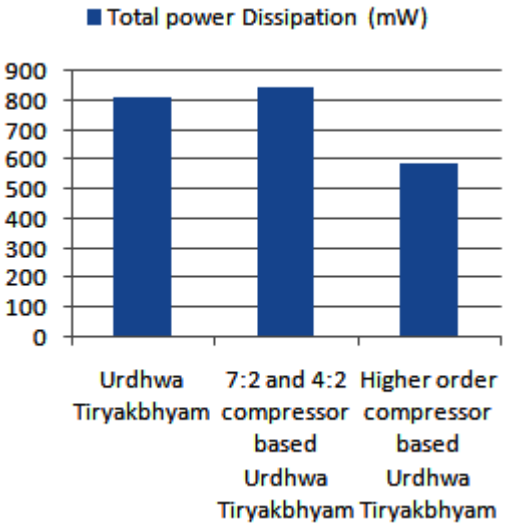

Fig.9. Power dissipation comparison for 8x8 multipliers

V. CONCLUSION

In this paper, various higher order compressors have been utilized to design an 8x8 multiplier. The performance of Urdhwa Tiryakbhyam based Vedic multiplier, conventional compressor based Vedic multiplier and higher order compressor based multiplier has been compared in terms of gate count, area and power dissipation.

The use of higher order compressors reduces the number of computational stages; thereby requiring lesser hardware. Hence the proposed design achieves significant reduction in area, leakage power, dynamic power and total power dissipation. The proposed Vedic multiplier architecture using higher order compressors can be used in area and power critical applications.

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