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DFT-Based Approach for Reducing Switching Activity during Scan Shift

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ABSTRACT
Power dissipation in digital circuits during scan based test is generally much higher than that during functional operation. Unfortunately, this increased test power can create hot spots that may damage the silicon, the bonding wires, and even the package. It can also cause intensive erosion of conductors-severely decreasing the reliability of a device. Finally, excessive test power may also result in extra yield loss. To address these issues, this paper first presents a detailed investigation of a benchmark circuit's switching activity during different modes of operation. Specifically, the average number of transitions in the combinational logic of a benchmark circuit during scan shift is found to be approximately 2.5 times more than the average number of transitions during the circuit's normal functional operation. A DFT-based approach for reducing circuit switching activity during scan shift is proposed. Instead of inserting additional logic at the gate level that may introduce additional delay on critical paths, the proposed method modifies the design at the register transfer level (RTL) and uses the synthesis tools to automatically deal with timing analysis and optimization.
Keywords **-** Automatic test pattern generation (ATPG), design for testability (DFT), functional power, power-sensitive scan cell, scan-based test.

I. INTRODUCTION

With Current advances in very large scale integrated technology (VLSI), the sensitivity of today's chips to deep submicrometer effects is increasing. Along with technology scaling, the increase in the operating frequency and the increase in the functional density of today's digital designs has led to new challenges for designers and test engineers. Furthermore, dynamic power consumption and IR-drop due to excessive switching activity are critical challenges. As a result, power reduction techniques have been extensively studied by both industry and academia with respect to both design and test.

Scan-based test remains one of the most widely accepted design-for-test techniques because it significantly improves the controllability and the observability of the circuit's internal nodes with an insignificant area and performance overhead.

When applying scan-based tests, test stimuli/test responses are loaded into/unloaded from the scan chain during scan shift. During capture, the scan cell contents are updated by applying capture clock(s).

Unfortunately, witching activity during scan-based test is often much higher than that during normal operation. There are multiple reasons for this phenomenon. First, the test vectors applied consecutively are not correlated. Second, nonfunctional states may be traversed during scan-test. Furthermore, test compaction and testing multiple cores simultaneously contribute toward high-switching activity. In addition, as patterns are shifted into and out of the scan chains, multiple changes of the flip-flop values can propagate into the combinational logic and cause massive amounts of switching. Excessive switching activity during test may destroy the chip, or decrease the reliability of the chip. It may also cause the chip to overheat and may lead to yield loss. Under such conditions, the design may fail to meet aggressive timing requirements when the supply voltage of the transistors is reduced by excessive IR-drop. As a result, a chip that would perform well during normal operation may be rejected during test, causing yield loss.

Power dissipation during scan test is analyzed in two categories depending on the clock cycles of interest. The test power consumed during scan shift cycles and capture cycles is referred to as the shift power and the capture power, respectively. During scan shift, the test stimuli are shifted into the scan chains one bit at a time, and they create transitions at the scan cell outputs that are further rippled through the combinational part of the circuit. In this paper, we focus our study on reducing shift power dissipation in scan-based tests through the insertion of additional logic at the register transfer level (RTL). The additional logic blocks the scan-cell transitions from propagating to the combinational logic in order to reduce the shift power consumption. The uniqueness of this method lies in the fact that the insertion of the extra hardware is performed at the RTL so that design constraints such as timing can be handled automatically by the synthesis tool.

II. EXISTING SYSTEM

To reduce the switching activity during scan shift, many different approaches have been proposed in literature. These approaches can be classified into two main categories: 1) automatic test pattern generation (ATPG)-based solutions; and 2) DFT-based solutions. The ATPG-based solutions attempt to reduce the test power dissipation during test generation, and they include nonrandom *X*-filling techniques, best primary input change time, application of a special input control pattern, test vector reordering, selection of the optimal test sequence, and power-aware test pattern generation algorithms etc. Chandra and Kapurt proposed a bounded adjacent *X*-fill technique where they studied the correlation between the scan-in test stimulus and the scan out test responses in order to reduce the shift and capture cycles' switching activity.

The advantage of the ATPG based solutions is that they do not modify the original design and the scan architecture. DFT-based solutions require one to either partition the conventional scan chain architecture or insert additional hardware into the design. The conventional scan architecture into a modified scan structure. The technique transforms a single scan path into a scan path with any number of length-balanced separate scan segments where only a certain number of the scan segments are enabled for each shift clock.

The multiple-phase clock scan technique (MPC-SCAN) inserts some additional logic into the conventional scan structure in order to generate multiple scan clocks that are out of phase with each other such that every scan chain will be controlled with a different scan clock. The simultaneous shift Operation of the multiple scan chains is blocked by the multiple phase clocks. The propagation of the test vectors in the compatible scan chain is done by a data copying procedure, where the first scan cell in the compatible scan segment gets its value from the scan-in input and holds it for certain number of clock cycles. During this hold time all the other subsequent scan cells in the same compatible scan segment will get assigned to their values by copying them from their upstream scan cells in the same compatible scan segment. The switching activity caused by shift of the test vectors into the scan chain is reduced by the data copying operation. All the scan cells that are incompatible with each other grouped into a single incompatible scan segment.

The test vector propagation on the incompatible scan segments is done by regular shift operation. The main disadvantage of these approaches is the large area overhead. Moreover, they may degrade circuit performance due to the extra logic added between the scan cell outputs and the functional logic. The supply gating transistors are placed on every gate that is directly driven by a scan cell. This technique reduces both dynamic and leakage power dissipation during shift mode. Given a set of test patterns, logic simulation is carried out to identify the violating shift cycles in which peak power violations occur. By using integer linear programming (ILP) techniques, the optimization problem is solved to select as few test points as possible such that all violating cycles can be eliminated. The disadvantages of this method are twofold: 1) inserted test points are test set dependent, therefore, violating cycles may not be eliminated when the test set is changed; 2) solving an ILP problem with a constraint matrix of the size of $Vc \times 2S$ is not applicable to large industrial circuits, where Vc is the total number of violating cycles, and S is the total number of scan cells. A medium size industrial circuit typically contains several hundred thousand scan cells. When simulating a random vector, the primary inputs and the pseudo-primary inputs (PPI) are set to the value *X* with pre-specified probabilities, and the number of gates becoming *X* after the change is used as a cost function to identify the logic value assigned at the primary inputs and the PPI, as well as to select scan cells to be held during scan shifting. To explore several hundred thousands of scan cells in an industrial circuit, a significant number of random vectors need to be simulated in order to choose good test points.

III. COMPARISON OF THE SWITCHING ACTIVITY DURING TEST AND FUNCTIONAL MODES

Compared to the power dissipation during normal operation, the research in low-power testing has highlighted that the increase in power dissipation during scan test is a significant problem for testing. However, a quantitative study of the switching activity during test as opposed to functional mode has not been published to the best of our knowledge. Thus, in this section, we present a quantitative analysis of the nature of the switching activity for an example circuit during test and functional modes. The example circuit is a benchmark circuit obtained from http://opencores.org/ and its function is to transform colors such as CIE XYZ↔RGB or RGB↔YCbCr. Fig. 1 shows the simulation flow for the functional inputs. The analysis flow for functional inputs is shown in Fig. 1. In this flow, an industrial synthesis tool is first used to synthesize the benchmark circuit from the RTL description to the gate level net list. During synthesis, the timing characteristics of the standard library cells are considered in order to allow comprehensive switching activity analysis carried out later at the gate level.

Our switching activity analysis flow only considers the timing information of the standard cells and the effect of the applied input patterns. More detailed switching activity analysis including the switching capacitance values of the cells can be performed if the layout information of the design is available.

Fig. 1. Analysis flow for functional inputs. After the gate level net list is created, we used ModelSimTM, to simulate the net list operated in functional mode. The test bench reads an ASCII coded input file that represents a picture and performs the color transformation. An ASCII coded output file is created after approximately 25000 clock cycles. When running the test bench, we made ModelSimTM generate a value change dump (VCD) file in order to record all the signal value changes at every gate that occurred during simulation.

The VCD file was processed by a script developed in house to analyze the distribution of the switching activity for all the nets over any specified time slot. In Table I, we show the average number of transitions per clock cycle at combinational library cell outputs and flip-flop outputs, respectively, after dividing the whole functional simulation into five time slots, 5000 clock cycles per slot. The average numbers of transitions per clock cycle over five time slots are given on the row *Average*. Next, we collected the switching activity during test mode for both shift and capture cycles. The analysis flow is shown in Fig. 2. Similar to the flow shown in Fig. 1, we first used the synthesis tool to create a gate level net list from the RTL description. We then ran the scan insertion tool to create the scan chain and the ATPG tool to generate 142 scan test patterns based on the stuck-at fault model. ModelSimTM was used next to simulate the test patterns according to the order they are generated. It is worth pointing out that we simulate the simultaneous scan in and scan out of adjacent patterns in order to collect accurate simulation data during test. Another VCD file was created during simulation for switching activity analysis.

The results of the switching activity analysis for the ATPG test patterns are shown in Table II. The average number of transitions per clock cycle at the combinational library cell outputs and the flip-flop outputs are listed in the rows *Shift* and *Capture* for the scan shift and capture, respectively. Comparing the switching activity between Tables I and II, it can be seen that the average number of transitions per clock cycle during scan shift is 2.3 and 2 times larger than that during normal operation for the combinational library cells and the flip-flop outputs, respectively. When considering the switching activity during capture, the ratios become higher, and they are 4.75 and 2 times larger than the switching activity during normal operation for the combinational library cells and the flip-flop outputs, respectively.

Although the number of transitions per clock cycle during scan shift is much lower than that during capture, it is worth pointing out that the number of shift cycles used to shift in a scan test pattern is typically much larger that the number of capture cycles in the same pattern. Therefore, heat accumulating during scan shift may damage the chip under test and cause the incorrect values captured into scan cell during capture. Reducing scan shift power is one of the major problems during test. Motivated by the switching activity analysis for functional and test modes shown above, a novel and effective method for reducing the switching activity during scan shift at RTL will be described in the next sections.

IV. PROPOSED SYSTEM

To significantly reduce scan shift power while minimizing extra hardware overhead, the approach uses the method described in the previous section to identify a small set of power-sensitive cells and their frozen values. Then, it modifies the circuit by replacing identified power-sensitive scan cells by frozen scan cells. A scan cell is said to be frozen during scan shift if an additional gate is inserted at the scan cell output and the logic value at the additional gate holds constantly during scan shift. Fig. 4(a) shows a scan cell without inserting an additional gate between the scan cell output and the functional logic it drives. Fig. 4(b) shows a frozen scan cell whose frozen value is logic 0. During scan shift, the scan enable signal *Scan−en* is asserted to 1 and the output value at the additional AND gate holds to 0. During capture and normal operation, *Scan−en* is disserted to 0 and the output of the scan cell drives the functional logic directly. Similarly, an additional OR gate can be inserted to freeze the scan cell to 1.

If the timing closure becomes invalid due to the change, one cannot insert the additional gate at that scan cell output, and hence the next most power-sensitive scan cell will be selected and evaluated. The problem of violating timing closure may prevent this method from being adopted in a practical design flow because: 1) re-evaluating timing is a tedious task; and 2) if the most power-sensitive scan cells happen to be on critical paths with small timing slacks, we cannot take advantage of these cells to reduce scan shift power.

To solve the problems mentioned above, a different flow to take advantage of power-sensitive scan cells for scan shift power reduction in this section. Instead of inserting the additional gates after the synthesis step, we move the circuit modification step to the RTL before synthesis. We rely on synthesis tools to meet the timing closure while allowing the freezing of power-sensitive scan cells during scan shift. In the proposed flow, we need to address two issues: 1) How to match the power-sensitive scan cells to the corresponding RTL bits; and (2) how to modify the RTL codes to freeze the power-sensitive cells.

3.1. Identifying Power-Sensitive RTL Bits

Since many designs in RTL are described in behavior rather than structure, directly extending the probability-based algorithm described in Section IV to identify the power-sensitive state elements defined in RTL is not only an extremely difficult task, but also not always feasible. We propose to quickly

synthesize the design in RTL to a "*prototype*" implementation ALPASLAN *et al.*: ON REDUCING SCAN SHIFT ACTIVITY AT RTL 1115 in gate level first. Then, the algorithm described in Section IV is applied to this prototype gate level net list in order to obtain a list of power-sensitive state elements to be scanned and their preferred frozen value. During synthesis, it is unnecessary to0 optimize the design in terms of performance and area, etc. What we need is a gate level implementation of the design for estimating signal probability. Once the power-sensitive state elements are identified from the prototype gate level net list, we map them back to the signal/variable bits in RTL codes by using hierarchical path names. The mapping is unique since the hierarchical path names in two levels of description must be the same. Then the design in RTL is modified such that the outputs of those power-sensitive signals/variables can hold to predefined values during scan shift. The detailed description of this step will be given in the next subsection.

By using the flow proposed above, it is worth mentioning that it is unnecessary to consider how the power-sensitive state elements identified in the RTL are stitched into the scan chain at the gate level. This is a distinct advantage because the power reduction obtained will be fairly constant even if the chains are spliced in different scan modes. The only assumption we made here is that the design will be converted to a full scan design at the gate level. If partial scan is preferred, it is straightforward to change the above flow to ensure that flip-flops that will not be on the scan chain will remain untouched.

3.2. Freezing Power-Sensitive RTL Bits

To block the transitions that occur at the outputs of the power-sensitive scan cells from propagating to the functional logic, a new primary input, named *scan enable*, is added into the RTL of the design. This signal can be reused during scan chain insertion at the gate-level after synthesis to control scan shift operation. Next, we create a new "potentially-frozen" Wire that will drive combinational gates, and its value depends on the value captured into the power-sensitive flip-flop during functional operation. Note that special attention must be paid when one or more bits of a multibit signal at the RTL must be frozen.

V. FIGURES AND TABLES

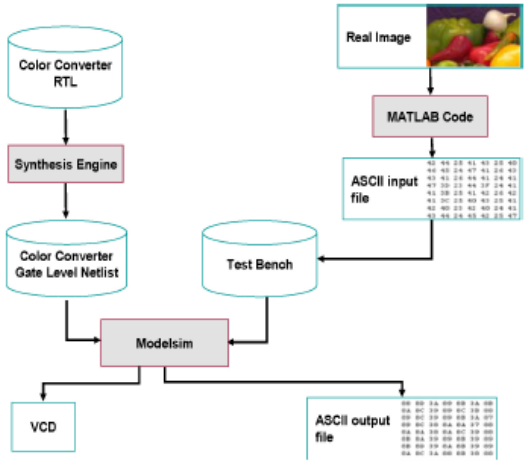

Fig. 1. Analysis flow for functional inputs.

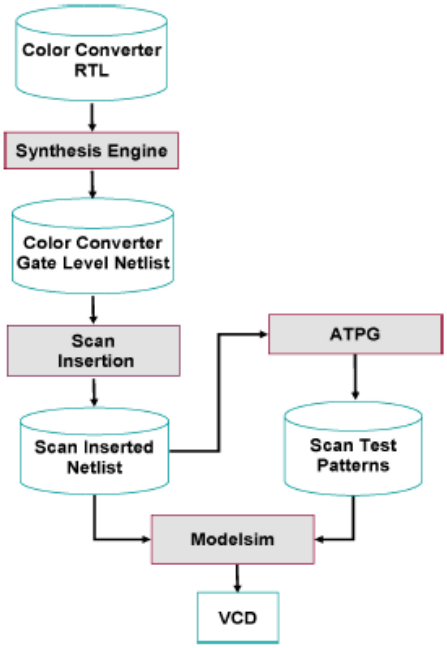

Fig. 2. Analysis flow for test patterns generated by ATPG.

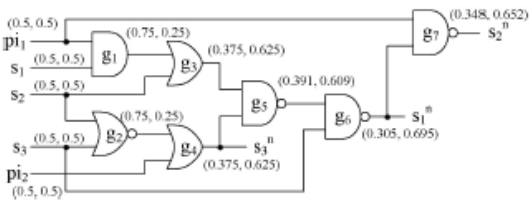

Fig. 3. Signal probability calculation.

TABLE I
AVERAGE NUMBER OF TRANSITIONS PER CLOCK CYCLE DURING FUNCTIONAL OPERATION

Time Slot	Average Number of Transitions Per Clock Cycle	
	Combinational Library Cell Outputs	Flip-Flop Outputs
1st 5000	656	135
2nd 5000	781	151
3rd 5000	758	155
4th 5000	687	143
5th 5000	638	136
Average	704	144

TABLE II
AVERAGE NUMBER OF TRANSITIONS PER CLOCK CYCLE FOR ATPG PATTERNS

Test Operation	Average Number of Transitions Per Clock Cycle	
	Combinational Library Cell Outputs	Flip-Flop Outputs
Shift	1620	286
Capture	3345	293

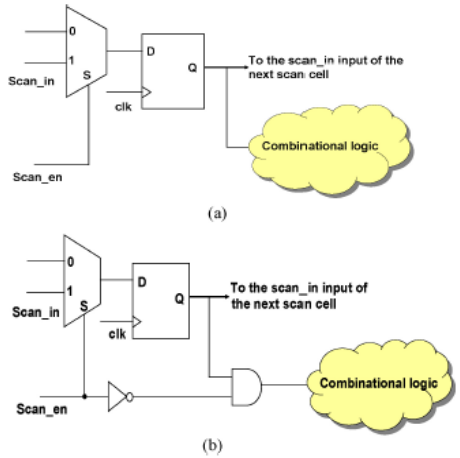

Fig. 4. Freezing a scan cell. (a) Original circuit. (b) Circuit after inserting an additional gate.

VI. CONCLUSION

In this paper, we have presented and analyzed a method for reducing switching activity during scan shift by freezing a small subset of all flip-flops at the RTL. We have shown that large reductions in switching activity can be achieved with very low-area overhead. The amount of scan flip-flops that are going to be frozen can be decreased or increased depending on the design's overhead budget. In comparison with previous methods, which freeze these flip-flops at the gate level, timing closure can be more easily met. When flip-flops are frozen at the gate level, individual Timing analysis have to be implemented to determine whether or not each flip-flop could be frozen without violating timing. By freezing all flip-flops simultaneously at the RTL,we allow the synthesis tool to automatically optimize for timing closure.

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