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An Area Efficient Enhanced SQRT Carry Select Adder

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ABSTRACT
In the design of Integrated Circuits, area occupancy plays a vital role because of increasing the necessity of portable systems. Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. In this paper, an area-efficient carry select adder by sharing the common Boolean logic term (CBL) is proposed. After logic simplification and sharing partial circuit, only one XOR gate and one inverter gate in each summation operation as well as one AND gate and one inverter gate in each carry-out operation are needed. Through the multiplexer, the correct output is selected according to the logic states of the carry in signal. Based on this modification a new architecture has been developed and compared with the regular and modified Square-root CSLA (SQRT CSLA) architecture. The modified architecture has been developed using Binary to Excess-1 converter (BEC). The proposed architecture has reduced area and delay as compared with the regular SQRT CSLA architecture. The result analysis shows that the proposed SQRT CSLA structure is better than the regular SQRT CSLA.

Keywords **-** Area efficient, Square-root CSLA (SQRT CSLA), Common Boolean Logic (CBL), Binary to Excess-1 Converter (BEC)

I. INTRODUCTION

Design of area and power efficient high speed data logic systems are one of the most substantial areas of research in VLSI system design. Addition usually impacts widely the overall performance of digital systems and an arithmetic function. In electronics applications adders are most widely used. In multipliers, DSP to execute various algorithms like FFT, FIR and IIR. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position [1].

The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independent generation multiple carries and then select a carry to generate the sum. However, the CSLA is not an area efficient because it uses multiple pairs of Ripple Carry Adders(RCA) to generate partial sum and carry by considering carry input as C_{in}=0 and C_{in}=1, then the final summation and carry are selected by the multiplexers.

The Carry select adders are classified as Linear Carry select adder and Square-root Carry select adder [6].

A. Linear Carry Select Adder:

The linear carry select adder is constructed by chaining a number of equal length adder stages. For an n-bit adder, it could be implemented with equal length of carry select adder and is called as linear carry select adder.

B. Square-root Carry Select Adder:

The square-root carry select adder is constructed by equalizing the delay through two carry chains and the block multiplexer signal from previous stage. It is also called as non-linear carry select adder.

The existing modified SQRT CSLA uses Binary to Excess-1 Converter (BEC) instead of RCA with C_{in}=1 in the regular CSLA to achieve lower delay with slightly increase in area. The basic idea of the proposed architecture is that which replaces the BEC logic by Common Boolean Logic. The proposed architecture generates a duplicate sum and carry-out signal by using NOT and OR gate and select value with the help of multiplexer [4]. The multiplexer is used to select the correct output according to its previously carry-out signal.

This paper is organized as follows; Section II and section III explains the regular and modified Square-root CSLA and detail structure of BEC respectively. A section IV deals with proposed architecture using Common Boolean Logic (CBL). Results are analyzed in the section V. Section VI with the conclusion.

II. REGULAR SQRT CARRY SELECT ADDER

The basic square-root Carry Select adder has a dual ripple carry adder with 2:1 multiplexer, the main disadvantage of regular CSLA is the large area due to the multiple pairs of ripple carry adder. The regular 16-bit SQRT Carry select adder is shown in Fig. 1. These 16-bits are divided into five groups with different bit sizes of ripple carry adders [7]. From the

structure of regular SQRT CSLA, there is scope for reducing delay and area utilization. The carry out is calculated from the last stage, in this the selection is done by using a multiplexer [1]. The internal structures of the group2, group3, group4 and group5 of the regular 16-bit SQRT CSLA is shown in Fig. 2.

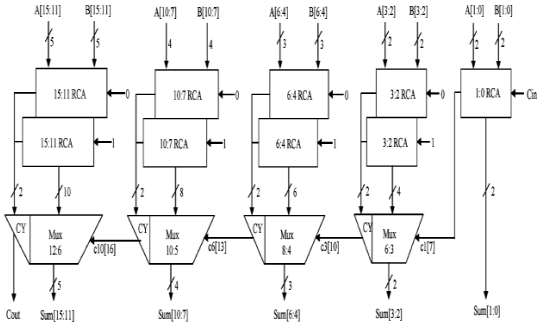

Figure 1. Regular 16-bit SQRT CSLA

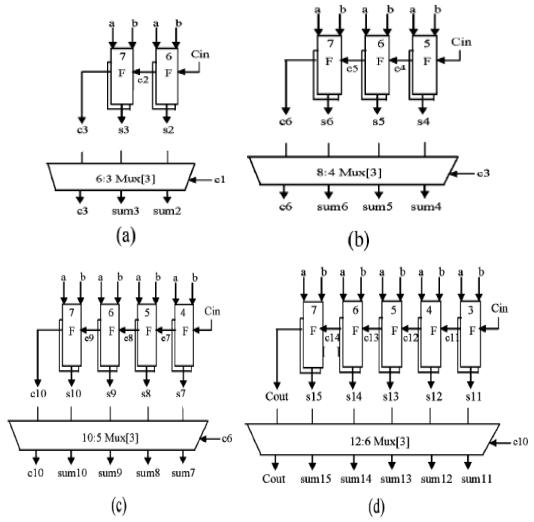

Figure 2. Individual groups of regular 16-bit SQRT CSLA

III. MODIFIED SQRT CARRY SELECT ADDER

The main idea of this work is to use BEC instead of the RCA with C_{in}=1 in order to reduce the delay and area utilization of the regular SQRT CSLA. To replace the n-bit RCA, a n+1 bit BEC is required [2]. The structure of a 4-bit BEC is shown in Fig. 3 and the function table given in Table I.

Fig. 3 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. In this structure one input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial outputs in parallel according to the control signal C_{in}. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed [1], [3]. The Boolean expression of the 4-bit BEC is listed as

X0 = ~B0
X1 = B0^B1
X2 = B2 ^ (B0 & B1)
X3 = B3 ^ (B0 & B1 & B2).

TABLE I. FUNCTION TABLE OF THE 4-BIT BEC

Binary [3:0]	Excess-1 [3:0]
0000	0001
0001	0010
:	:
:	:
1110	1111
1111	0000

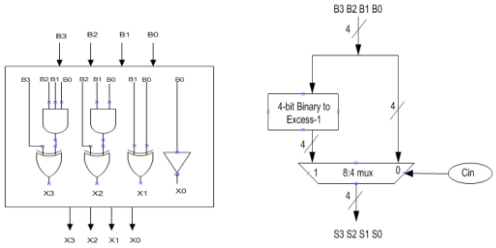

Figure 3. Struture of 4-bit BEC with 8:4 mux

The modified 16-bit SQRT CSLA using BEC is shown in Fig. 4. The structure is again divided into five groups with different sizes of Ripple carry adder and BEC. The group2, group3, group4 and group5 of 16-bit SQRT CSLA are shown in Fig. 5. The parallel Ripple carry adder with C_{in}=1 is replaced with BEC. One input to the multiplexer goes from the RCA with C_{in}=0 and other input from BEC. Comparing the individual groups of both regular and modified SQRT CSLA, it is clear that the BEC structure reduces delay. But the disadvantage of BEC method is that the area is increasing than the regular SQRT CSLA.

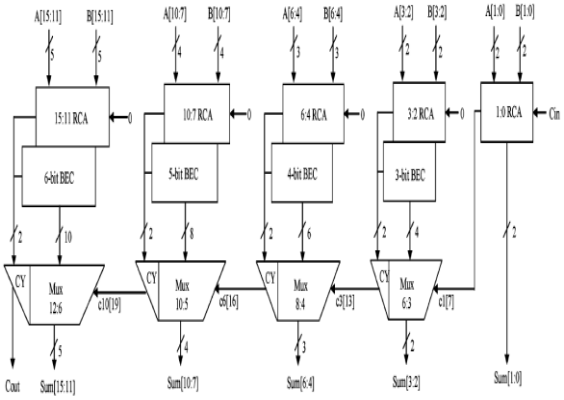

Figure 4. Modified 16-bit SQRT CSLA

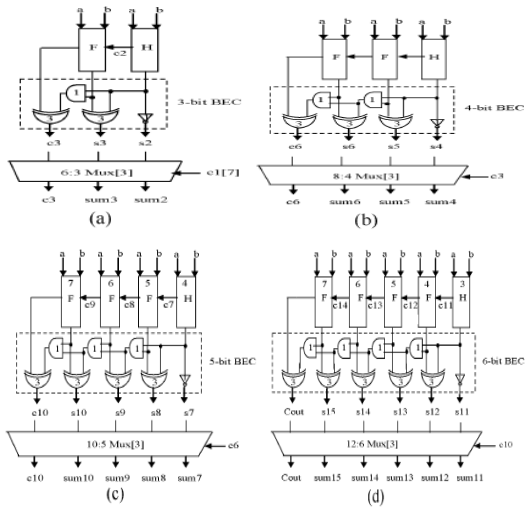

Figure 5. Individual groups of modified 16-bit SQRT CSLA

IV. PROPOSED SQRT CARRY SELECT ADDER

In proposed architecture, an area-efficient carry select adder by sharing the common Boolean logic term to remove the duplicated adder cells in the conventional carry select adder is shown in this way, it saves many transistor counts and achieves a low power. Through analyzing the truth table of a single bit full adder, to find out the output of summation signal as carry-in signal is logic '0' is the inverse signal of itself as carry-in signal is logic '1'. By sharing the common Boolean logic term in summation generation, a proposed carry select adder design is illustrated in Fig. 6. To share the common Boolean logic term, it only needs to implement one OR gate with one INV gate to generate the carry signal and summation signal pair. Once the carry-in signal is ready, then select the correct carry-out output according to the logic state of carry-in signal [4].

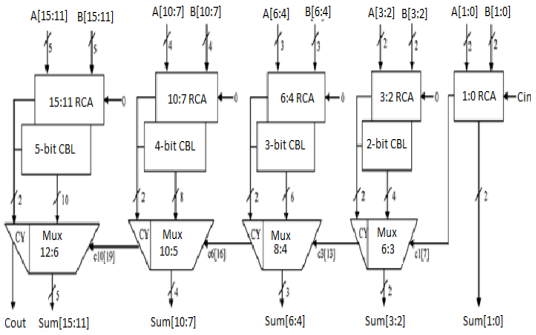

Figure 6. Proposed 16-bit SQRT CSLA

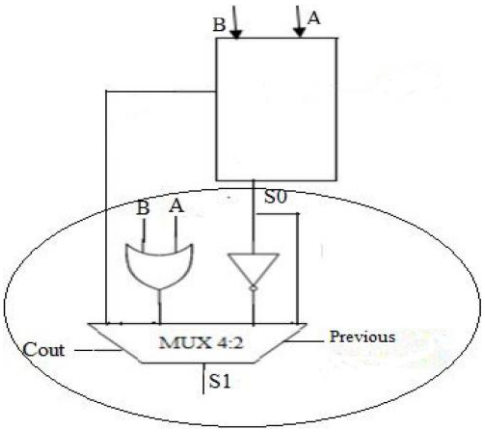

Figure 7. Single bit Full adder with CB

This method replaces the BEC add one circuit by Common Boolean Logic. The proposed 16-bit SQRT CSLA architecture is shown in Fig. 7. The summation and carry signal for full adder which has C_{in}=1, generate by INV and OR gate. Through the multiplexer, the correct output result is selected according to the logic state of carry-in signal. The internal structure of the group3 of proposed CSLA is shown in Fig. 8. One input to the mux goes from ripple carry adder block with C_{in}=0 and other input from the Common Boolean logic.

The group3 performed a three bit addition which are A[4] with B[4], A[5] with B[5] and A[6] with B[6]. This is done by one half adders (HA) and two full adders (FA). The CBL block has a 4:2 multiplexer to select the appropriate carryout and summation signal for carry-in signal "1". Through 2:1 multiplexer the carry signal is propagate to the next adder cell. The 6:3 multiplexer and 4:2 multiplexer is the combination of 2:1 multiplexer.

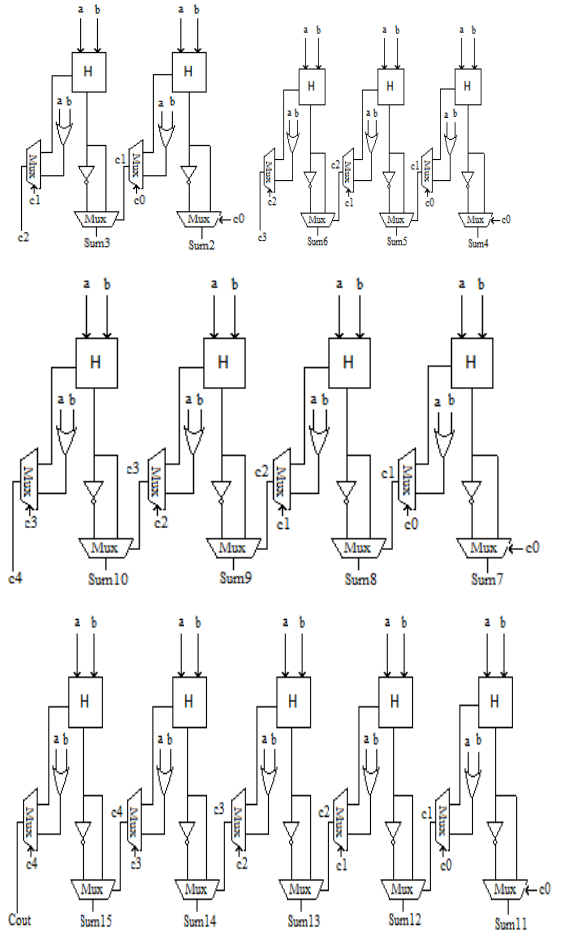

Figure 8. Individula groups of proposed 16-bit SQRT CSLA

As compared with the modified square-root carry select adder, the proposed square-root carry select adder is little bit faster and Area efficient.

V. RESULT ANALYSIS

The 8-bit SQRT CSLA is done by the same structure of 16-bit SQRT CSLA except group4 and group5. The 8-bit inputs are directly given to the full adder to complete the 8-bit sum and carry. The 32-bit SQRT CSLA is done by cascading the two 16-bit SQRT CSLA. Table. II exhibit the delay and area of regular, modified and proposed 16-bit SQRT CSLA. Simulation is carried out using Xilinx simulation tool and Spartan 3E as the target device. The major disadvantage of modified architecture using BEC is increasing area. This disadvantage is overcome in the proposed architecture which reduces area than the regular and modified Square-root Carry select adder. The comparison chart between area, delay and logic levels is shown below:

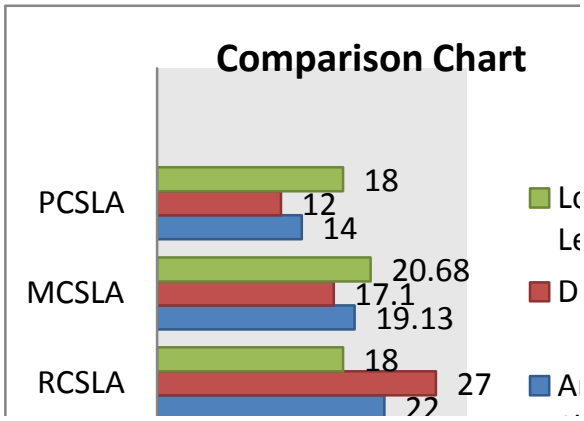

TABLE II. DELAY AND AREA COMPARISION OF 16-BIT SQRT CSLA

Adder Topology	Delay (ns)	Area (no. of Slices)	Logic Levels
Regular (with dual RCA)	19.13	22	14
Modified (with BEC)	17.11	27	12
Proposed (with CBL)	20.68	18	18

VI. CONCLUSION

The 8-bit SQRT CSLA is done by the same structure of 16-bit SQRT CSLA except group4 and group5. The 8-bit inputs are directly In this paper, an area efficient square-root carry select adder is proposed. By sharing the common Boolean logic (CBL) term, the duplicated adder cells in the conventional carry select adder is removed. The reduced number of gates of this work offers the great advantage in the reduction of area. The regular SQRT CSLA has the disadvantage of occupying more chip area. This paper proposes a scheme which reduces the area than the regular and modified SQRT CSLA. It would be interesting to test the design of the 64 and 128 bit SQRT CSLA.

REFERENCES

[1] B. Ramkumar and Harish M Kittur, "Low power and area efficient carry select adder", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 20, no. 2, pp. 371-375, Feb 2012.

[2] B. Ramkumar , Harish M Kittur and P. M. Kannan, "ASIC implementation of modified faster carry save adder", Eur. J. Sci. Res. , vol. 42, no. 1, pp. 53-58, Jun 2010.

[3] R. Priya and J. Senthilkumar, "Implementation and comparision of effective area efficient architecuture for CSLA", Proceedings of IEEE International

Conference on Emerging trends in Computing, Communicaton and Nano Technology, pp. 287-292, 2013.

[4] I-Chyn Wey, Cheng-Chen Ho, Yi-Sheng Lin and Chien-Chang Peng, "An area efficient carry select adder design by sharing the common boolean logic term", Proceedings on the International Multiconference of Engineering and computer scientist, IMECS 2012.

[5] T. Y. Ceiang and M. J. Hsiao, "Carry select adder using single ripple carry adder", Electron. Lett, vol. 34, no. 22, pp. 2101-2103, Oct 1998.

[6] J. M. Rabaey, *Digital Integrated Circuits-A Design Perspective*, Upper Saddle River, NJ: Prentice-Hall, 2001.

[7] Y. Kim and L. S. Kim, "64-bit carry select adder with reduced area", Electron. Lett. Vol. 37, no. 10, pp. 614-615, May 2001.

[8] Edison A. J and C. S. Manikanda babu, "An efficient CSLA architecture for VLSI hardware implementation", Interanational Journal for Mechanical and Industrial Engineering, vol. 2, Issue 5, 2012.

[9] P. Sreenivasulu, K. Srinivasa rao, Malla Reddy and A. Vinay Babu, "Energy and area efficient carry select adder on a reconfigurable hardwware", International Journal of Engineering Research and Applicaions, vol. 2, Issue. 2, pp. 436-440, Mar 2012.