RESEARCH ARTICLE OPEN ACCESS

Comparison of High Efficiency with Different Topology Transformerless Photovoltaic Power Converters

A Kurmaiah[1], S.Anil Kumar[2]
*(Assistant Professor,Department of EEE,JNTUH , Hyderabad)
** (Assistant Professor,Department of EEE,JNTUH,Hyderabad)

ABSTRACT
Transformer-less photovoltaic (PV) inverters offer better efficiency compared to inverters connected to the grid through a transformer providing galvanic isolation. However, in case the transformer is omitted, the generated common-mode voltage greatly influences the leakage current flowing to ground through the parasitic capacitance of the PV array. Hence, both the power stage and the modulation strategy of the converter, shall be properly designed to avoid leakage current while guaranteeing high efficiency and reactive power handling capability that are requested by national grid codes. In this paper, three single phase transformer-less inverter topologies are analyzed: the Highly Efficient and Reliable Inverter Concept converter (HERIC), a recently published topology based on a combination of step-down converters and a recently patented modification of the Neutral Point Clamped converter (NPC) optimized for MOSFET use. Simulation results are used to show: current waveform, reactive power handling capability, efficiency and produced common-mode Voltage.
Keywords - photovoltaic transformer-less inverter, efficiency, leakage current, common-mode voltage.

I. INTRODUCTION

The renewable energy sources, in particular those of photovoltaic (PV) origin, have experimented a great development in recent years mainly due to the special feed-in tariffs. The full-bridge (FB) inverter topology is widely adopted also for PV grid-connected applications, but the need of high efficiency and manufacturing cost reduction has led to new innovative topologies [1]. As pointed-out, the main method used to increase the efficiency is to eliminate the transformer. In this case the absence of galvanic isolation leads to leakage current flowing due to the capacitance coupling to earth provided by the PV panels. Hence the transformer-less structure requires more complex solutions, typically resulting in novel topologies in order to keep the leakage current and DC current injection under control in order to comply with safety issues. The aim of this paper is to analyze and to compare the performances of some new PV transformerless converters. Three topologies are described in Section II, their simulation results in terms of leakage currents, voltage to the ground, efficiency and reactive power handling capability are provided in Section III.

II. TRANSFORMERLESS PV INVERTER TOPOLOGIES

In the following section three power converters Topologies are outlined: the first topology is one with the best performances in industrial PV inverters, while the other two are emerging topologies recently published or patented.

2.1 HERIC topology

The topology called *"Highly Efficient and Reliable Inverter Concept"* (HERIC), commercialized by *Sunways,* derives directly from the Full-Bridge converter, in which a bypass leg has been added in the AC side by means of two back-to-back IGBTs operating at grid frequency. The HERIC circuit is shown in Fig. 2.1, where Cin is the DC-link capacitor, Lfi and Lfg are the output filter inductors, respectively on the inverter-side and gridside, and Cf is the filter capacitor. The bypass branch has two important functions: decoupling the PV array from The grid (using a method called *"AC decoupling"*), Avoiding the presence of high-frequency voltage Components across it and preventing the reactive power exchange between the filter inductors and Cin during the zero voltage state, thus increasing efficiency [2]. The converter operates as it follows (see Table I): during the positive half-cycle S+ remains connected, whereas S1 and S4 commutate at switching frequency in order to generate both active and zero vectors. When an active vector is present (S1 and S4 are ON), current flows from the PV panels to the grid, while, when a zero vector occurs, S1 and S4 are switched OFF and the current flows through S+ and D-, this is the freewheeling situation. On the other hand, when the negative cycle is coming, S+ goes OFF and S- goes ON, whereas S3 and S2 commutate at switching frequency. It means that an active vector is present when S3 and S2 are ON, therefore the current flows from the PV panel towards the load, thus when S3 and S2 turn off, a zero voltage vector is present in the load, then current flows through S- and D+. With regard to the classical Full-Bridge

converter, the HERIC inverter achieves a unipolar output voltage having the same frequency as the switching one. Moreover there are no high fluctuations at the DC terminals of the PV array, therefore the leakage current is very small.

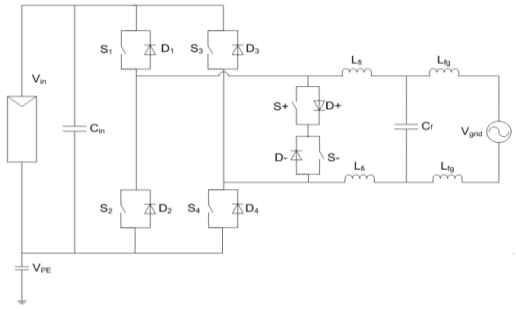

Fig.2.1.HERIC Inverter.

Table I. Conduction states for HERIC inverter.

S1	S2	S3	S4	S+	S-	D+	D-	Vout
ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	Vin
OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	0
OFF	ON	ON	OFF	OFF	ON	OFF	OFF	-Vin
OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	0

The modulation outlined in Table I does not provide capability of reactive power processing since the bidirectional switch of this topology made up of S+ and S- is not controlled to be turned-ON simultaneously, therefore current can only flow in a predefined direction, defined by the currently turned-ON switch. Modifying the switching strategy this inverter can inject reactive power into the grid [2].

2.2 Araujo topology

The basic principle of operation of the converter called *"Araujo topology"* [3] relies on two paralleled step-down converters that modulate a rectified sinusoidal current, with the output connected to the load using opposite polarities (Fig.2.2). The possible conduction states of the Araujo topology are depicted in Table II. The negative half-wave for both circuits is modulated by the high-frequency switching of S1 following a sinusoidal reference, while S4 remains turned on. When S1 is deactivated, the diode D1 provides the current freewheeling path, while the energy from the PV array is stored in the DC-link capacitors. Similarly, the positive half-wave is provided with S2 switching at high frequency, while S3 remains activated. Freewheeling occurs through D2. Moreover D3 and D4 are clamp diodes to protect the switches located on the grid side against possible transients. A small dead-band between the signals of the low frequency switches (equal to 30 μs @ 10 kHz switching frequency) shall be added to avoid grid short-circuit. In particular, unlike other inverters where both filter inductors are always active, in this Topology the current has to be equal to zero in the Inductor before turning off the respective low frequency switch, so that no overvoltage across the switch will happen.

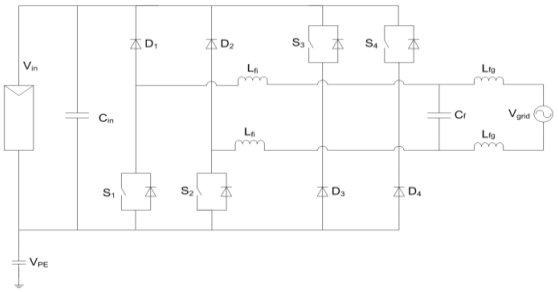

Fig.2.2: ARAUJO Inverter.

Table II. Conduction states for ARAUJO inverter

S1	S2	S3	S4	D1	D2	D3	D4	Vout
ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	-Vin
OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	0
OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	Vin
OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	0

A first advantage is the possibility to work with just one high frequency switch (S1 or S2) in every condition, reducing significantly the switching losses, while S3 and S4 are under a voltage stress equal to the grid voltage and operate only at grid frequency, reducing the conduction losses. Since the positive terminal of the PV-array is either directly connected to the phase output during the positive half-wave and to the neutral during the negative half-wave, there are no high-frequency oscillations to the ground, consequently leakage currents are avoided.

However with this converter it is also not possible to process reactive power.

2.3 NPC topology with decoupled output and MOSFETs

In order to increase the efficiency of a converter, it is desirable to use transistors that have low switching losses and anti-parallel/freewheeling diodes across each transistor with good recovery performance. MOSFETs are generally known to allow very fast switching, but the internal anti-parallel body diode exhibits poor recovery performance. This diode can conduct current even if another current path is available, such as a parallel connected freewheeling diode. When a MOSFET switch turns off, the current can transfer from the MOSFET channel into the parasitic body diode, while, when the control MOSFET turns on, the recovery charge stored in the

body diode during conduction is swept out. Abrupt reverse recovery of the body diode can cause higher switching losses and high frequency ringing, which places higher stresses on the components and can cause noise and EMI associated problems. To compensate, inverter designs using MOSFETs have traditionally required the addition of both series and freewheeling ultra-fast diodes. The addition of these diodes significantly increases the cost of the inverter design and adds conduction losses. For these reasons IGBTs have been a more practical choice for inverters operating above 100 to 200 VDC. IGBTs typically have poorer switching performance than MOSFETs, but require the addition of fewer diodes to provide rapid recovery behavior, since the internal series diode present in IGBTs allows the designer to add a single diode to the freewheeling path. The use of IGBTs can reduce the cost of an inverter design but may lower the inverter efficiency at higher frequencies.

Furthermore, when developing highly efficient inverter topologies which can handle reactive power, the intrinsic diode of the MOSFET will cause high reverse recovery losses when reactive power has to be managed.

Accordingly, there is a need to provide an inverter power module that effectively controls and minimizes the effect of the body diode of MOSFETs and specifically, there is a need to provide means to reduce the adverse effects of EMI and the power loss due to the parasitic body diode.

The disabling element which can be used in bridge or in neutral point clamped (NPC) configurations, can comprise a bypass diode for providing an alternative conduction path for a reactive load current or an inductor for decoupling the MOSFET from the reactive load. When decoupling the MOSFET by means of an inductor, also a bypass diode for the reverse path can be advantageous.

An inverter topology based on these principles is shown in Fig. 2.3. It is called "*NPC inverter with decoupled output and MOSFETs for all switches"* and can reach high values of the conversion efficiency [4]. The invention minimizes the effect of parasitic body diodes by preventing significant current flow through the internal body diode of MOSFETs present in the inverter circuit.

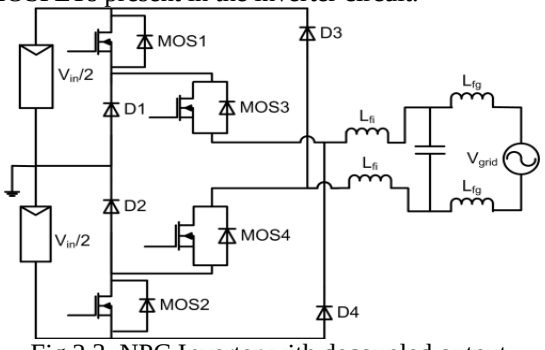

Fig.2.3. NPC Inverter with decoupled output.

Table III. Conduction states for NPC inverter with decoupled output and MOSFETs

M1	M2	M3	M4	D1	D2	D3	D4	Vout
ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	Vin
OFF	OFF	ON	OFF	ON	OFF	ON	OFF	0
OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	-Vin
OFF	OFF	OFF	ON	OFF	ON	OFF	ON	0

This ensures minimal body diode reverse recovery effects on every switching cycle. This topology is derived from the well-known NPC one, so the PWM strategy is quite similar and a three level output voltage is obtained, by switching MOS1 and MOS2 at high frequency and MOS3 and MOS4 at grid one. In particular, MOS1 and MOS3 are switched-ON during the positive half-wave, while MOS2 and MOS4 in the negative one and the reverse flow of the current is allowed by the four diodes, respectively D1-D3 and D2- D4 (see Table III). Moreover the reactive power is managed by the diodes D3 and D4, for whom Silicon Carbide ones are recommended in order to reach maximum efficiency in the reverse conduction [5].

III. SIMULATION RESULTS

To compare the performances of inverters in terms of leakage current, efficiency and reactive power handling capability, the mentioned topologies have been tested through simulations developed with PLECS toolbox, used for simulation of electrical circuits within the Simulink environment. The simulation parameters are reported in Table IV. The models of the PV converters have been developed on the basis of the thermal models of the following components: 600V TrenchStop IGBT, 650V CoolMOS™ Power Transistor, 600V 3rd Generation thinQ!™ SiC Schottky Diode and 1200V thinQ!™ SiC Schottky Diode. The SiC diodes are used in order to guarantee near-zero reverse recovery current, because it allows reducing switching losses.

Table IV. Parameters used in the simulations

Switching frequency [Hz]	**Fsw = 10khz**
Input DC voltage	**Vin = 500V**
DC link capacitance	**Cin = 1 mF**
Filter inductance inverter-side	**Lfi = 6.9 mF**
Filter inductance grid-side	**Lfg = 1 mH**
Filter capacitance	**Cf = 2.2 µF**
Grid voltage(peak of phase to neutral voltage)	**Vgrid = 325V**
Grid frequency	**Fg = 50 Hz**
Grid inductance	**Lg = 50 µF**
Rated power	**Pn = 1.6 KW**

3.1 HERIC topology

The HERIC inverter was introduced like a Modification of the Full-Bridge, in order to offer high Efficiency and constant common-mode voltage, using a technique called "*AC DECOUPLING".* The output Voltage of the inverter has three levels and the load Current ripple, shown in Fig. 3.1 (a), is very small, although the frequency of the current ripple is equal to the switching frequency.

As already mentioned, the HERIC topology generates no varying common-mode voltage, by disconnecting the PV from the grid during the state of the zero voltage, when the output of the inverter is short-circuited. This separation ensures that the common-mode voltage acting on the parasitic capacitance of the PV array does not change over time, therefore keeping the leakage current through the parasitic capacitance of the PV array at very low values. As shown in Fig. 3.1 (b), the voltage measured between the DC- terminal of the DC-link and ground has only a sinusoidal shape, therefore its spectrum has no high frequency content.

The HERIC topology, as also suggested by its name, has very high conversion efficiency throughout the whole working range (Table V), due to the fact that its bidirectional switch is controlled with the main frequency.

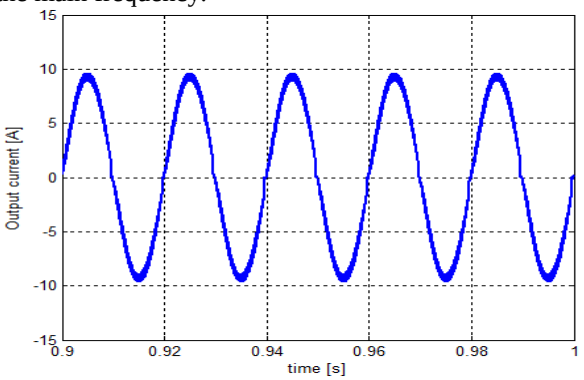

Fig.3.1 (a) Output current of the HERIC inverter.

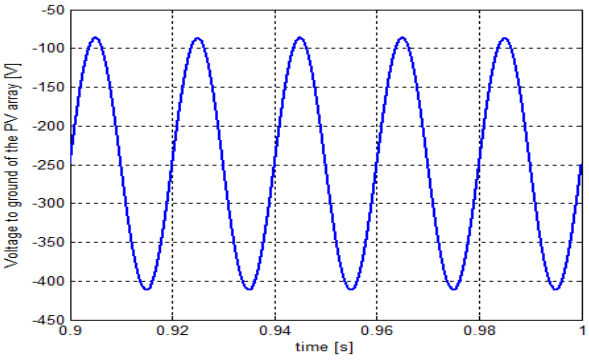

Fig.3.1 (b) Voltage to ground of the PV array for HERIC inverter.

Table V. HERIC inverter - Measured efficiency at different percentage of rated power

3.2 ARAUJO topology

The Araujo inverter exhibits high efficiency (Table VI), with low switching losses, thanks to the restricted amount of semiconductors among the other circuits, such as the HERIC topology. Also in this case, the obtained output voltage has three levels and the load current ripple (Fig. 3.2 (a)) is greater than in the HERIC inverter, leading to higher losses across the filter. The applied modulation strategy provides a small dead-band between the signals of the low frequency switches in order to avoid grid short circuit. As shown in Fig. 3.2 (b) and 3.2 (c), the current across one inductor is equal to zero, before turning off the respective low-frequency switch and no over voltages across the switch happen (please consider that L1 and L2 denote respectively Lfi of the upper and lower wire). Since the voltage to ground of the PV array has the waveform shown in Fig. 3.2 (c), the leakage current does not reach high values.

Table VI. ARAUJO inverter - Measured efficiency at different percentage of rated power

Transformerless Inverter Topology	**□ 5 %**	**□ 10 %**	**□ 20 %**	**□ 30 %**	**□ 50 %**	**□ 75 %**	**□ 100 %**
HERIC inverter	**98.08**	**98.44**	**98.45**	**98.40**	**98.33**	**98.29**	**98.27**

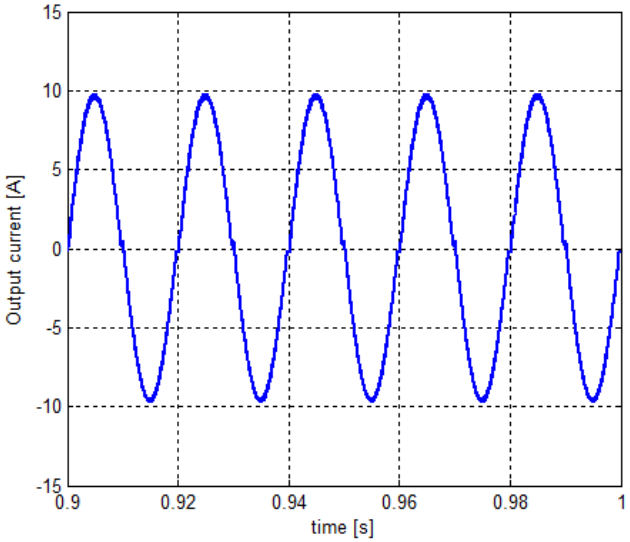

Fig.3.2 (a). Output current of the Araujo inverter

Transformer less nverter Topology	**□5 %**	**□10 %**	**□ 20 %**	**□ 30 %**	**□ 50 %**	**□ 75 %**	**□ 100 %**
HERIC inverter	**98.08**	**98.44**	**98.45**	**98.4**	**98.3**	**98.29**	**98.27**

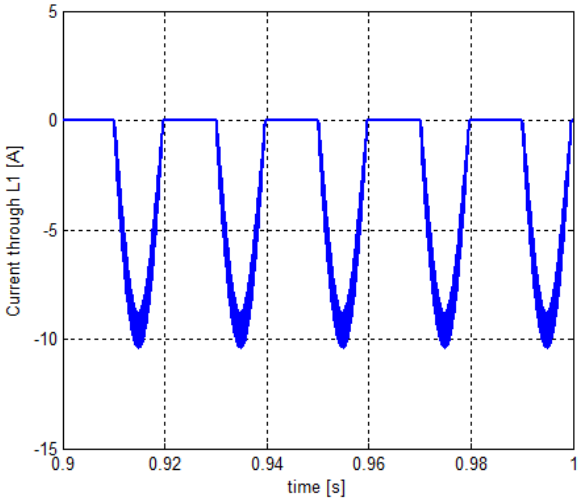

Fig.3.2 (b). Current in the inductor L1

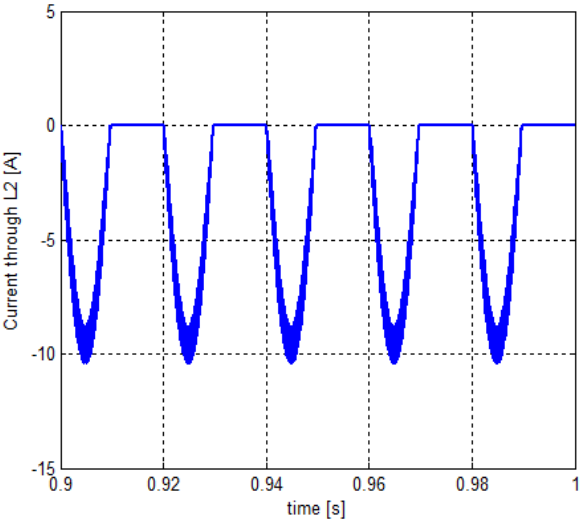

Fig.3.2 (c). Current in the inductor L2

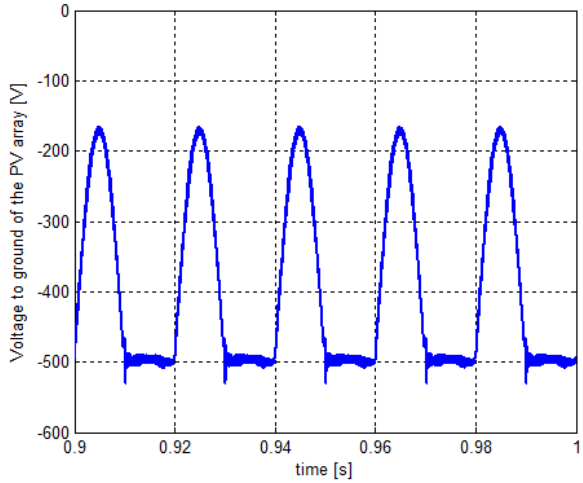

Fig.3.2 (d) Voltage to ground of the PV array

3.3 NPC topology with decoupled output and MOSFETs

The results obtained by testing the NPC inverter with decoupled output and MOSFETs are largely indicative of its excellent performance compared with previous inverters employing IGBTs. The classical NPC inverter allows reaching high value of efficiency, because switching losses are reduced due to the fact that the voltage rating of outer switches can be reduced to Vin/4 and one leg is controlled at lower frequency [6]. The NPC inverter with decoupled output and MOSFETs improves the performance of the classical NPC, in combination with reactive power handling capability. As shown in Table VII, the conversion efficiency reaches very high values, up to 99.13 % at 30% of rated load. The load current, as shown in Fig.3.3 (a), has a higher harmonic distortion than the other two topologies. Moreover, being the voltage VPE constant and equal to Vin/2 (see Fig. 3.3 (b)), the leakage current will be very low. The simulation results do not match exactly the expectations because the Plecs does not take into account precisely the intrinsic diode of MOSFET and its poor recovery performance.

Better results are expected by simulating this topology with *"Altium Designer"*: in this case, it is necessary to use *Spice* models for each electronic component, in which advanced operating features can be parametrically specify.

Table VII. NPC topology - Measured efficiency at different percentage of rated power

Transformerless Inverter Topology	**□5 %**	**□10 %**	**□ 20 %**	**□ 30 %**	**□ 50 %**	**□ 75 %**	**□ 100 %**
NPC topology with decoupled output and MOSFETS	**97.95**	**98.85**	**99.09**	**99.13**	**98.87**	**98.42**	**97.81**

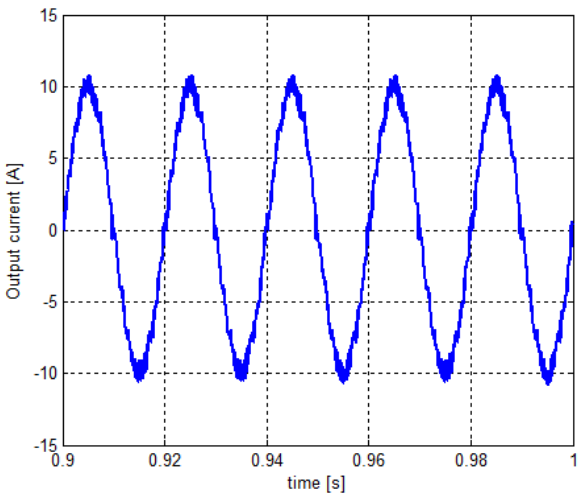

Fig.3.3 (a). Output current of the NPC inverter with decoupled output

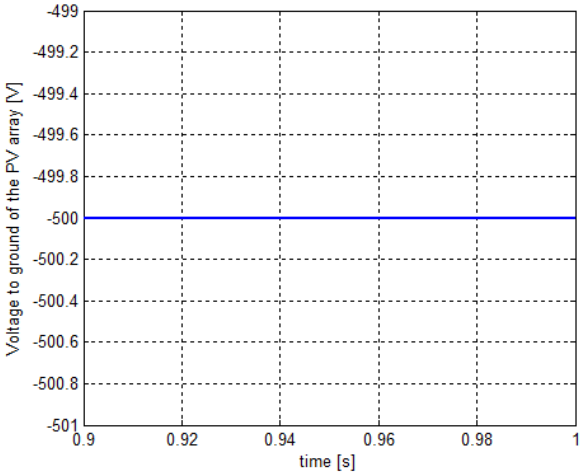

Fig.3.3 (c). Voltage to ground of the PV array

IV. HIGHEST EFFICIENCY COMPRESSION OF DIFFERENT TOPOLOGY

In this paper the Highly Efficient and Reliable Inverter Concept converter (HERIC), a recently published topology based on a combination of step-down converters (ARAUJO topology) and a recently patented modification of the Neutral Point Clamped converter (NPC) optimized for MOSFET and IGBT use are discussed and compared in terms of output common-mode voltage, efficiency and reactive power handling capability as shown in Table VIII.

Table VIII. Weight efficiencies and reactive power handling capability for the mentioned inverters

Transformer less Inverter Topology	**HERIC MOSFET inverter**	**HERIC IGBT inverter**	**ARAUJO MOSFET inverter**	**ARAUJO IGBT inverter**	**NPC MOSFETS inverter**	**NPC IGBT inverter**
□ EU[%]	98.34	**98.71**	98.23	**98.65**	98.68	**98.98**
□ CEC[%]	98.32	**98.68**	98.22	**98.62**	98.62	**98.80**
REACTIVE POWER	YES	**YES**	NO	**NO**	YES	**YES**

In order to compare the global efficiency of Photovoltaic inverters, two weighted values, called European efficiency (μEU) and Californian efficiency (μCEC), can be calculated as:

$$\_EU \_ 0.03\_\_5\% \_0.06\_\_10\% \_ 0.13\_\_20\% \_ 0.1\_\_30\% \_ 0.48\_\_50\% \_ 0.2\_\_100\ \% \quad \text{..... (1)}$$

$$\_CEC \_ 0.04\_\_10\% \_0.05\_\_20\% \_0.12\_\_30\% \_ 0.21\_\_50\% \_ 0.53\_\_75\% \_ 0.05\_\_100\ \% \quad \text{..... (2)}$$

Where μi% denotes the inverter efficiency at an in percentage of its rated power [7]. Testing all mentioned topologies in different operating points, it is possible to calculate their European and Californian efficiencies, which are represented in Table VIII. It should be noticed that the reactive power handling capability could be one of the most important comparison parameter in the future looking at national grid codes.

It has been verified that all mentioned topologies, except the Araujo one, guarantee this feature, as shown in Table VIII.

V. CONCLUSIONS

In this paper the Highly Efficient and Reliable Inverter Concept converter (HERIC), a recently published topology based on a combination of step-down converters (ARAUJO topology) and a recently patented modification of the Neutral Point Clamped converter (NPC) optimized for MOSFET use are discussed and compared in terms of output common-mode voltage, efficiency and reactive power handling capability. The HERIC topology results particularly good for transformer-less PV applications exhibiting higher efficiency and lower leakage currents than the Araujo topology. The NPC topology with decoupled output allows the highest efficiency compared to the others due to the use of MOSFETS in place of IGBTs. It provides also a constant voltage to ground of the PV array and very low leakage currents. Finally, both the HERIC and NPC topologies can handle reactive power.

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AUTHORS

Mr.A.Kurmaiah working as an Assistant Professor at Visvesvaraya College of Engineering & Technology, Hyderabad in Andhra Pradesh . His area of interest is Power system.

Mr.S.Anil Kumar working as an Assistant Professor at Visvesvaraya College of Engineering & Technology, Hyderabad in Andhra Pradesh. His area of interest is Power Electronics. He was ratified from JNTU Hyderabad.