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Various Low Power Techniques for CMOS Circuits

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Abstract
Designing high-speed low-power circuits with CMOS technology has been a major research problem for many years. The increasing demand for low-power design can be addressed at different design levels, such as software, architectural, algorithmic, circuit, and process technology level. This paper presents different approaches to reduce power consumption of any arbitrary combinational logic circuit by applying power minimization techniques at circuit level.
Index Terms—Static power, Dynamic power, Dual Vt, Multi threshold voltage, Stacking, Forced stack, Low power design

I. INTRODUCTION

In the past, the major concerns of the VLSI circuit designers were area, speed and cost. In recent years, this has changed dramatically and power dissipation is being given increased weightage in comparison to area and speed design metrics. Power wall is a clear and present roadblock in the semiconductor industry. The proliferation of portable and hand-held electronics combined with increasing packaging costs is forcing circuit designers to adopt low power design methodologies. Low power design of application specific integrated circuits (ASIC) result in increased battery life and improved reliability. Indeed, the Semiconductor Industry Association technology roadmap has identified low power design techniques as a critical technological need. Hence it becomes imperative for circuit designers to acknowledge the importance of limiting power consumption and improving energy efficiency at all levels of the design hierarchy, starting from the lower levels of abstraction, when the opportunity to save power is significant.

The remaining part of this paper is organized as follows. Section 2 highlights the reasons underpinning the choice of the logic style considered and its typical advantages. Section 3 deals with the issue of power dissipation in CMOS circuits. Section 4 surveys on power minimization techniques and finally conclude.

II. COMPLEMENTARY CMOS LOGIC STYLE

Complementary CMOS logic or Static CMOS logic style consisting of complementary nMOS pull-down and pMOS pull-up networks to drive '0' and '1' outputs are used for the vast majority of logic gates in digital integrated circuits. They have good design margins, fast, low power, insensitive to device variations, easy to design, widely supported by commercial CAD tools, and readily available in standard cell libraries. When noise does not exceed the margins, the gate eventually will settle to the correct logic level. Indeed many ASIC methodologies allow only complementary CMOS circuits. Even custom designs use static CMOS for 95% of the logic. They also enable low leakage designs owing to their inherent flexibility to accommodate leakage control transistors at the junction between the pull-up and pull-down network nodes .

Other advantages of static CMOS logic style are its robustness against voltage scaling and transistor sizing and thus ensuring reliable operation at low voltages and arbitrary transistor sizes. Input signals are connected to transistor gates only, which facilitates the usage and characterization of logic cells. The layout of CMOS gates is straightforward and efficient due to the complementary transistor pairs. Given the correct inputs, it will eventually produce the correct output so long as there were no errors in logic design or manufacturing. Static CMOS logic also has the advantage that there is no precharge/predischarge operation and charge sharing does not exist. Other circuit families tend to become prone to numerous pathologies, including charge sharing, leakage, threshold drops and ratioing constraints. Basically, CMOS fulfils all the requirements regarding the ease-of-use of logic gates.

III. POWER DISSIPATION IN CMOS CIRCUITS

Average power dissipation (Pavg) in CMOS digital circuits can be expressed as the sum of three main components , which are summarized in the following equation, as

Pavg = Pshort-circuit + Pleakage + Pdynamic

Pshort-circuit is the power from stacked P and N devices in a CMOS logic gate that are in the ON state simultaneously. This happens briefly during switching. This type of power dissipation can be controlled by minimizing the transition times on nets. It usually accounts for 15%-20% of the overall power dissipation.

Pleakage is the power dissipation due to spurious currents in the non-conducting state of the transistor. This component becomes a larger problem as device geometries shrink and transistor threshold voltages (Vt) drop. Leakage current depends upon the supply, Vdd (or how close it is with respect to Vt), Vt itself, transistor aspect ratio (W/L) and temperature. As the supply voltage scales down with technology, this increases exponentially and is construed to dominate the total power dissipation in ultra deep submicron technologies. Increasing die area also increases the leakage power adversely, as this increases the number of transistors.

Pdynamic is the dynamic power dissipation, also called the switching power. This is the dominant source of power consumption in CMOS system-on-chip (SoC), accounting for roughly 75% of the total. It is generally represented by the following approximation,

Pdynamic=α.CL.Vdd2.fclk

where 'α' is the switching activity factor (also called transition probability) and it tends to increase as the need for bandwidth increases, 'CL' is the overall capacitance to be charged and discharged in a reference clock cycle. Technology scaling has resulted in smaller transistors and hence smaller transistor capacitances, but interconnect capacitance has not scaled much with process and has become the dominant component of capacitance. 'Vdd' is the supply voltage. Though voltage scaling has the biggest impact on power dissipation (nearly quadratic savings in power), this generally comes at an expense of an increase in delay. 'fclk' is the switching frequency of a global clock for a globally synchronous design, local clock for a locally synchronous design or the input arrival rate in case of a pure static system.

IV. POWER MINIMIZATION TECHNIQUES

Power consumption in a static CMOS circuit basically comprises three components: dynamic switching power, short circuit power and static power. Compared to the other two components, short circuit power normally can be ignored in submicron technology.

A. Dynamic Power

Dynamic power is due to charging and discharging the loading capacitances.

B. Leakage power

The leakage current of a transistor is mainly the result of reverse-biased PN junction leakage, subthreshold leakage and gate leakage as illustrated in Figure 1.

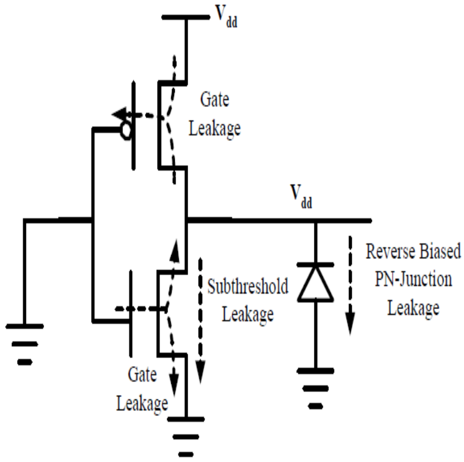

Figure 1 : Leakage currents in an inverter.

Leakage is becoming comparable to dynamic switching power with the continuous scaling down of CMOS technology. To reduce leakage power, many techniques have been proposed, including dual-*Vth*, multi-*Vth*, optimal standby input vector selection, transistor stacking and body bias.

1. Optimal Standby Input Vectors

Subthreshold leakage current depends on the vectors applied to the gate inputs because different vectors cause different transistors to be turned off. When a circuit is in the standby mode, one could carefully choose an input vector and let the total leakage in the whole circuit to be minimized model leakage current by means of linearized pseudo-Boolean functions.

2. Dual-*Vth* Assignment

Dual-*Vth* assignment is an efficient technique for leakage reduction. In this method, each cell in the standard cell library has two versions, low *Vth* and high *Vth*. Gates with low *Vth* are fast but have high subthreshold leakage, whereas gates with high *Vth* are slower but have much reduced subthreshold leakage. Traditional deterministic approaches for dual-threshold assignment utilize the timing slack of non-critical paths to assign high *Vth* to some or all gates on those non-critical paths to minimize the leakage power.

3. Multi-Threshold-Voltage CMOS

A Multi-Threshold-Voltage CMOS (MTCMOS) circuit is implemented by inserting high *Vth* transistors between the power supply voltage and the original transistors of the circuit. The original transistors are assigned low *Vth* to enhance the performance while high-*Vth* transistors are used as sleep controllers. In active mode, SL is set low and sleep control high-*Vth* transistors (MP and MN) are turned on. Their on-resistance is so small that VSSV and VDDV can be treated as almost being equal to the real power supply. In the standby mode, SL is set high, MN and MP are turned off and the leakage current is low. The large leakage current in the low-*Vth* transistors is suppressed by the small leakage in the high-*Vth* transistors. By utilizing the sleep control high-*Vth* transistors, the requirements for high performance in active mode and low static power consumption in standby mode can both be satisfied.

4. Super Cutoff CMOS Technique (SCCMOS)

This technique is very much similar to the MTCMOS but instead of a high Vth sleep transistor, a nominal Vth sleep transistor is employed to reduce the additional delay caused due to the presence of increased threshold value in sleep transistor.

5. SLEEP Transistor Technique

This is a State-destructive technique which cuts off either pull-up or pull-down or both the networks from supply voltage or ground or both using sleep transistors. This technique is MTCMOS, which adds high-Vth sleep transistors between pull-up networks and Vdd and pull-down networks and gnd while for fast switching speeds, low-Vth transistors are used in logic circuits. Isolating the logic networks, this technique dramatically reduces leakage power during sleep mode. However, the area and delay are increased due to additional sleep transistors. During the sleep mode, the state will be lost as the pull-up and pull-down networks will have floating values. These values impact the wakeup time and energy significantly due to the requirement to recharge transistors which lost state during sleep.

6. SLEEPY STACK Technique

This technique combines the structure of the forced stack technique and the sleep transistor technique. In the sleepy stack technique, one sleep transistor and two half sized transistors replaces each existing transistor. Although using of W0/2 for the width of the sleep transistor, changing the sleep transistor width may provide additional tradeoffs between delay, power and area. It also requires additional control and monitory circuit, for the sleep transistors.

7. SLEEPY KEEPER Technique

This technique consists of sleep transistors connected to the circuit with NMOS connected to Vdd and PMOS to Gnd. This creates virtual power and ground rails in the circuit, which affects the switching speed when the circuit is active. The identification of the idle regions of the circuit and the generation of the sleep signal need additional hardware capable of predicting the circuit states accurately, increasing the area requirement of the circuit. This additional circuit consumes power throughout the circuit operation to continuously monitor the circuit state and control the sleep transistors even though the circuit is in an idle state.

8. Transistor Stacking

The two serially-connected devices in the off state have significantly lower leakage current than a single off device. This is called the stacking effect. With transistor stacking by replacing one single off transistor with a stack of serially-connected off transistors, leakage can be significantly reduced. The disadvantages of this technique are also obvious. Such a stack of transistors causes either performance degradation or more dynamic power consumption.

9. Forced Stack

In this technique, every transistor in the network is duplicated with both the transistors bearing half the original transistor width. Duplicated transistors cause a slight reverse bias between the gate and source when both transistors are turned off. Because sub-threshold current is exponentially dependent on gate bias, it obtains substantial current reduction. It overcomes the limitation with sleep technique by retaining state but it takes more wakeup time.

10. Variable Threshold CMOS (VTCMOS)

Variable Threshold CMOS (VTCMOS) is a circuit design technique that has been developed to reduce standby leakage currents in low VDD and low VT applications. Rather than employ multiple threshold voltage process options, a VTCMOS circuit inherently uses low threshold voltage transistors, and the substrate bias voltages of the nMOS and pMOS transistors are generated by the variable substrate bias control circuit.

11. MULTI- PURPOSE TECHNIQUE

This technique has a combined structure of the following techniques.

- MTCMOS technique
- SCCMOS technique
- Forced stack technique

Unlike the MTCMOS and SCCMOS technique, This technique can reduce power consumption during active mode and retain the exact logic state and unlike the forced stack technique, it technique can save power consumption during standby mode.

12. ZIGZAG Technique

Wake-up cost can be reduced in zigzag technique but still state losing is a limitation. Thus, any particular state which is needed upon wakeup must be regenerated somehow. For this, the technique may need extra circuitry to generate a specific input vector.

13. LEAKAGE FEEDBACK Technique

This technique is based on the sleep approach. To maintain logic during sleep mode, the leakage feedback technique uses two additional transistors and the two transistors are driven by the output of an inverter which is driven by output of the circuit implemented utilizing leakage feedback. Performance degradation and increase in area are the limitations along with the limitation of sleep technique.

14. GALEOR Technique

In the Galeor technique two gated leakage transistors are inserted between pull-up and pull-down networks of CMOS circuit. Gated leakage NMOS transistor is placed between output and pull-up circuit and a gated leakage PMOS transistor is placed between output and pull-down circuitry. The gates of these additional transistors are controlled by the drain voltages. Gated Leakage transistors cause increase in resistance of the path from Vdd to ground since one of the leakage transistors is always near its cutoff region, thereby decreasing leakage current. Galeor technique reduces the leakage current to some extent but it suffers from a significant problem of low voltage swing. In this technique the logic low level is very much higher than 0 volts and logic high level is much lower than Vdd, which makes voltage swing to be lowered. This reduced voltage swing increases the propagation delay through the circuit.

V. CONCLUSIONS

When scaling down to deep sub-micron technology leakage is a critical problem. In this paper we have proposed some of the Power minimization techniques.

Experiments have to be conducted on these technique to decide which technique is best suited for power minimization.

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