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Mitigating and Protection of Power Systems for Peak Current Limitation with Fcl and Pll – Aided Fault Detection

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ABSTRACT

This paper presents a new method is that Phase locked loop and synchronization techniques are one of the most important issues for operating grid-interfaced converters in practical applications, which involve Distributed Power Generation Systems, Flexible AC Transmission Systems (FACTS), and High Voltage Direct Current (HVDC) Transmission, and so on. This paper presents a comprehensive review of the recently developed phase locked loop and synchronization methods that can be used to discriminate faults from switching transients. It is primarily intended for use in systems where fault is clearing before the first peak of the fault current are required.

Index Terms—Fault protection, phase-locked loop, power system, fault current limiters,fault current diverters,

I. INTRODUCTION

Short circuit power is often desired in an industrial system in order to connect and disconnect loads without causing disturbances to sensitive equipment or processes. With the high short circuit power, a high fault current develops in case there are faults in the system. This high fault current has to be considered when designing the switchgear and other components that build up the power system.

This is easily done in new installations but can be problematic when there is a need for higher short-circuit power in an existing system. In these cases, the installation of a fault current limiter could be an alternative to rebuilding the switchgear.This paper is structured in the following way: First, a back ground on fault current limiters and fault protection is given.

Finally, there is a section with concluding remarks and proposal for future work. Furthermore, a short appendix describing some methods of estimating power system signals is added for convenience. In [1], a trend toward increased short-circuit power is reported, which is also illustrated by an experience of more than 2 800 installations of fault-current limiters throughout the world.

II. FAULT CUREENT LIMITERS & DIVERTERS,ARC PROTECTION SYSTEMS

a.A fault current limiter is a device that during normal operating conditions allows a strong network but when a fault occurs, introduces enough impedance in the circuit so that the fault current is limited. The purpose of a fault current limiter is to limit the fault current so that its prospective peak value never is reached. The current limiting functionality can be achieved in several ways and power-electronic-based current limiters. (e.g.,current limiting reactors [2]; fuses [3]; triggered fuse [1];

b. Fault current diverters can be used as an alternative to fault current limiters. A current diverter consists of a switch that is in open position under normal operating conditions. When a fault is detected, the switch closes and short circuits the phases of the power system to earth at a predetermined location. One example of a current diverter is given in [4]. It is a de- vice that in case of a short circuit involving an open arc operates quickly and achieves a short circuit between phases and earth, thus short-circuiting the arc. The voltage drop across the arc becomes practically zero, making the arc extinguish.

c. Arc protection systems**.** An arcing fault in an enclosed substation environment will, if not extinguished, lead to extensive damage and potential harm to safety against human hazard. As the arc develops the temperature will rise and in turn cause the pressure to rise. After approximately a pressure wave will travel through the substation A pressure relief that opens when the pressure exceeds a certain threshold can to a certain extent but not completely mitigate the potential damages caused by the pressure wave. If the arc is not extinguished, it will rapidly cause severe meltdown of conductors and partitions, hence damaging the switchgear so that extensive repair or even replacement is necessary. An arc is relatively easy to detect using the light from the arc as a fault detector. The signal from the fault detector can then be used to trip the main circuit breaker thus extinguishing the arc.The damage to the substation is then limited but some maintenance is required before

the substation can be put back in service. It is possible to achieve a shorter arc extinguishing time if a bypass switch is used. The bypass switch is closed thereby short-circuiting the arc by closing a parallel path to earth. Two examples of such bypass switches are available as an Arc Eliminator [5] or an Arc Terminator[6] Both switches operate to extinguish the arc .

III. PROTECTION OF POWER SYSTEM

As concluded in the previous section, power system protection is another important issue. It is essential for safe operation of the power system that faults are detected and cleared automatically in a fast and reliable manner so that the operation of the power system is not disturbed. A typical fault protection system is built from circuit breakers (CBs), protection relays, and primary transducers, such as voltage and current transformers and auxiliary equipment.

Even though the detection of faults is the primary concern for fault protection devices (dependability), the ability to distinguish between a fault and a switching transient (security) is also important. Switching transients can, under certain circum- stances, give rise to high currents, which are much larger in magnitude than normal load currents. In existing relay protection, capacitor energization and transformer energization have been detected by analyzing the measured current to find certain characteristics of the two types of current transients as de- scribed in, for example, [7].

IV. PROPOSED METHOD

In this section, the proposed method of using a PLL for discrimination between faults and switching transients will be described. First, a short description of the basics of a PLL is given. Second, a well-known implementation of a PLL suitable for simulation purposes is described and the relevant signals that are used for the actual discrimination between a fault and a switching transient are identified. Third, the tuning of the parameters of the PLL implementation is discussed and suggestions for a first selection of parameters are given.

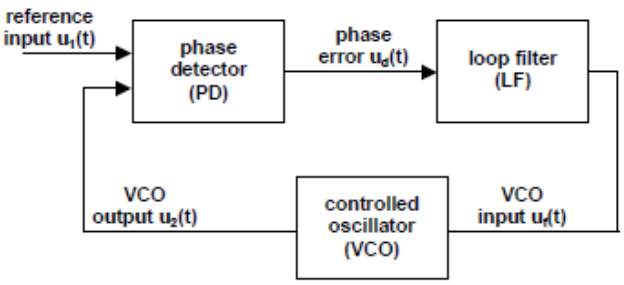

Fig. 1 Block diagram of basic PLL structure

A. Basics of a PLL

The PLL has been an important device in electronics and power system applications ever since the first implementation in the 1930s by de Bellescize. by de Bellescize, as mentioned in [8]. A PLL is a circuit that is used to synchronize an input signal with respect to phase and frequency ,hence the name phase locked.

Recent research related to PLLs has been from several research fields: general descriptions of PLLs [9], distributed generation applications [10], active power-line conditioner applications [11], servo controllers [12], as well as protection and control [13]–[15].

B. Description of a PLL that is Suitable for the Discrimination Between a Fault and a Switching Transient

A vector implementation of a PLL is described in this paragraph. The error signal $e(t)$ corresponds to the output of the PD, whereas the proportional-integral (PI) regulator and the integrator corresponds to the loop filter and the voltage controlled oscillator error signal is fed through a PI regulator

$$\begin{aligned} I_a &= I \cdot \sin(\omega t) \\ I_b &= I \cdot \sin\left(\omega t - 2 * \frac{\pi}{3}\right) \\ I_c &= I \cdot \sin\left(\omega t + 2 * \frac{\pi}{3}\right). \end{aligned} \quad (1)$$

Then, the Clarke's components I_α and I_β equate to

$$\begin{aligned} I_\alpha &= \frac{(2 \cdot I_a - (I_b + I_c))}{3} = I \sin(\omega t) \\ I_\beta &= \frac{(I_b - I_c)}{\sqrt{3}} = -I \cos(\omega t). \end{aligned} \quad (2)$$

Now, with reference to Fig. 2, the error signal is given by

$$e(t) = I_\alpha \cdot \cos(\theta) + I_\beta \cdot \sin(\theta) = I \sin(\omega t - \theta). \quad (3)$$

Thus, the error is zero exactly when the output angle of the PLL is in phase with the current of phase a. When a transient occurs in the system, the error signal will deviate from zero. The behavior of the error signal of the PLL will also depend on the tuning of the PLL.

C.Tuning of the PLL

The PLL will be tuned to the power system frequency. PLL shave been used for many years in HVDC transmission in order to synchronize the firing of the thyristors to the phase angle of the connected ac system. It is thus a well-known procedure and it is advisable to use parameters from such an installation as a starting point for the tuning.

D. Fault Detection and Discrimination Using a PLL

The method that is used to detect a fault and discriminate the fault from a switching transient is described here. Two algorithms are executed in parallel. The first algorithm is based on the estimation of the magnitude of the current. If the estimated magnitude is higher than a preselected threshold, a flag is set. The second algorithm is as previously mentioned, monitoring the error signal of a PLL.

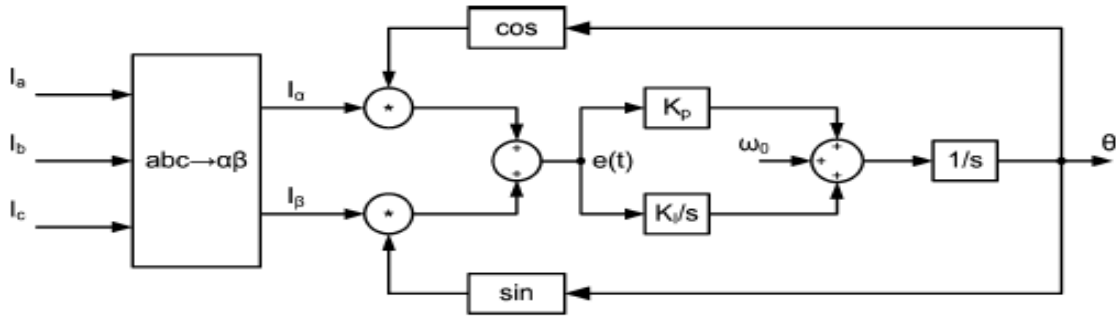

Fig. 2

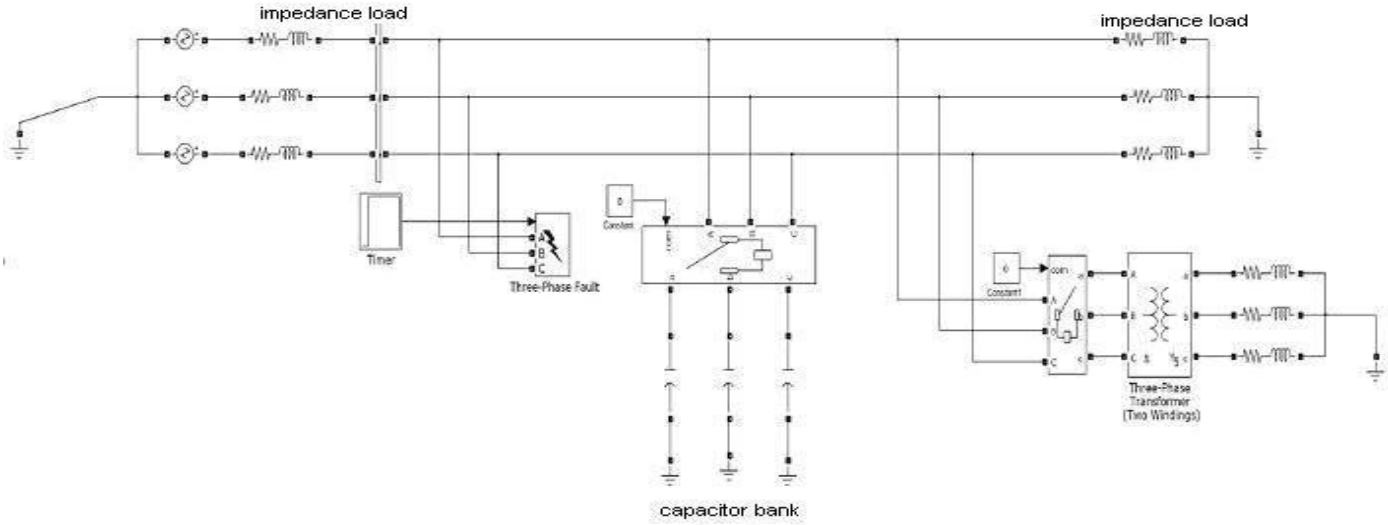

Fig. 3

The test system, consists of an infinite source, an impedance load, a shunt capacitor a transformer (with an associated CB), and a fault.

V. SIMULATION AND RESULT

In order to test the proposed method, a simple test system has been developed and implemented in an ElectromagneticTransients Program (PSCAD/EMTDC) selection arrangement. The data of the system are summarized as follows.

- The infinite source is modeled with a voltage source that is connected in series with an impedance. The supply voltage of the source has been chosen as $U_k = 12$ kV. The series impedance has been chosen so that the power system will have a short-circuit power of approximately $S_k = 831$ MVA m 0.55 mH). The supply frequency of the voltage source is selected to 50 Hz. A short-circuit power of $S_k = 831$MVA will give a short-circuit current of approximately $I_k = 40$ kA.
- The shunt capacitor is modeled by a capacitance of $C = 90.19\,\mu$F. The shunt capacitor gives a reactive power supply of 4.08 MVAr at nominal voltage. The shunt capacitor is connected to the power system by a CB which, at the start of the simulation, is open. The capacitor is uncharged at the start of the simulation.
- The transformer is modeled by a transformer model available in the master library of PSCAD/EMTDC. The winding voltages of the transformer are 12 kV at the primary side and 240 V at the secondary side. The leakage reactance is 0.122 p.u. on a transformer rating of

10.2 MVA. The residual flux in the transformer is also modeled.

- A. Simulated Events A large selection of shunt faults, capacitor energizations, and transformer energizations have been simulated. The instant when the event occur will determine some of the characteristics of the transient current such as, for example, the magnitude and possible dc offset.

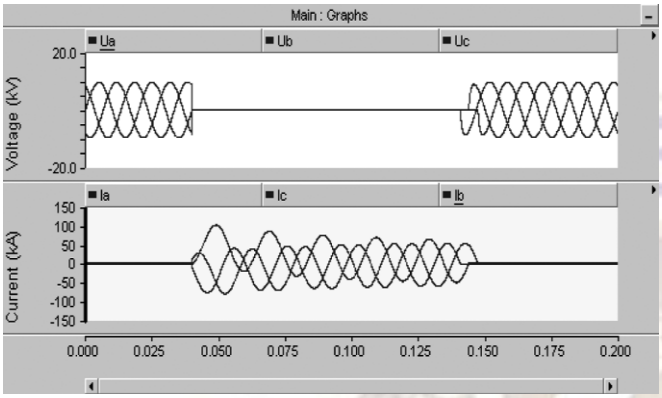

Fig. 4. Phase voltages and currents due to a three-phase fault.

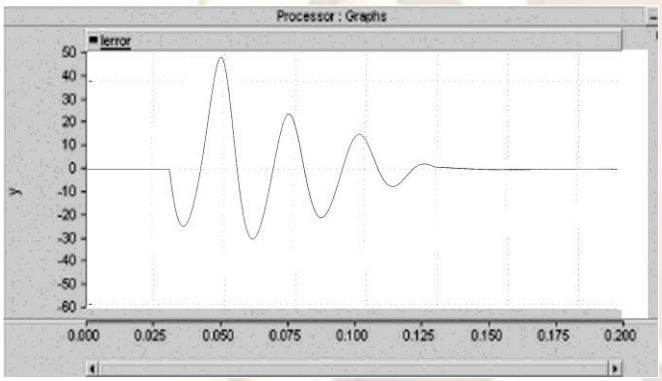

Fig. 5. Error signal due to a three-phase fault (in per unit).

VI. Results

A large number of results are available as a result from the simulations. A few selected results are presented here.

1.Faults: This section contains plots of signals caused by shunt faults in the power system. Both three phase and phase to phase faults have been analyze. Faults have been applied with different fault inception angles. The magnitude of the error signal of the PLL was well above 10 p.u. for all fault inception angles

2.Transformer Energization: In this section, plots of signals (voltages, currents, and relevant parameters from the control system) caused by transformer energization in the power system are presented. Typical phase voltages and phase currents

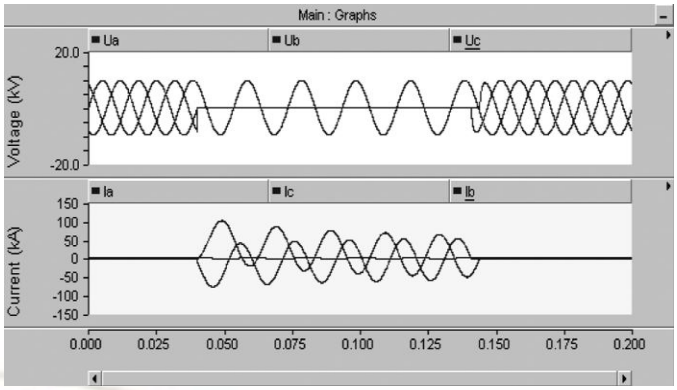

Fig. 6. Phase voltages and currents due to a phase-to-phase fault.

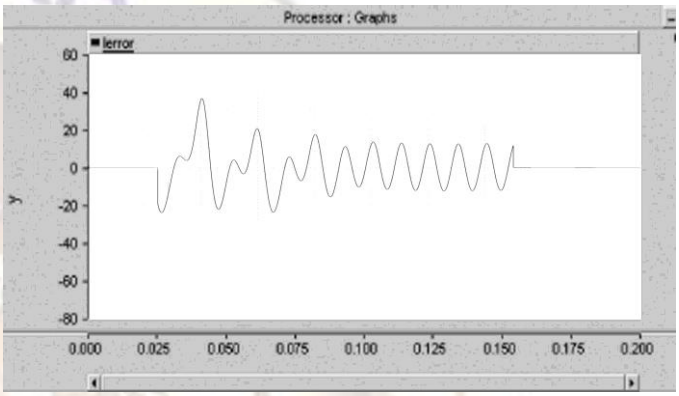

Fig.7.Error signal due to a phase-to-phase fault

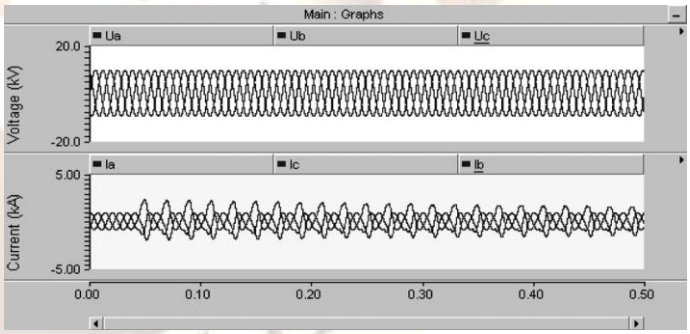

Fig. 8. Phase voltages and currents due to transformer energization.

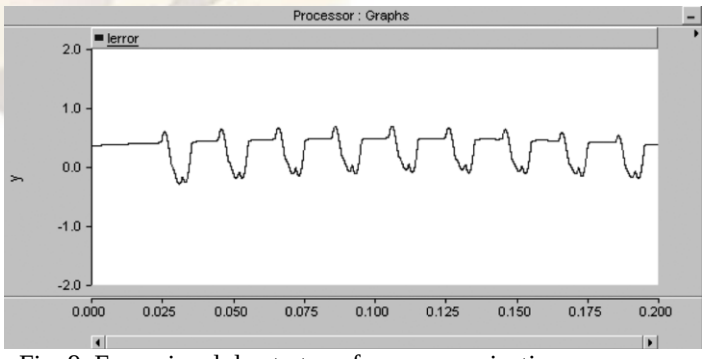

Fig. 9. Error signal due to transformer energization (in per unit).

transformer energization are plotted The error signal of the PLL for this event. As can be seen from that figure, the error signal deviates from zero shortly after the event has occurred but returns to steady state when the

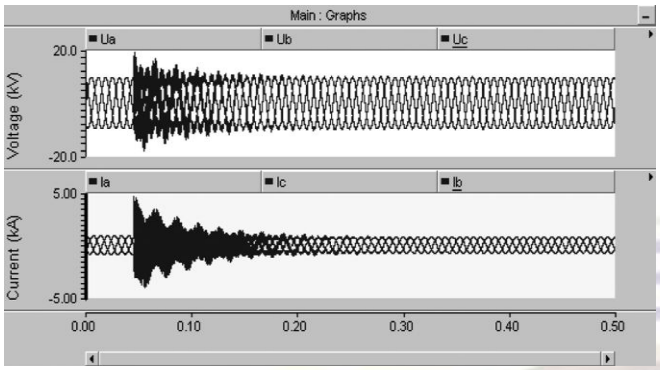

Fig. 10. Phase voltages and currents due to capacitor energization.

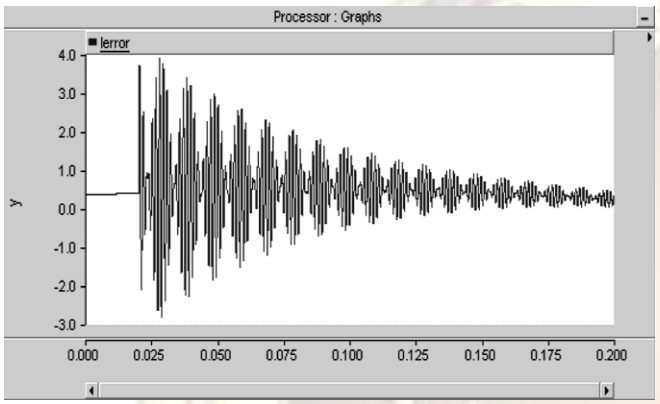

Fig. 11. Error signal due to capacitor energization (in per unit.)

PLL has adapted to the new conditions. Different switching instants were investigated and the magnitude of the error signal was never above 2 p.u.

3.Capacitor Energization: In this section, plots of signals (voltages, currents, and relevant parameters from the control system) caused by capacitor energization in the power system are presented. Different switching instants were investigated and the magnitude of the error signal was never above 5 p.u.

Analysis of the Proposed Method

First, a threshold for the measured current magnitude is selected. It can be concluded that the algorithm is able to discriminate between a fault and a switching transient. The magnitude based protection algorithm, all four transients would have been considered as faults since the first threshold was reached. In order to use a pure magnitude based protection algorithm, the first threshold would have to be increased.

VII. CONCLUSSION AND FUTURE WORK

In this paper, I have been demonstrated that a PLL can be used to determine whether a current transient is due to a fault in the system or due to a switching transient. Transformer and capacitor switching have been specifically studied due to the large occurrence of these switching transients in the power system. Simulations have been performed using a test system where faults and switching transients have been simulated The work presented in this paper is based on simulations and theoretical investigations. The focus has been on discrimination between switching transients and low impedance faults.

VIII. CALCULATIONS

RMS Value Calculation: The rms value of a current is estimated from measured current samples as

$$I_{rms} = \sqrt{\frac{\sum_{k=0}^{n} i_k}{n}} \qquad (A.1)$$

where i_k denotes the measured current samples and denotes the number of samples that are used for the rms calculation. Typically, is selected so that the rms calculation is performed over one period of fundamental power system frequency.

FFT-Based Calculation: The peak value of a current is estimated from measured current samples in two steps. First, the orthogonal components I_c and I_s are calculated as

$$I_c = \frac{2}{K}\sum_{k=1}^{K} i_k \cos(k\theta) \qquad (A.2)$$

and

$$I_s = \frac{2}{K}\sum_{k=1}^{K} i_k \sin(k\theta). \qquad (A.3)$$

Finally, the estimated peak current is calculated as

$$I_p = \sqrt{I_c^2 + I_s^2}. \qquad (A.4)$$

LSQ-Based Calculation: The peak value of a current can be estimated from measured current samples by fitting the measured current samples to a signal model. Three measured current samples can be fitted to the signal model

$$i(t) = I_c \cos\omega_0 t + I_s \sin\omega_0 t. \qquad (A.5)$$

If it is assumed that the frequency in the system is known the signal model contains two contains two unknown parameters .The three measured currents samples are fitted to the signal model by a least square approach and Ic and Ia are calculated as

$$I_c = \frac{[i_1 \cos\theta + i_0 + i_{-1} \cos\theta]}{1 + 2\cos^2\theta} \qquad (A.6)$$

and

$$I_s = \frac{[i_1 - i_{-1}]}{2\sin\theta}. \qquad (A.7)$$

Finally, the estimated peak current is calculated as

$$I_p = \sqrt{I_c^2 + I_s^2}. \qquad (A.8)$$

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