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VLSI Design in MIMO-OFDM for Wireless LAN Networks

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Abstract

MIMO-OFDM (Multiple Input Multiple Output-Orthogonal Frequency Division Multiplexing) technology has been utilized widely in wireless communication systems for faster transmission of data and efficient bandwidth utilization. MIMO-OFDM technology is the core of the 4th generation wireless networks. However, the computational complexity of MIMO OFDM receivers is much higher than in the single-input single-output (SISO) OFDM approach. This paper presents, to the best of the knowledge, the first 4 × 4 MIMO-OFDM WLAN physical layer ASIC based on the OFDM specifications of the IEEE 802.11a standard. and a VLSI design of MMO-OFDM systems targeted to future wireless LAN systems. Implementation provides reference for the silicon complexity of MIMO-OFDM systems

Keywords-MIMO, OFDM, SISO, VLSI Design, wireless networks, LAN.

I. INTRODUCTION

In the past decade we have witnessed explosive growth in the wireless communications industry with over 4 billion subscribers worldwide. While first and second generation systems focussed on voice communications, third genera- tion networks (3GPP and 3GPP2) embraced CDMA (code division multiple access) and had a strong focus on enabling wireless data services. As we reflect on the rollout of 3G services, the reality is that first generation 3G systems did not entirely fulfill the promise of high-speed transmission, and the rates supported in practice were much lower than that claimed in the standards. Enhanced 3G systems were subsequently deployed to address the deficiencies. However, the data rate capabilities and network architecture of these systems are insufficient to address the insatiable consumer and business sector demand for the nomadic delivery of media and data centric services to an increasingly rich set of mobile platforms Multiple-input multiple-output (MIMO) systems [1, 2] employ multiple antennas at both transmitter and receiver to significantly improve link reliability and throughput of wireless communication systems. These gains come at no additional transmit power or bandwidth expenditure. MIMO is considered the key enabling technology for future wireless local area networks (WLANs) and wireless local loop (WLL) systems targeting peak data rates of up to 1 Gbps [3]. IEEE 802.11a [4] is an established WLAN standard that provides data rates of up to 54 Mbps using single-input single-output (SISO) antenna technology and employ- ing orthogonal frequency division IEEE 802.11n standard, which extends the IEEE 802.11a standard to higher data rates by using up to four antennas at both transmitter and receiver. While ASICs for the IEEE 802.11a standard have been presented (e.g. [5]), little is known about suitable VLSI architectures for MIMO-OFDM systems and the corre- sponding silicon complexity. To the best of our knowledge no ASIC implementation of a MIMO-OFDM WLAN transceiver with up to four transmit and receive antennas has been reported much in the literature to date.

II. WHAT IS MIMO-OFDM?

OFDM has many advantages compared to other transmission techniques.One of such advantages is high spectral efficiency (measured in bits/sec/Hz).The 'Orthogonal' in OFDM implies a precise mathematical relationship between the frequencies of the sub-channels that are used in the OFDM system [1][2]. Each one of the frequencies is an integer multiple of a fundamental frequency. This ensures that a sub-channel does not interfere with other sub-channels even though the sub-channels overlap. This results in high spectral efficiency [6].
OFDM has been adopted in the IEEE802.11a LAN and IEEE802.16a LAN/MAN standards. OFDM is also being considered in IEEE802.20a, a standard in the making for maintaining high bandwidth connections to users moving at speeds up to 60 Mbps. The IEEE802.11a LAN standard operates at raw data rates up to 54 Mbps (channel conditions permitting) with 20 MHz channel spacing, thus yielding a bandwidth efficiency of 2.7 b/s/Hz. The actual throughput is highly dependent on the MAC protocol . Likewise, IEEE802.16a operates in many modes depending on channel conditions with a data rate ranging from 4.20 to 22.91 Mb/s in a typical bandwidth of 6 MHz, translating into a bandwidth efficiency of 0.7 to 3.82 bits/s/Hz.

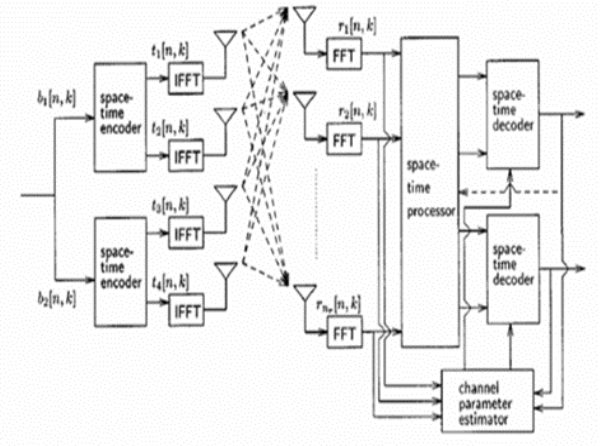

Figure 1. Block diagram of MIMO-OFDM

Multiple antennas can be used at the transmitter and receiver, an arrangement called a MIMO system. A MIMO system takes advantage of the spatial diversity that is obtained by spatially separated antennas in a dense multipath scattering environment. MIMO systems may be implemented in a number of different ways to obtain either a diversity gain to combat signal fading or to obtain a capacity gain. Generally, there are three categories of MIMO techniques. The first one aims to improve the power efficiency by maximizing spatial diversity. Such techniques include delay diversity [2], STBC, and STTC [6][7]. The second class uses a layered approach to increase capacity. One popular example of such a system is V-BLAST suggested by Foschinietal, where full spatial diversity is usually not achieved. Finally, the third type exploits the knowledge of channel at the transmitter. It decomposes the channel coefficient matrix using SVD and uses these decomposed unitary matrices as pre and post-filters at the transmitter and the receiver to achieve near capacity.

III. DIVERSITY IN MIMO-OFDM

In telecommunications, a diversity scheme refers to a method for improving the reliability of a message signal by using two or more communication channels with different characteristics. Diversity plays an important role in combating fading and co-channel interference and avoiding error bursts[7]. It is based on the fact that individual channels experience different levels of fading and interference. Multiple versions of the same signal may be transmitted and/or received and combined in the receiver. Alternatively, a redundant forward error correction code may be added and different parts of the message transmitted over different channels. Diversity techniques may exploit the multipath propagation, resulting in a diversity gain, often measured in decibels.

a) Time diversity: Multiple versions of the same signal are transmitted at different time instants. Alternatively, a redundant forward error correction code is added and the message is spread in time by means of bit-interleaving before it is transmitted. Thus, error bursts are avoided, which simplifies the error correction.

b) Frequency diversity: The signal is transmitted using several frequency channels or spread over a wide spectrum that is affected by frequency-selective fading.Example of it is OFDM modulation in combination withsubcarrier interleaving and forward error correction.

c) Space diversity: The signal is transmitted over several different propagation paths. In the case of wired transmission, this can be achieved by transmitting via multiple wires. In the case of wireless transmission, it can be achieved by antenna diversity using multiple transmitter antennas (transmit diversity) and/or multiple receiving antennas (reception diversity). In the latter case, a diversity combining technique is applied before further signal processing takes place. If the antennas are far apart, for example at different cellular base station sites or WLAN access points, this iscalled macrodiversity or site diversity. If the antennas are at a distancein the order of one wavelength, this is called microdiversity.

d) **Polarization diversity**: Multiple versions of a signal are transmitted and received via antennas with different polarization. A diversity combining technique is applied on the receiver side.

e)Cooperative diversity: Achieves antenna diversity gain by using thecooperation of distributed antennas belonging to each node.

IV. SIMULATION RESULT OF MATLAB:

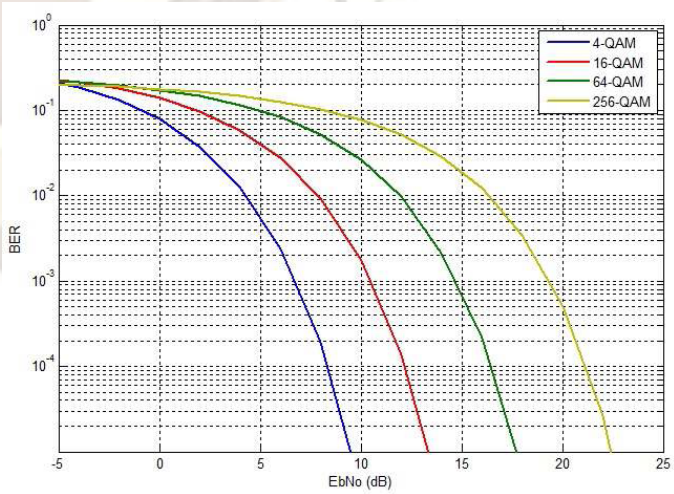

Figure 2 Plot for various sampled signal

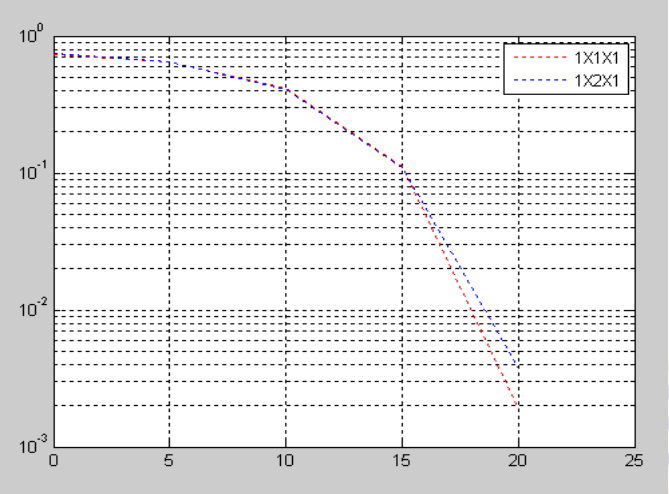

Figure 3 Plot showing MIMO have higher signal to noise ration and lesser Bit error rate as compared to SISO systems

V. HARDWARE IMPLEMENTATION ASPECTS IN VLSI

The gains achievable in MIMO(-OFDM) systems come at an (often significant) increase in hardware complexity. Little is known about suitable VLSI architectures for MIMO(-OFDM) systems and the corresponding silicon complexi- ty. The first commercial MIMO(-OFDMA) chip set was developed by IospanWireless, Inc. in 2002 for a proprietary fixed wireless system. This chip set supported two-stream spatial multiplexing and space-time coding. Several companies have announced MIMO-OFDM chip sets for the upcoming IEEE 802.11n WiFi standard.

Compared to a SISO transceiver, the 4 × 4 MIMO transceiver requires the four-fold replication of most functional blocks and, in addition, a channel-matrix preprocessor for MIMO detection and the MIMO detector itself; as a result, the overall chip area increases by a factor of 6.5. The main bottleneck in implementing the 4 × 4 MIMO system was found to be the latency incurred by preprocessing the channel matrices for MIMO-OFDM detection. We therefore conclude that algorithms for computationally efficient MIMO-OFDM channel matrix preprocessing, such as those described in [9], are of utmost importance for practical implementations.

VI. HIGH-LEVEL VLSI ARCHITECTURE

Our ASIC is partitioned into three major blocks as shown in Figure 4. The block denoted as multi-antenna OFDM processing is responsible for OFDM demodulation and for frequency offset correction and frame start detection. The MIMO detection unit (MDU) is in charge of performing spatial separation of the individual data streams. Finally, a FIFO buffer is required to bridge the latency period incurred by the MDU. The system is externally configurable through an AMBA peripheral bus (APB).

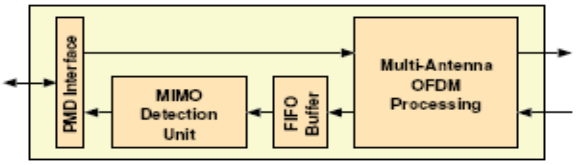

Figure 4: Block diagram of MIMO-OFDM transceiver

VII. Multi Antenna OFDM Processing

We shall next describe the individual elements of the multi-antenna OFDM processing block depicted in Figure 5.

OFDM modulation and demodulation: The bit stream to be transmitted is mapped to QAM symbols followed by a 64-point IFFT, parallel-to-serial conversion and extension of the resulting time-domain sequence by a cyclic prefix of length 16. Since IEEE 802.11a is a time divisionduplex (TDD) system, the same hardware can be reused toperform the FFT. Moreover, one I/FFT hardware block is shared by the four transmit (receive) antennas. At the system clock frequency of 80 MHz, a single-butterfly radix-4 I/FFT was found to provide sufficient performance.

Digital up/down conversion: In order to reduce the number of required off-chip data converters and the associated large pin-count, I/Q de-/modulation is performed in the digital domain (using an IF of 20 MHz). This methodalso eliminates the problem of I/Q imbalance. However,the digital up-conversion (DUC) and the digital downconversion(DDC) for the four antennas require a significantamount of registers and multipliers.

Automatic gain control (AGC): The considerable peak-to-average power ratio of OFDM signals renders AGC very important. We applied AGC to each antenna separately and used the following two-stage algorithm: The first stage generates a control signal for gain control in the analog domain. The second stage operates in the digital domain, at the input of the DDC. The AGC adjusts the signal level within 3.2 μs after the frame start.

Frequency offset estimation (FOE) and compensation: FOE is based on the Schmidl-Cox algorithm [7] with the
corresponding autocorrelation function obtained by estimating a weighted (across the four antennas) correlation function; the weights are chosen to undo the effect of the second stage (digital part) of the

AGC. The FOE block employs six real-valued multipliers. The frequency offset is compensated using one complex-valued multiplier in the frequency offset compensator (FOC) block

Frame start detection (FSD): The start of a frame is detected by having the AGC detect a substantial power increaseon at least three of the four receive antennas. The frame start detection process is assisted by the FOE block providing a metric indicating periodicity in the incoming signal which is a characteristic signature of the preamble of a frame.

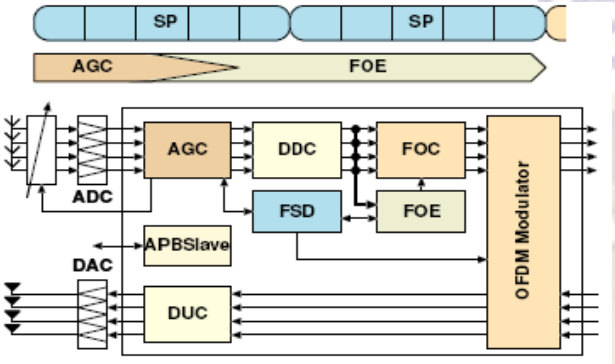

Figure 5: Different phases of frame acquisition (top) and block diagram of the multi-antenna OFDM processing unit (bottom).

VIII. MIMO DETECTION UNIT

The use of OFDM converts the MIMO wideband channelinto NC parallel narrow-band MIMO channels so that detection of the spatially multiplexed data streams can be carried out on a tone-by-tone basis. The input-output relation for the i-th tone is given by

$$y_i = H_i s_i + n_i, \quad i = 1, \ldots, N_C \qquad (1)$$

where si and yi denote the transmitted and received vector respectively, ni is thermal noise and Hi is the effective channel matrix corresponding to the i-th tone. MIMO detection aims at estimating si from yi. To this end, a variety of algorithms can be employed [9].Optimum performance is achieved with maximum likelihood detection, implemented for example based on sphere decoding [10]. Unfortunately, even the fastest known ASIC implementation of the sphere decoder [11] does not achieve sufficient throughput for the MIMO-OFDM system under consideration. We therefore implemented an ordered successive interference cancellation scheme (OSIC) realizing a reasonable tradeoff between silicon complexity and performance. As outlined below, the ordering scheme employed in our case differs from the one used in the V-BLAST scheme [1]. In summary, the MIMO detection unit (MDU) carries out three major steps as illustrated in Figure 6 and described next.

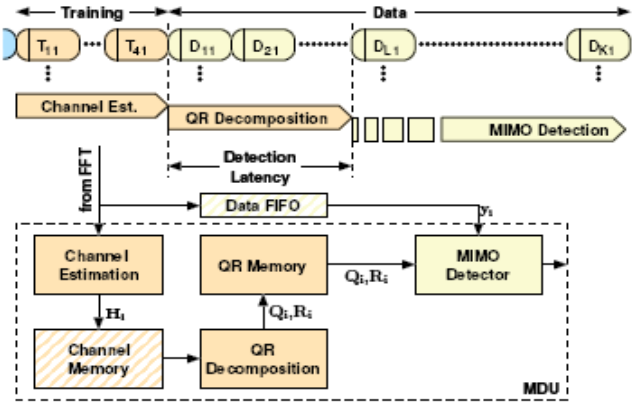

Figure 6: Timing diagram (top) and block diagram of MIMO detection (bottom).

Zero-forcing

The zero-forcing (ZF) algorithm is simply achieved by computing an inverse matrix G. The inverse formula is givenby

$$\begin{pmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{pmatrix} = \frac{1}{h_{11}h_{22} - h_{12}h_{21}} \begin{pmatrix} h_{22} & -h_{12} \\ -h_{21} & h_{11} \end{pmatrix},$$

where hij and gij are factors of the channel matrixH and the inverse matrix G, respectively.The QR decomposition is generally utilized in the inverse matrix calculation in orderto reduce a complexity. However, the complexity is not large as for a 2x2 MIMO configuration. Figure 6 shows the circuit structure of the ZF algorithm. This circuit operates a 8-stage pipeline including a complex divide operation. The total latency is 11 cycles including memory access. It can satisfy the above timing constraint for the guard interval of 64 cycles (12.5-ns clock period £ 64 cycles = 800 ns). The numbers of real and complexmultipliers are 8 and 11, respectively.

MMSE-VBLAST

The original V-BLAST is expressed as a recursive procedure [7]. In our architecture, the procedure is modified to introduce pipeline and concurrent pro- cessing. In the 2x2 MIMO, the modified procedure is described as follows:

G1 = H+ (2)
G2a = (H)2+ (3)
G2b = (H)1+ (4)
wa = (G1)1 (5)
wb = (G1)2 (6)
ya = waTr (7)
yb = wbTr (8)
ˆ αa = Q[¯ ya] (9)
ˆ αb = Q[¯ yb] (10)
´ ra = r − ˆ αa(H)1 (11)
´ rb = r − ˆ αb(H)2 (12)
ˆ ya = G2a´ ra (13)
ˆ yb = G2b´ rb (14)
k = argmin j k(G1)jk2 (16)

	Circuit Area (μm^2)	No. Logic Gates	Power TX (mW)	Power RX (mW)
System Control	5006	1668	0.11	0.11
Coder & Mapping	10143	3381	0.29	0.10
Timing Synchronization	80573	26858	1.44	5.26
FFT/IFFT & Equalizer	838144	279381	39.30	39.92
GI•PLCP Signals	13854	4618	0.34	0.13
SRAMs for Pre-FFT	285576	95192	10.06	9.64
SRAMs for Post-FFT	285576	95192	9.12	9.36
Soft Demapper	3315	1105	0.01	0.18
Viterbi Decoder	804624	268208	3.81	35.88
Total	**2326811**	**775603**	**64.48**	**100.58**

Table 1: Circuit performance of the SISO-OFDM Transceiver

	Circuit Area (μm^2)	No. Logic Gates	Power TX (mW)	Power RX (mW)
System Control	118353	39451	0.01	1.33
Coder & Mapping	20286	6762	0.49	0.10
Timing Synchronization	81967	27322	1.42	4.84
FFT/IFFT	1166008	388669	70.50	73.32
MIMO Detection	1114612	371537	5.05	26.38
GI•PLCP Signals	50928	16976	0.43	0.10
SRAMs for Pre-FFT	573584	191195	13.76	14.00
SRAMs for Post-FFT	573584	191195	14.02	14.06
Soft Demapper	6480	2160	0.02	0.35
Viterbi Decoder	1600206	533402	7.36	71.20
Total	**4256008**	**1418669**	**113.06**	**205.68**

Table 2: Circuit performance of the zero-forcing MIMO-OFDM Transceiver.

$$y = \begin{cases} (\bar{y}_a, \hat{y}_b)^T & \text{if k=1} \\ (\hat{y}_a, \bar{y}_b)^T & \text{otherwise} \end{cases},$$

where (H)j is the j-th column of H and + denotes an inverse matrix operation based on a MMSE criterion. The inverse matrices of G2a and G2b are precomputed before the MIMO detection at Eqs. (3) and (4). This pre-computation converts a recursive procedure into a one-time procedure. It prepares both candidates of (¹ya; ^yb) and (^ya; ¹yb) for optimal detection ordering. It depicts the modifed procedure in MMSE-V-BLAST algorithm, which is applied to the MIMO detection block. While the two candidates are calculated at Eqs. (5) to (14), the channel order information of k is simultaneously computed at Eq. (15). The channel estimation and the pre-processing Finish within a 13-cycle latency including memory accesses. The numbers of real and complex multipliers require 16 and 27, respectively.

IX. IMPLEMENTATION RESULTS

The layout of the MIMO-OFDM baseband signal processing ASIC described in this paper is shown in Figure 7. The area requirements of the different components described in Sections along with the area requirements in a corresponding SISO system are summarized in Table 3. Most of the SISO components have to be replicated in the MIMO case which results in a fourfold chip area increase.The area occupied by the I/FFT processor increases only by 50% (compared to the SISO case) which is due to the fact that only one FFT block is used in the MIMO case with the same butterfly architecture as in the SISO case. The 50% area increase is therefore due to an increase in memory requirements in the MIMO case.

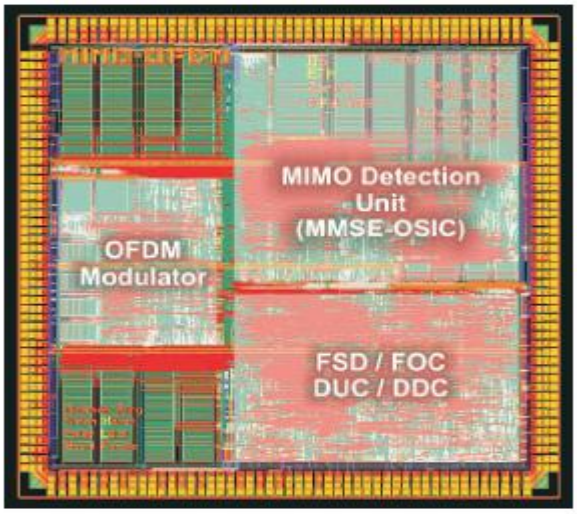

Figure 7: Layout of the MIMO-OFDM baseband signal processing ASIC manufactured in 0.25 µm 1P/5M 2.5V CMOS technology.

Component	Area	
	SISO	4 × 4 MIMO
DDC, DUC	0.5 mm^2	1.9 mm^2
AGC	0.1 mm^2	0.4 mm^2
FOE, FOC, FSD	0.3 mm^2	1.3 mm^2
Modulator, I/FFT	0.9 mm^2	1.4 mm^2
Frame buffers	-	3.3 mm^2
Ch. est. & Ch. mem.	<0.1 mm^2	1.12 mm^2
QR-decomposition	-	1.29 mm^2
QR-memory	-	1.23 mm^2
MIMO detector	-	0.9 mm^2
Total	1.9 mm^2	12.8 mm^2

Table 3: Chip area of baseband signal processing components in a 0.25 µm CMOS technology.

The size of the data FIFO buffer and the latency incurred by QR-preprocessing can be reduced by reducing the algorithmic complexity of the QR-decompositionHi = QiRi
(i = 1, ..., 64). Corresponding algorithms exploiting the correlation between the Hi have recently been proposed in [11]. Another viable option for memory reduction is sharing of the same memory for the Hi and the Qi matrices, which allows to save about half of the QR-memory. (These considerations also hold for other types of MIMO detectors like MMSE.)

X. FPGA VERIFICATION

The FPGA verification board used to verify circuit behavior of the OFDM transceivers and RF

modules. Figure 8 shows the block diagram of the FPGA board in the SISO-OFDM system. The FPGA board activates three chips of the transmitter, the receiver, and the Viterbi decoder, which is based on Xilinx Vertex II-Pro XC2VP70. We have addedan interpolator, a decimator, a random signal gener-ator, and bus interfaces to communicate with a PC.The interpolator and the decimator require 100-MHz

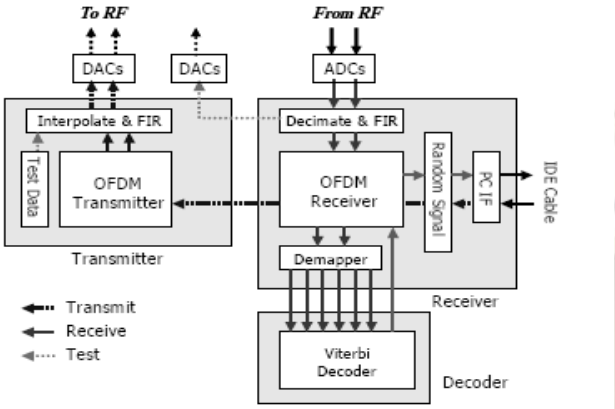

Figure 8: Block diagram of the FPGA board.

clock frequency and the other modules operate at itshalf clock speed. The current FPGA board enablesbaseband transmission via ADCs and DACs. BERand PER can be obtained from this baseband transmission.

XI. CONCLUSION

In the hardware architecture, the SISO-OFDM and the MIMO-OFDM transceivers have been designed by the policy of applying full-pipeline and concurrent processing. The zero-forcing and MMSE-V-BLAST techniques have been implemented to hardware as practical instances. The OFDM transceivers have been implemented to a 90-nm CMOS process and evaluated on circuit area and power dissipation. The FPGA board has been presented to verify circuit behaviors and execute baseband transmission. A 4 × 4 MIMO-OFDM WLAN baseband signal processing ASIC based on the IEEE 802.11a specifications has been presented. We observed that going from SISO to 4 × 4 MIMO the chip area increases by a factor of 6.5. Furthermore, the chip area occupied by the multi-antenna OFDM processing part is almost on par with the chip area corresponding to the MIMO detection unit. The main bottleneck was found to be the latency incurred by preprocessing the channel matrices for MIMO detection.

REFERENCES

[1] G. J. Foschini and M. J. Gans, "On limits of wireless communications in a fading environment using multiple antennas," *Wireless Personal Communications*, vol. 6, pp. 311–335, 1998.

[2] A. Paulraj, R. Nabar, and D. Gore, Introduction to Space-Time Wireless Communications, Cambridge Univ. Press, 2003.

[3] A. J. Paulraj, D. A. Gore, R. U. Nabar, and H. B¨olcskei, "*An overview of MIMO communications–A key to gigabit wireless,"* Proc. IEEE, vol. 92, pp. 198–218, 2004.

[4] IEEE 802.11a Standard, ISO/IEC 8802-11:1999/Amd 1:2000(E).

[5] S. Mehta et al., "An 802.11g WLAN SoC," in Proc. IEEE ISSCC, 2005, vol. 1, pp. 94–95.

[6] Changick Song, Inkyu Lee "*Maximum Achievable Diversity of Coded MIMO-OFDM Amplify-and- Forward Relaying Systems*", IEEE Transaction on Communications, vol. 10, pp. 2445 - 2450, July 2011

[7] L. J. Cimini, "*Analysis and simulation of a digital mobile channel using orthogonal frequency division multiplexing*", IEEE Transaction on Communications, Vol. 33, Issue 7, pp. 665–675, July 1985

[8] S. Alamouti, "*A simple transmit diversity technique for wireless communications*", IEEE Journal on Selected Areas of Communication, Vol. 16, pp. 1451–1458, Oct. 1998.

[9] H. B¨olcskei, D. Gesbert, C. Papadias, and A. J. vander Veen, Eds., Space-Time Wireless Systems: From Array Processing to MIMO Communications, Cambridge Univ. Press, 2005, to appear.

[10] E. Viterbo and J. Boutros, "*A universal lattice decoder for fading channels*," IEEE Trans. Inform. Theory, vol. 45, no. 5, pp. 1639–1642, July 1999.

[11] A. Burg, M. Borgmann, M. Wenk, M. Zellweger, W. Fichtner, and H. B¨olcskei, "*VLSI implementation of MIMO detection using the sphere decoder algorithm," IEEE J. Solid-State Circuits*, 2005, to appear

[12] D. Perels et al., "ASIC Implementation of a MIMO- OFDM Transceiver for 192 Mb/s WLANs," Euro. Solid- State Circuits Conf., Sept. 2005, pp. 215–18.

[13] D. Cescato, M. Borgmann, H. B¨olcskei, J. C. Hansen, and A. Burg, "Interpolation-based QR decomposition in MIMO-OFDM systems," in IEEE Workshop on Signal Processing Advances in Wireless Communications (SPAWC), New York, NY, 2005, to appear

[14] L. Zheng and D. N. C. Tse, "Diversity and Multiplexing: A Fundamental Trade-off in Multiple Antenna Chan- nels," IEEE Trans. Info. Theory, vol. 49, no. 5, May 2003, pp. 1073–96.