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# Development of FPGA for Custom Waveform Generator Based on Direct Digital Synthesizer

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## ABSTRACT

**In this paper an efficient approach is present to design custom waveform generator based on DDS with low phase noise and high switching speed for military communication applications. It can generate custom signals with different modulations whose amplitude, frequency or phase are controlled by the description words given from an external computer. DDS is a frequency synthesizer which can generate arbitrary waveforms from a single, fixed frequency reference clock. In order to implement such custom waveform generator along with DDS we need FPGA. FPGA are used to realize DDS to meet different demand of the user such as high switching speeds. Then, the AD9858 used as the DDS core with compression ROM is compiled using Xilinx XC2V250 FPGA by VHDL language. The performances such as integration, expansibility are very much improved. We need design a Graphical User Interface (GUI), which allows simple control of the hardware.**

*Keywords* - **DDFS, FPGA, GUI, PIC, AD9858**

## I. INTRODUCTION

Generally in any equipment, it is important to readily control and produce accurate waveforms of different frequencies. In Military Communication Attack application, Bio-medical and industrial applications are require highly agile, very low phase noise and high resolution synthesizers for communications. The digital synthesizing method synthesizes the waveform data in digital processing and the data is converted to analog signal with a DAC. This is the method called DDS. DDS devices will offer faster switching between output frequencies and fine resolution in frequencies. As the technology advance in design and technology, DDS devices consume less power and very compact compared to the analog method, and can be fully controlled by software.

AD9858 DDS chip will generate an analog signal usually a sine wave, but we can generate other signals also. Here we are using AD9858 DDS chip. It will generate signal with frequencies from 20-500MHz (based on 1GHz clock). Multichannel waveform generator can be designed using multiplied AD9858 DDS chips and PC controller along with FPGA to control those DDS chips. Here we are designing 3 channel waveform generator using 3 DDS chips using FPGA during Fixed Frequency mode, Amplitude Modulated mode, Frequency Modulated mode, Frequency Chirp mode, Time Division Multiplexed mode, Frequency Division Multiplexed mode and Binary Frequency Shift Keying mode.

In Fixed Frequency mode of operation, the FPGA receives frequency command from the PC based external controller in BCD format, computes the 32 bit frequency tuning word and programs it into the DDFS.

In the Amplitude Modulated mode of operation, the FPGA receives the message frequency command from the external controller in BCD format. It triggers the external ADC at a rate of 1MHz and reads the ADC output to calculate the FTW and program the DDFS instantaneously.

In the Frequency Modulated mode of operation, the FPGA receives the center frequency and deviation commands from the external controller in BCD format. It computes the FTW and programs it into the DDFS. It triggers the external ADC at a rate of 1MHz and reads the ADC output to recalculate the FTW and reprogram the DDFS instantaneously.

In the Frequency Chirp mode of operation, the FPGA receives the Start Frequency, Stop Frequency and Chirp Step commands from the external controller. It computes the frequency tuning words and Ramp Rate word and programs it into the DDFS. It retriggers the DDFS at regular intervals to return the DDFS to the Start Frequency.

In the Time Division Multiplexed mode of operation, the FPGA receives up to 4 frequencies from the external controller. It computes the frequency tuning words and programs them into the DDFS. At regular intervals the FPGA changes the profile selection of the DDFS in order to switch between the frequencies.

In the Frequency Division Multiplexed mode of operation, the FPGA receives frequencies from the external controller. It computes the frequency tuning words and programs them into the

DDFS. In specific frequency range the FPGA generate frequencies.

In the Binary Frequency Shift Keying mode of operation, the FPGA receives two frequencies from external controller. The FPGA calculate the two FTW words. FPGA device accepts the modulating signal and selects the appropriate tuning word and program into the DDFS.

## II. DDS TECHNOLOGY

In the simplest case a Direct Digital Synthesis is constructed by a ROM with many samples of sine wave stored in it (sine look-up table, LUT) and it was introduced in[2]-[3]. Figure.1 shows the block diagram of a DDS system. The DDS produces sinusoidal at a given frequency by digital integration of higher clock frequency. The phase Accumulator stage accepts the so called Frequency Tuning Word (FTW) which determines the phase step. Once set, this digital word determines the sine wave frequency to be produced. The phase accumulator then continuously produces in the output proper binary words indicating the instantaneous phase to the table look-up function. In other words the phase accumulator is used to "calculate" the successive addresses of the sine look-up table which generates a digital sine wave output. In this way the samples are swept in a controlled manner i.e. with a step depending on the Frequency Tuning Word. The DDS translates the resulting phase to a sinusoidal waveform via the look-up table, and converts the digital representation of converter followed by a low pass filter (LPF).

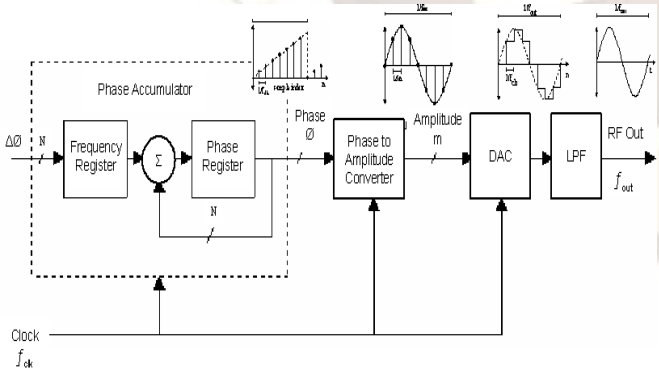



Figure 1: Block diagram of DDS system

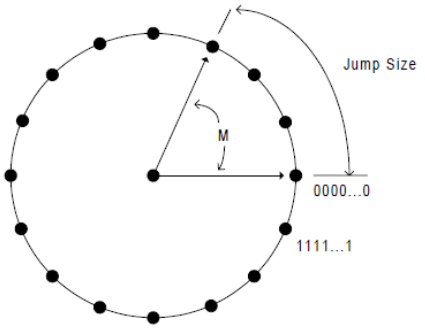
Where N denotes the number of bits used to represent the tuning word. Generally for AD9858 Frequency Tuning Word (FTW) is 32 bit.

The output frequency $f_{out} = M \times f_{clk} / 2^N$

and resolution $f_{clk}/2^n$

where

$f_{out}$= output frequency of DDS
M= frequency tuning word
$f_{clk}$= internal clock frequency
N=length of phase accumulator in bits




| N | NUMBER OF POINTS |
|---|---|
| 8 | 256 |
| 12 | 4096 |
| 16 | 65535 |
| 20 | 1048576 |
| 24 | 16777216 |
| 28 | 268435456 |
| 32 | 4294967296 |
| 48 | 281474976710656 |

Figure 2: Digital Phase Wheel

For understanding the basic function consider sine wave oscillations as a vector rotating around a phase circle. The number of discrete points can be determined by the resolution of phase accumulator. Each point on the phase circle corresponds to equivalent point on cycle of sine waveform. As the vector rotates along the wheel, corresponding output sine wave will be generated. As vector completes one revolution at a constant speed around the phase wheel it completes one cycle of output sine wave. The phase accumulator will provide the equivalent of the vector's linear rotation around the phase wheel. Each content of the phase accumulator represent the corresponding point on the cycle of the output sine wave. The number of phase points on the wheel are determined by the resolution N of phase accumulator. As the output of the phase accumulator is linear we cannot directly generate any wave expect ramp. So, we use phase-to-amplitude lookup table to convert output value of phase accumulator to sine wave amplitude information and then it is applied to D/A converter. The output frequency and length of the accumulator are related by the equation.

Here we are using AD9858 DDS chip which can generate waveforms ranging from 20-500 MHz, whose clock frequency is 1 GHz with 14 bit DAC.

## III. SYSTEM ARCHITECTURE

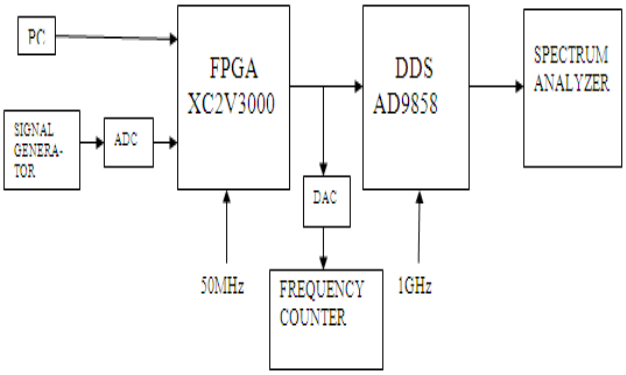



Figure.3 Implementation of frequency synthesizer using FPGA

### Graphical User Interface (GUI)

In order to generate the signals we need to store the corresponding hexadecimal data into the internal registers of DDS. So we need GUI to convert the corresponding amplitude, frequency and phase description into corresponding hexadecimal data using the formulas specified in the AD9858 datasheet and it has to send the hexadecimal data through serial port from the pc.

### PIC Micro Controller

As we are sending data from pc using GUI through serial port. We have to receive the data send by the pc so we are using PIC microcontroller. PIC micro controller has to receive the data from the serial port and it has to send the data to the FPGA.

### Field Programmable Gate Array (FPGA)

We have to send the data to the DDS based on some control signals and we have to provide some clock signals to the DDS so we are using FPGA. PIC will send the data received from the pc to the FPGA using SPI. FPGA will provide clock signal to the DDS and it has to receive the data from PIC and based on the control signals it has to send the data to the DDS

### 3 Channel Board

Our requirement is to generate an identical signals whose phase, amplitude, frequency should be in our control. So in order to generate identical signals first we need to synchronize DDS chips for synchronization one of the DDS chips has to generate SYNC_CLK and CY2308 will distribute that SYNC_CLK to all the DDS chips. One which generates the SYNC_CLK behaves like master remaining as slaves, thus the DDS chips are synchronized and they will operate on the same internal clock so they will produce identical signals. SYNC_CLK will be generated from the internal clock only by using frequency divider. CY2308 will distribute the clock signal generated by the FPGA to all the DDS chips. By using these devices the custom waveform generator is designed. Now in the GUI we need to enter the amplitude, phase and frequency and we need set the mode in which the AD9858 DDS chip has to operate generally we will operate the DDS chip in single tone mode in which DDS will generate the signal based on the information provided from the serial port. After setting all the controls we will send the data to be stored in the registers through serial port. FPGA will receive the data and then it will send the data to the DDS chips based on some control signals along with that it need to provide clock signals to DDS devices.

Figure 4 shows GUI module developed on Microsoft Visual C++ for the evaluation of the Frequency Synthesizer.

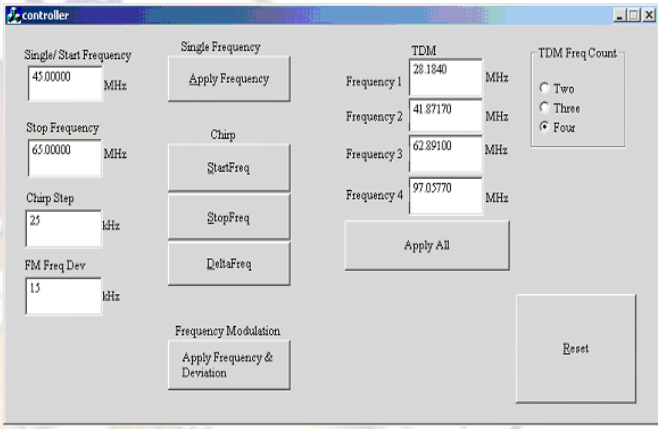



Figure.4 External Controller Software for the Evaluation of the Synthesizer

## IV. THE DESIGN APPROACH

According to the specifications of this project, the range of frequencies that the Frequency Synthesizer is expected to generate is 20–500MHz at a step size of 10Hz. The CMOS Integrated Circuit AD9858 of Analog Devices is a Direct Digital Frequency Synthesizer having 32 bit Frequency Tuning Word operating on 1GHz clock is capable of meeting these specifications. Also the AD9858 is capable of generating Chirp over a band of frequencies at the specified frequency steps. Having four profiles for frequency selection, the AD9858 is ideally suitable for the specification of up to four Time Division Multiplexed signals. AD9858 is controllable through a set of 20 command lines at a rate of 100MHz max. This meets the maximum data input rate required by the specifications for TDM and Chirp Signal generation. But since no Personal Computer with a Commercial Operating System can generate data at this high speed, a Field Programmable Gate Array (FPGA) capable of operating on 50MHz clock is required to control the AD9858.

XC2V250-5FG256I is chosen to control the DDFS. This FPGA is an Industrial Grade 250k gate FPGA of Xilinx Corporation that meets the

requirements mentioned above. The specifications of this IC are featured in the reference along with the remaining components used in this project.

## V. RESULTS

Figure 5 presents the fixed frequency and phase noise performance of the synthesizer. The phase noise achieved is -112dBc/Hz at 1 kHz against the specification of –110dBc/Hz. Figures 6 show the Frequency Synthesizer operating in Amplitude Modulation mode with 1 kHz deviation at center frequency of 135MHz. Figures 7 show the Frequency Synthesizer operating in Frequency Modulation mode with deviations of 15 kHz from the center frequency of 20MHz. The Chirp performance of the Synthesizer is shown in figure 8. Between 300 MHz and 360 MHz the output spectrum in the chirp mode of operation is very flat over the entire frequency range of operation. Figure 9 shows the TDM performance of the Synthesizer with 4 Frequencies switched at the minimum switching time. Due to the rapid switching, all the 4 frequencies of the Synthesizer appear to exist simultaneously as displayed in the spectrum. Figure 10 shows the FDM performance of the Synthesizer. All the frequencies of the Synthesizer appear to exist simultaneously as displayed in the spectrum. Figure 11 shows the BFSK performance of the Synthesizer.

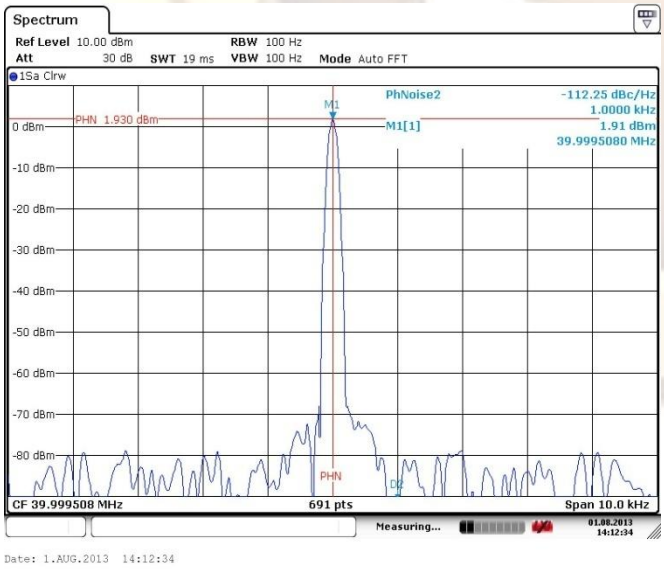



Figure 5: Fixed Frequency and Phase Noise performance of the Synthesizer

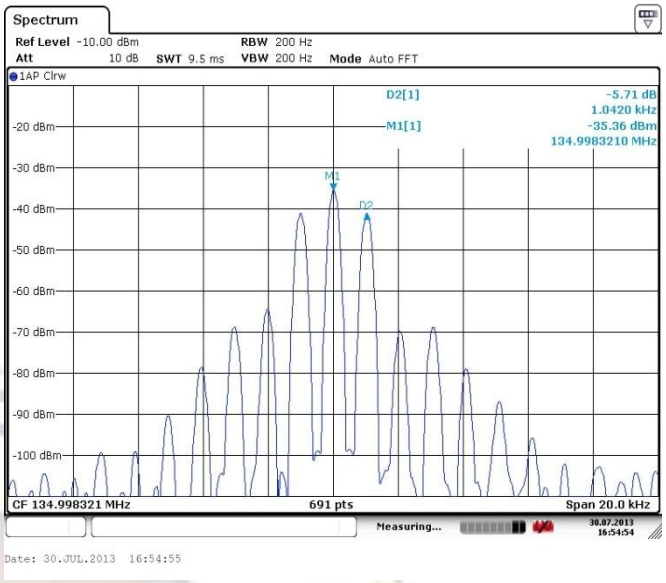



Figure 6: Amplitude modulation performance of the Synthesizer

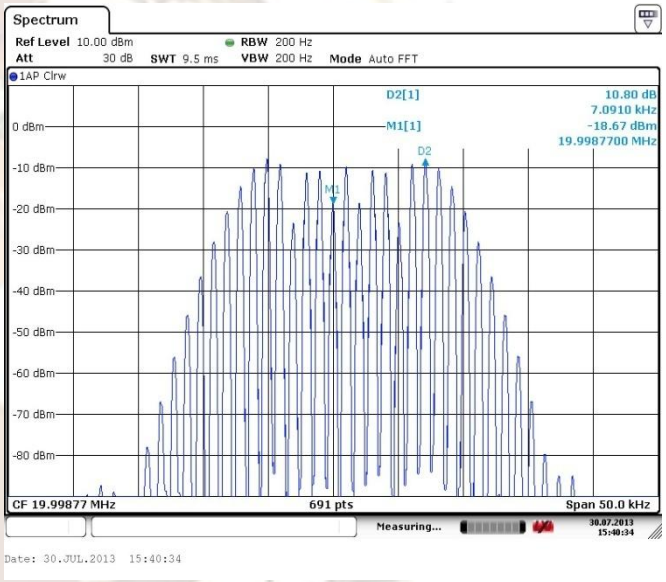



Figure 7: frequency modulation performance of the Synthesizer

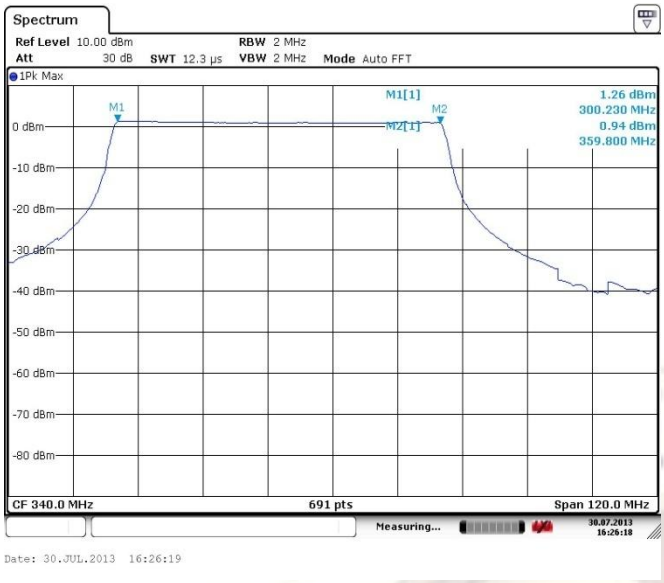



Figure 8: chirp mode performance of the Synthesizer

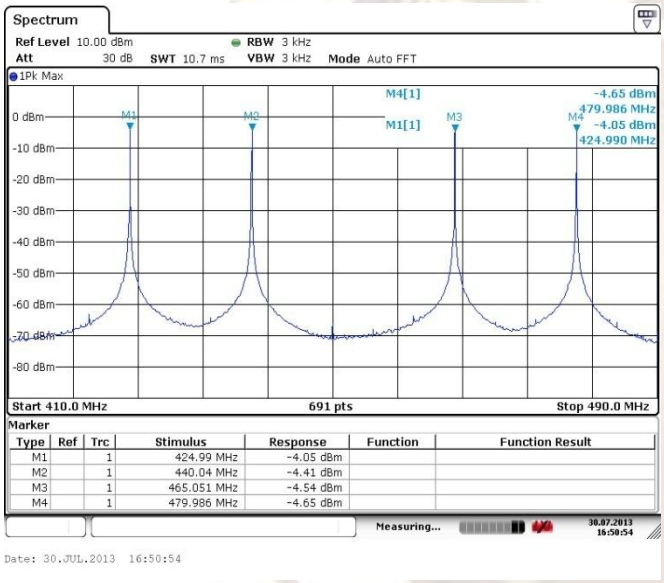



Figure 9: TDM performance of the Synthesizer with 4 Frequencies

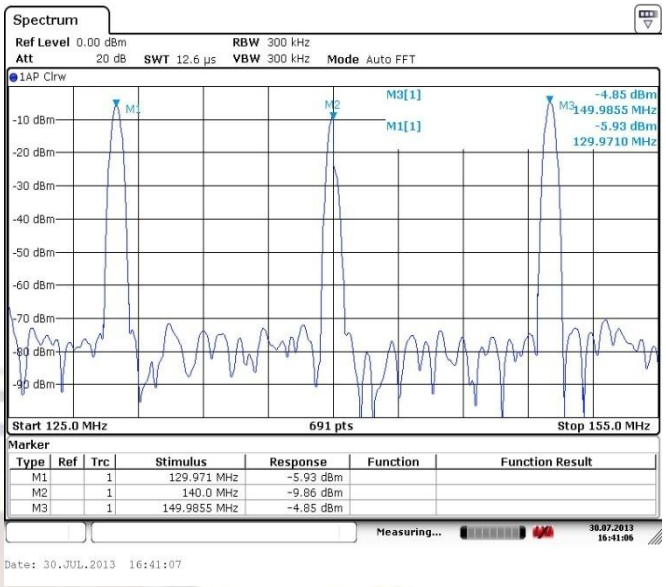



Figure .10 FDM performance of the Synthesizer

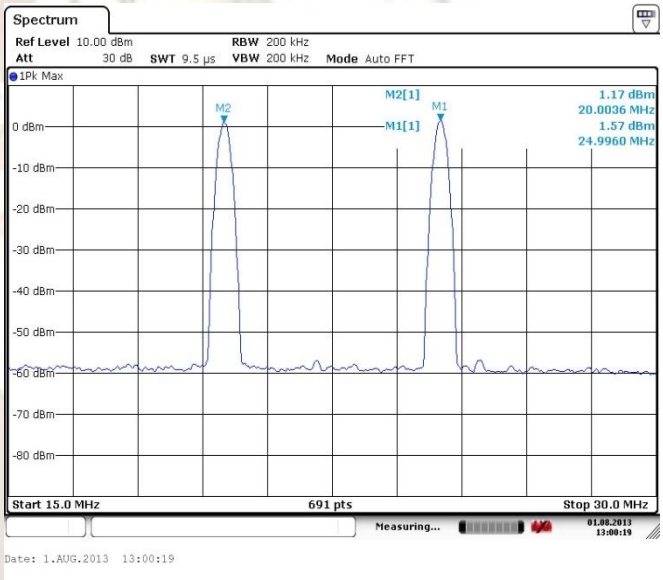



Figure.11 BFSK performance of the Synthesizer

## VI. DEVICE UTILIZATION SUMMARY

Selected Device : 2v250fg256-5
Number of Slices : 1264 out of 1536 (82%)
Number of Slice Flip Flops: 536 out of 3072 (17%)
Number of 4 input LUT : 2238 out of 3072 (72%)
Number of bonded IOBs : 52 out of 172 (30%)
Number of GCLKs : 3 out of 16 (18%)

## VII. CONCLUSION

According to the results, we can conclude that the custom waveform generator based on DDFS achieved low phase noise and high switching speed for military communication applications. In this

paper, custom waveform generator architecture which is designed using AD9858 DDS chips, PIC microcontroller and FPGA.

**ACKNOWLEDGEMENTS**

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