ULTRA-LOW POWER SUBTHRESHOLD CMOS INVERTER AT 90nm CMOS TECHNOLOGY

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Abstract
In the medium power consumption design region, alot of efforts have been made. However, much research has not been done at the ultra-low power with acceptable performance and high performance design with power. This paper focuses on design techniques for ultra-low power dissipation where performance is of secondary importance. One way to achieve this goal is by running the CMOS inverter circuit in sub threshold mode.[2,3]The incentive of operating the circuit in sub threshold mode is to be able to exploit the sub threshold leakage current as the operating current for the circuit. The sub threshold current is found to be exponentially related to the gate voltage. Thus, this exponential relationship not only gives an exponential reduction in power consumption, but also an exponential increase in delay. The simulation results show that the reduction in power outweighs the increase in delay, and thus, giving the overall reduction in energy consumption per switching.

Keywords -Sub threshold Power, CMOS Inverter

I. Introduction
Due to the growth in scale of integration, more and more signal processing systems need to be implemented on a single VLSI chip. Also the power consumption have become a major concern for this respect. The need for low- power CMOS inverter raised from two main forces:

- Firstly large current has to be delivered and the heat due to large power consumption must be removed by proper cooling techniques.
- Second, battery life in portable electronic devices is limited. Low-power design directly leads to prolonged operation time in these portable devices. Also, with reduction in sizes, energy efficiency has become a critical aspect of designing digital circuits.

In sub threshold circuits, the supply voltage is reduced well below the threshold voltage of a transistor.[4] Ultra low-power CMOS inverters are classified as the sub threshold circuits in which exponential reduction in power with respect to the supply voltage takes place.

In the low frequency applications, circuits operating in the sub threshold region are the ideal choice. With growing needs for low-power consumption, low energy circuits have become more attractive. [3]The characteristics of semiconductor behaviour in weak inversion are different than those in strong inversion, resulting in different sizing and ratio optimizations. This short paper briefly presents the concept of subthreshold operation and comparisons of PDP at different voltages at different temperatures is shown through simulations in advanced CMOS processes, such as 90nm.

II. CMOS Inverter
1. Conventional CMOS inverter
The inverter is truly very important for all the digital designs. The electrical behaviour of complex circuits can be almost completely derived by deriving the results from inverters. Figure 1 shows the circuit diagram of a static CMOS inverter. [1]

When V_{in} is high and equal to VDD, the NMOS transistor is on, while the PMOS is off. A direct path exists between V_{out} and the ground node, resulting in a steady-state value of 0 V. On the other hand, when the input voltage is low (0 V), NMOS and PMOS transistors are off and on, respectively. A path exists between V_{dd} and V_{out}, yielding a high output voltage.
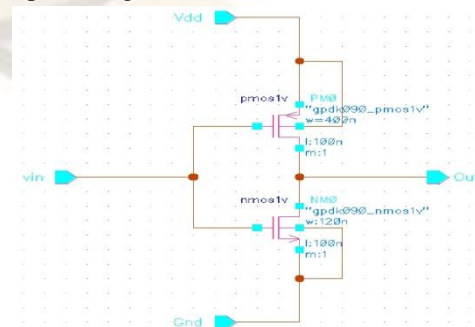

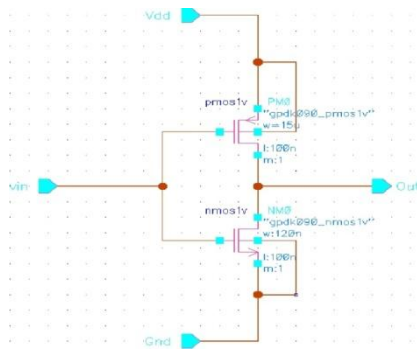Figure 1 Conventional CMOS Inverter [1]

Figure 2 Sub threshold CMOS Inverter [1]

2. Sub threshold CMOS Logic

Sub threshold CMOS logic operates with the power supply V_{dd} less than the transistors' threshold voltage Vt. This is done to ensure that all the transistors are indeed operating in the sub threshold region. In sub threshold region, for $V_{ds} > 3kT/q$, Ids becomes independent of V_{ds} for all practical purposes. The 3kT/q drop (about 78mV at T=300K) is practically negligible compared to the V_t drop in the normal strong inversion region.[2]

a) Power Consumption

Figure3 shows the power consumption vs. frequency for various power supply values.

From the figure, we notice that:

- At higher frequency, the power consumption is linearly dependent with the operating frequency.
- At same operating frequency, sub threshold CMOS inverter consumes less power than the strong inversion circuits.
- At lower frequency, the power consumption becomes independent of operating frequency as the static power component takes over.
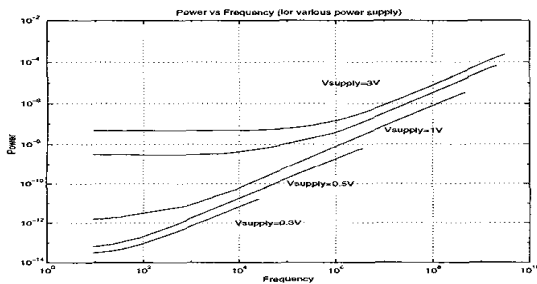

Figure 3 Power Consumption Vs Frequency [2]

3. Reduction of power [3]

Till now, the power consumption has not been of great concern because of the availability of large packages and other cooling techniques having the capability of dissipating the generated heat. However,

continuously increasing density as well as the size of the chips and systems might cause to difficulty in providing adequate cooling and hence, might either add significant cost to the system or provide a limit on the amount of the functionality that can be provided.

Another factor that fuels the need for low-power chips is the increased market demand for portable consumer electronics powered by batteries. For these high performance portable digital systems, running on batteries such as-laptops, cellular phones and personal digital assistants (PDAs), low-power consumption is a prime concern because it directly affects the performance by having effects on battery longevity.

Hence, low-power VLSI design has assumed great importance as an active and rapidly developing field.[8] Due to their extreme low-power consumption, sub threshold design approaches are appealing for a widening class of applications which demand low-power consumption and can tolerate larger circuit delays.

III. Design simulation and simulation results

- **Calculation OF V_T For NMOS AND PMOS**

The output characteristics of both NMOS and PMOS. From the observation of both the characteristics, and using the values, the process parameters can be calculated as shown.[1][2]

Table 1 Current at different operating regions in NMOS

S.No.	V_{DS} (V)	I_D (µA)	$V_{GS(V)}$
1	0.5	69.98	1.5
2	0.1	40.64	1.2
3	0.6	12.93	0.5
4	0.4	10.51	0.5
5	0.4	0.7114	0.3

Table 2 Current at different operating regions in PMOS

S.No.	V_{DS} (V)	I_D (µA)	$V_{GS(V)}$
1	0.8	29.63	1.1
2	0.3	17.16	1.2
3	0.6	2.899	0.5
4	0.4	2.343	0.5
5	0.2	0..477	0.4

Table 3 Parameters in 90 nm Technology

	V_{th} (V)	k(μA/V^2)	λ (V^{-1})	V_{sat} (V)
NMOS	0.13	74.5	3.71	0.35
PMOS	-0.16	-21.4	-3.9	-0.77

Table 4 Comparison of Delay, Avg. Power and PDP at different voltages at 27degrees

V_{dd}(V)	Delay(t_p) (10^{-9})	Average Power (P_a)(10^{-9})	PDP($t_{p*}P_a$)
0.1	71.57	0.402	28.77
0.12	44.79	0.582	26.10
0.13	35.67	0.684	24.41
0.14	28.14	0.795	22.39
0.15	22.40	0.914	20.48
0.16	17.85	1.039	18.562
1	0.076	39.58	3.042

Technology used

In this research paper simulations are to be performed in CADENCE design tool and the schematic diagrams are drawn in VIRTUOSO schematic editor using 90nm technology file.

IV.Conclusion & self analysis

We examined characteristics of CMOS inverter operating in sub threshold region as a mean to achieve ultra-low power in this paper. The operation of CMOS Inverter in sub threshold region was simulated and comparison of Delays, Average Power and PDP are tabulated for 90 nm Technology in Cadence. From this the delay of CMOS Inverter is more in sub threshold region and power consumption is less compared to strong inversion region. The width of PMOS is varied up to 15u for an inverter to be operated in sub threshold region. By observing the power delay component operated in sub threshold region, supply voltage of 0.12V is preferable for sub threshold operation.

The sub threshold logic can be easily implemented and derived from traditional existing circuits by lowering the supply voltage to be less than Vt. A number of advantages in sub threshold operation includes improved gain, noise margin, and tolerant to higher stack of series transistors while being more energy efficient than standard CMOS at low frequency of operation. However, due to its slow performance, sub threshold circuit is limited to only certain applications where ultra-low power is the main requirement, and performance is of secondary importance.

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