Dual material gate-all-around Fully Depleted SOI MOSFET with Strained Si/Ge Channel

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ABSTRACT

After a lot of efforts to scale down the devices, now the scaling limits of device have reached i.e. it's not possible to scale down the CMOS further. For further scaling of device we need to change the materials used for the gate and channel. In this paper different structures suggested by different authors are covered along with their benefits and limitations. A structure based on the Fully Depleted SOI Gate All around (FD SOI GAA) MOSFET with strained Si Channel has been suggested to overcome the scaling limits along with the QME consideration in modeling.

Keywords-CMOS, FD, Gate-All-Around, Quantum Mechanical Effect, Scaling Effects, SOI, Strained Si.

I. INTRODUCTION

CMOS technology has contributed significantly for the development of almost all the countries. This is due to the vast applications used in every sphere and industry. With the fast pace of technological changes, consumer electronic device requirements are also growing. Hence, the need for large scale, complex integrated circuits increases at the same pace. With the scaling of the device or with the increase in the device count in an IC, area decreases, but power dissipation and the speed becomes most important issues. Keeping in mind all these issues, now the device dimensions have reached a limit that cannot be further scaled down. With further scaling of the device, the effects like Short-Channel-Effects (SCE), Quantum Mechanical Effects (QME) becomes dominating. So while designing, the most fundamental challenge is the trade-off between short-channel effects and the impact of Source-drain resistance (due to change in channel length).

With the scaling, the devices trends from microelectronics to nanoelectronics regime following the moore's law. This movement starts with the bulk CMOS transistor followed by SOI CMOS with different gate structures like single gate, double gate, trigate and then gate all around, with different gate materials like single material, dual material. In a conventional, bulk-silicon microcircuit, the active elements are isolated from the silicon body with a depletion layer of a p-n junction. The leakage current of this p-n junction exponentially increases with temperature and limit the operation of microcircuits at high temperatures. Bulk CMOS transistor as discussed by Kang [1] aces a very serious problem of Latch-up due to the formation of parasitic bipolar transistors. As discussed by Ulicki [2], Silicon-on-insulator (SOI) offers superior CMOS devices with higher speed, higher density, excellent radiation hardness and reduced second order effects for submicron VLSI applications. Dual-Material Gate (DMG) structure offers an alternative way of simultaneous SCE suppression and improved device performance by careful control of the material work function and length of the laterally amalgamated gate materials explained by Chaudhary [3]. With the change in the no of gates i.e. from single gate to multigate the control of the gate voltage on the channel surface potential increases. By combining the benefits of Dual material with the dual gate, Kushwaha [4] concluded that the DMDG SOI MOSFET is the option that can limit the SCE to a very large extend. Choudhary [5] suggested the stressed Si structure for improving the carrier mobility.

In this review paper, there are four sections. Section I includes the introduction. In Section 2, various problems, encountered during scaling of MOSFET, are explained. In Section 3, various structures, suggested of different authors to overcome those problems, are explained. Section 4 includes the proposed work on the basis of section III suggestions.

II. SCALING EFFECTS

In 1965, Gordon Moore wrote a paper entitled "Cramming more Components onto Integrated Circuits" where he first proposed that transistor density on chips would grow exponentially [6]. Following this law, various MOSFET models designed. This law was followed for more than forty-five years. But now with further scaling of the devices, the various problems are encountered Quantum Tunneling of carriers, Short Channel Effects Like Edge potential effects, Punchthrough, Drain Induced Barrier Lowering (DIBL), Hot Carrier Effect and subthreshold Swing. So, there is a large need of considering the new structures with new materials that can be proven suitable to follow the law with suppressed problems.

2.1. Quantum Mechanical Effect

With the scaling of the device, the model used to describe the behavior of MOS faces difficulties to achieve the accurate description. As more complicated phenomena starts arising out of down-

scaling of MOSFET, we need to consider those entire phenomenon before the modeling of MOSFET. One such phenomenon is the failure of classical physics. At this classical physics limit, quantum mechanics need to be taken into account. The major issue is the increase in quantum effects near the Si/SiO2 interface that affects the charge carrier distribution in the channel inversion layer. The thermal wavelength of an electron is given by $\pi h\sqrt{2/m\ K_B T}$, which is about 8nm at room temperature when m is the free electron mass. This wavelength is very smaller than the gate length in the foreseen future described by ITRS [7], oxide thickness, and channel depth for current devices. So the quantum plays a very important role in modeling the MOSFET that can be used as a simulation model.

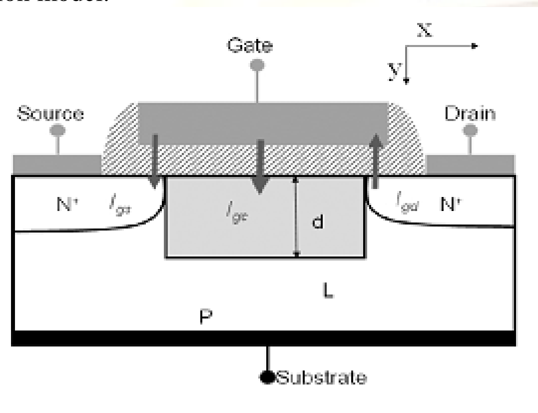

Fig.1 Tunneling currents Igs, Igd, Igc of MOSFET by WANG [8]

In case of ultra thin gate oxide, the electric field will be very high, which in turn pushes the charge carriers through the channel to account for the gate direct tunneling current, demonstrated by Wang [8] shown in the fig.1. Other Quantum mechanical effects are energy quantization, displacement of energy charge density of the bulk, Quantum mechanical tunneling from source to drain, threshold voltage and drain saturation voltage shift described by Choudhary & ROY [9] and Abebe [10]. Hence to best describe the characteristics of a device the model approach should include the QME.

2.2. Short Channel Effects

2.2.1 End effects and channel length modulation

The voltage applied on the gate, drain and the source induces the depletion region in the body. Hence there are three depletion regions i.e. under the gate which is balanced by gate voltage and other two regions are balanced by the source and drain voltages as shown in the fig.2 below. But as the channel length decreases then the effect of drain to source voltage as well as the gate voltage affects the depletion region under the gate. And the control of gate starts decreasing over the effect introduced under the gate and hence the operation of MOSFET gets disturbed. One more factor i.e. drain voltage also affects the channel length. When the effect of the drain voltage is more as compared to the gate voltage, then channel length modulates and the transistor starts conducting a constant value current i.e. saturation region current. This effect is more dominating in case of short channel.

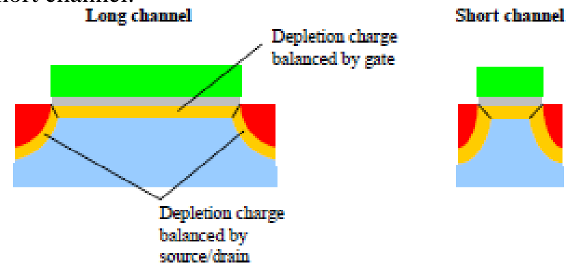

Fig.2 Depletion charge region in long channel (left) and Short channel (right)

2.2.2 DIBL-Drain Induced Barrier Lowering

Due to the reduction of gate control over the drain current, DIBL effect comes into the picture. In short channel devices, drain biased depletion region has the effect of lowering the barrier potential at the source end and hence there is a current flow even when the device is OFF. This effect is also more dominating in Short channel devices and can be alleviated by increasing the doping concentration of the channel region.

2.2.3 Punchthrough

Punchthrough is an extreme version of the DIBL and occurs when due to the increase in drain voltage the depletion region of source and drain overlaps. When the depletion region of drain and source overlaps, then a substantial current flows through the channel, even with no bias at the gate terminal. Increasing the doping of channel region can alleviate this problem.

As discussed, the solution to overcome this problem of SCE is to increase the doping level in the channel region. But with the increase of doping level in the channel region, the scattering at the ionized impurities also increases and the elevated vertical electrical field due to the impurities also increases which in turn degrade the device performance. Also suggested by Subrahmanyam & Kumar [11] Vertical gate structure can be used to mitigate the SCEs.

III. MOSFET STRUCTURES

Different authors suggested different structures, from time to time, with various improvements. Some of the models using planar technology are:

3.1. Structure with different Channel doping: Partially Depleted, Fully Depleted MOSFET.

3.2. Structure with different Substrate: Bulk Si MOSFET, SOI MOSFET.

3.3. Structure with different gate structures i.e. single gate, Double gate, Gate-all-Around.

3.4. Structure with different gate materials: Single material, dual material Gate.

3.5. Structure with strained and unstrained Channel: Strained Si Channel, Unstrained Si Channel MOSFET.

3.1. Partially Depleted Vs Fully Depleted MOSFET

In Partially Depleted MOSFET, a part of the body region remains undepleted while in Fully Depleted MOSFET; the depletion region extends in the whole body. The various Characteristics of the two models are as follows:

3.1.1. Kink in the drain current

In PD, the current kink is observed at a particular drain voltage due to the electron-hole pair generated by impact-ionization. In FD, there is lower potential barrier for the minority carriers as whole of the body is depleted of carriers. So there is no accumulation of holes in the body region and consequent kink in the drain characteristics.

3.1.2. Floating Body Effect

PD devices are significantly sensitive to dynamic body effect due to the presence of different doping structures available in the body and require the body to be connected to a constant potential. FD devices are unaffected by the dynamic body effects and are more stable.

Floating body PD SOI MOSFETs biased above the kink voltage have a drain current higher than tied body devices, but dependent on switching frequency. Perron et Al. [12] showed the results that in MHz range the on current increases, but the leakage current in Off-state also increases.

3.1.3. Parasitic bipolar effects

Parasitic bipolar transitors are formed in the MOSFET where Source, body and drain act as emitter, base and collector respectively. As the body is more depleted in FD devices, parasitic transistor is more effective in FD devices. These parasitic transistor leads to the latch-up problem.

3.2. Bulk Si Vs SOI MOSFET

The SOI employs a thin layer of Si isolated from the Si substrate by a thick layer of silicon oxide. Insulator layer provides dielectrically isolation and reduces various circuit parasitic capacitances and hence reduces the latch-up problem and also increases the speed of the device.

The SOI layer also provides some protection against the radiation hardness, as the electron-hole pair generated in the SI substrate due to the radiations cannot affect the channel. But in case of Bulk Si, as there is no isolation between the Si substrate and the channel, so the electron-hole pair generated affects the channel and ultimately the device performance is degraded. Also the Short-channel-effects are reduced to a very large extend in SOI MOSFETS due to the presence of thin Si film.

Fig.3 shows the performance of SOI MOSFETs. The low resistivity substrate that is used in bulk silicon CMOS processes limits the integration of high-quality passive components and gives rise to substrate coupling issues.

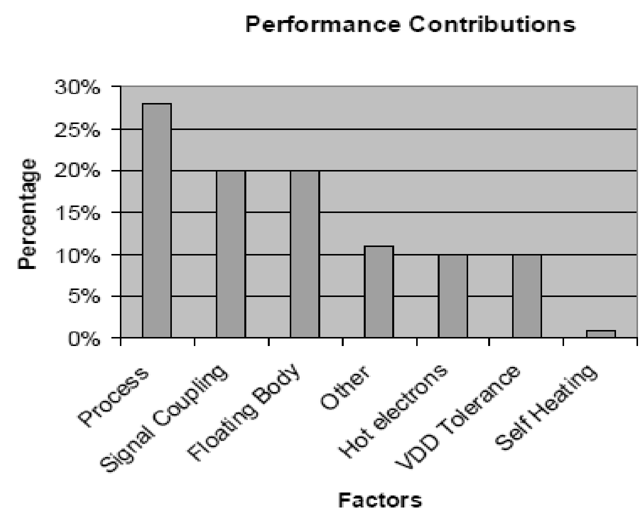

Fig.3 Performance improved in SOI MOSFETS

Tinella et al. [13] explained that the HRSOI (high resistive SOI) improves the RF circuit performance and reduces the substrate coupling issues.

3.3. Single Gate Vs Multigate

Gate terminal is the input terminal whose potential creates an effect in the channel to control the flow of current inside the channel. Colinge [14] demonstrated the reasons for evolving from single gate to multi-gate structures. The fig.4 shows the Source and drain terminals, which are connected by a channel. L is the length of the channel and E is the electric field induced in the channel due to the gate voltage. This Electric field has different components along different axes.

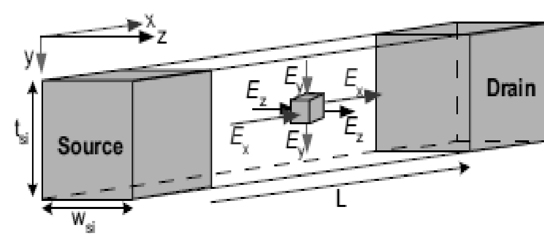

Fig.4 Electric field lines from source to drain

When there are two gates as shown in fig.5 (middle), then there are voltages from two sides gate to control the current flow in the channel i.e. much better control over the charge flow in the channel.

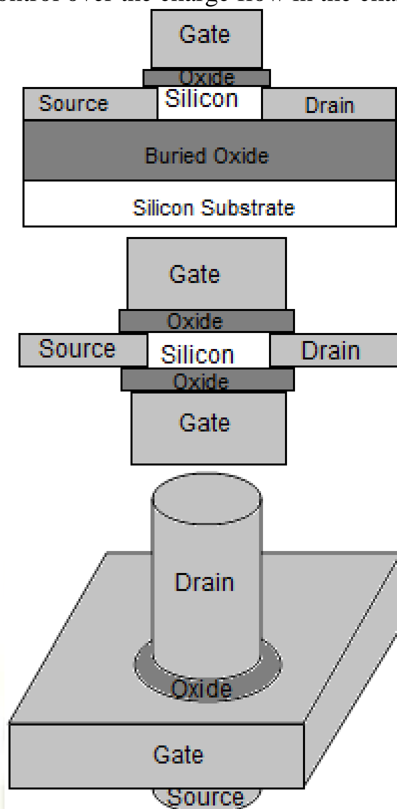

Fig.5 MOSFET with single gate (top), double gate (middle) and gate all-arround (bottom)

So in case of double gate, when the channel is even shortened, the flow of current can be better controlled in comparison to the single gate. Similarly in the case of Gate-all –around, the best control over the channel in comparison to double gate and tri-gate. The relation of the Electrostatic control effect with no of gates was best described by Colinge [15] in the equation form as:

$$\text{Electrostatic Control } \alpha \sqrt{{n\,\varepsilon_{ox}}/{\varepsilon_{Si}\, t_{Si} t_{ox}}}$$

Where n is the no of gates.
Jingbin et al. [16] explained that the explosive growth of power consumption and sensitivity to size variations limits the single-gate scalability below 6 nm gate length. Jimenez [17] explained the use of benefits of GAA MOSFET in various applications i.e. Nanowire.

3.4. Single Material Vs Dual Material Gate

Proposed by Long et al. [18] dual material gate MOSFET induces the step potential at the interface between the different gate materials and make the much higher field in the channel region that improves the carrier transit speed and hence increases the device driving capability. Due to the screen effects from the gate with low work function of DMG MOSFET, the high electric field near the drain end is effectively reduced, which suppresses the hot carrier effects and reduces the substrate current leakage.

As predicted by Choudhary [3] Dual material when used in Single gate SOI MOSFET gives the much better performance in terms of SCEs. Kumar & Chaudhary [19] developed the threshold voltage model for dual material surrounding gate MOSFET using Quasi potential approach (QPA). Chiang [20] developed the exact two-dimensional subthreshold behavior model, which comprises two-dimensional potential, threshold voltage, subthreshold current, and subthreshold swing and found that DMSG MOSFET exhibits superiority over single material for lowering SCEs.

3.5. Strained Vs Unstrained Si Channel

By appling the stress on the Si the lattice constant of Si changes and so we have to use SiGe below the strained Si as shown in fig.6, so that there are no dislocations in the structure explained by Kim et al. [21] and Batwani et al. [22].

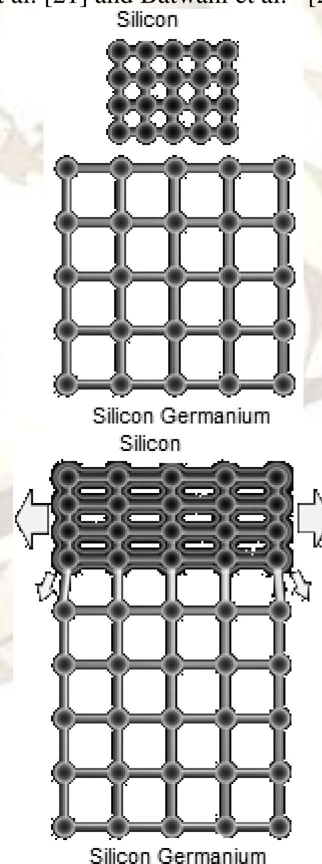

Fig.6 Unstrained Si (top) and Strained Si (bottom)

The stress applied to Si channel lifts band degeneracies, causes band warping and hence results in carrier effective mass change.
From the mass-mobility relation we have:

$$\mu = \frac{e\,\tau}{m^*\,\mu}$$

Where m* is the effective mass, τ is the relaxation time and μ is the mobility. So as the effective mass reduces the mobility increases. In this way by using stressed Si, the mobility in the channel can be increased.

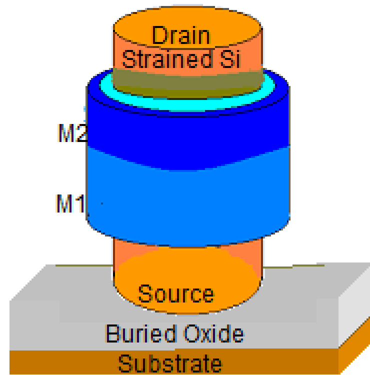

Fig.7 Dual-material Gate-all-around strained Si MOSFET

Nuo [25] suggested the Strained Si MOSFET as the next generation MOSFET by simulating the results for different gate structures.Gate-all-around MOSFET along with the benefits of dual-material and the strained Si model is the proposed one and is shown in fig.7.

IV. Conclusion and Future Work

The scaling of CMOS transistors has driven the tremendous growth of the semiconductor industry. As described by various authors CMOS is reaching its limits. In this review paper all models derived till now has been discussed along with their limits. A work can be proposed for modeling of a SOI MOSFET using DM Gate-All-Around Structure with stressed III-V group materials for channel including the QME. This proposed model could replace the CMOS when the limit is reached.

REFERENCES

[1] S. M. Kang, "Chip Input and Output (I/O) Circuits," in *CMOS Digital Integrated Circuits*, 3rd edition, Ed. New York: McGraw Hill, 2012, pp. 576-81.
[2] Bob Ulicki, "SOI Fundamentals", presented at SOI Consortium, march 2009.
[3] A. Choudhary, "Analytical Modeling and Simulation of Short-Channel Effects in a Fully Depleted Dual-Material Gate (DMG) SOI MOSFET," Master Thesis, IIT, Delhi, Dec-2003.
[4] A. K. Kushwaha, "On the Modeling of Dual Material Double-gate Fully Depleted Silicon on Insulator MOSFET," PhD Thesis, NIT, Kurukshetra, 2011.
[5] A. Chaudhary, S. Sangwan, J.N. Roy, "Mobility Models for Unstrained and Strained Silicon MOSFETS: A review," *journal of Comtemporary Engineering Sciences,* Vol. 4, No.5, 2011, pp. 229-247.
[6] G. E. Moore, "Cramming more Components onto Integrated Circuits," *Electronics letter*, Vol. 38, No. 8, April 19, 1965.
[7] International Technology Roadmap for Semiconductors. Website: http://www.itrs.net/Links/2011ITRS/2011Chapters/2011ERD.pdf
[8] lihui Wang, "Quantum Mechanical Effects on MOSFET scaling limits," PhD Thesis, Georgia Institute of Technology, 2006.
[9] A. Chaudhary and J.N. Roy, "MOSFET Models, Quantum Mechanical Effects, Modelling Approaches: A review," *Journal of Semiconductor technology and Science*, Vol. 10, No. 1, 2010.
[10] H. Abebe and E. Cumberbatch, "Quantum Mechanical Effect Correction Model for Inversion Charge and Current-Voltage Characteristics of MOSFET Device," in *proc. of Nanotech Conference*, Vol 2, 2003, pp. 218-221.
[11] B. Subrahmanyam, M. Jagadesh Kumar, "Recessed source concept in nanoscale vertical surrounding gate (VSG) MOSFETs for controlling short-channel effects," *journal of Physica E*, vol. 41, 2009, pp. 671–676
[12] L. Perron, C. hamagucchi, A. Lacaita, S. Maegawa, Y. Yamaguchi, "Dynamic Floating body effect in PD SOI MOSFETs biased in Kink region," Osaka University, 2008.
[13] C. Tinella1, F. Gianesello, D. Gloria1, C. Raynaud, P. Delatte, A. Engelstein, J.M. Fournier, Ph. Benech, J. Jomaah, "Partially Depleted CMOS SOI Technology for Low Power RF Applications," presented at 13th GASS Symposium, Paris, 2005.
[14] J. P. Colinge, "The New Generation if SOI MOSFETs," *Romanian Journal of Information science and technology,* Vol. 11, 2008, pp. 3-15.
[15] J. P. Colinge, "Multi-gate SOI MOSFETs," *journal of Microelectronic Engineering,* vol. 84, 2007, pp. 2071–2076.
[16] Jingbin Li, Thomas J. Walls, and Konstantin K. Likharev, "Nanoscale SOI MOSFETs: In Search for the best geometry," Storny Brook University, U.S.A.
[17] D. Jimenez, J.J. Saenz, B. Iniguez, "Modeling of Nanoscale Gate-All-Around MOSFETS," *IEEE Electron Device Letters,* Vol. 25, No.5, 2004.
[18] W. Long, H. Ou, J. M. Kuo, and K. K. Chin, "Dual material gate (DMG) Field Effect

Transistor," *IEEE Transactions on Electron Devices*, Vol. 46, pp. 865-870, 1999.

[19] M.J. Kumar, A. Chaudhary, "Two-dimensional analytical modelling of fully depleted DMG SOI MOSFET and evidence for SCEs," *IEEE Transactions on Electronic Devices,* Vol. 4, pp. 569-75, 2004.

[20] T.K. Chiang, "A new compact subthreshold behavior model for dual material surrounding gate (DMSG) MOSFETs," *Journal of Solid-state electronics,* Vol. 53, 2009, pp. 490-496.

[21] K. Kim, O. Kwon, J. Seo and T. Won, "Two-Dimensional Quantum-Mechanical Modeling for Strained Silicon Channel of Double-Gate MOSFET," *Journal of the Korean Physical Society,* Vol. 45, December 2004, pp. S909_S913.

[22] H. Batwani, M. Gaur and M. Jagadesh Kumar, "Analytical drain current model for nanoscale strained-Si/SiGe MOSFETs," *International Journal for Computation and Mathematics in Electrical and Electronic Engineering,* Vol. 28, No. 2, 2009, pp. 353-371.

[23] J. Walczak and B. Majkusiak, "Electron mobility and drain current in strained-Si MOSFET," *journal of telecommunication and information technology,* 2007, Pages 84-87.

[24] P. Ghosh, S. Haldar, R. S. Gupta, M. Gupta, "An analytical drain current model for dual material engineered cylindrical/surrounded gate MOSFET," *Journal of Microelectronics*, Vol. 43, 2012, pp. 17–24.

[25] Nuo Xu, "Effectiveness of Strain Solutions for Next-Generation MOSFETs," PhD Thesis, University of California, Berkeley, Spring, 2012.