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Design and Analysis of an Enhanced Novel Multiplier with Low Power in Submicron Technology for VLSI Applications

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ABSTRACT

While performance and area remain to be two major design goals, power consumption has become a critical concern in today's VLSI system design. International technology roadmap for semiconductors (ITRS) reports that —when technology scales down leakage power dissipation may come to dominate total power consumption. So it's important and challenging task for low power designers in sub micron circuits. Multiplication is a fundamental operation in most arithmetic computing systems.Multipliers has large area, long latency and consumes considerable power. The innovative power gating schemes stacking power gating are analyzed which minimizes the power dissipation in submicron circuits.

The overall view of this paper is to attain high speed, low power full multiplier with alternative logic cells that lead to have reduced power dissipation. Here the total multiplier architecture is designed sub micron technology and observed the power analysis.

***Keywords* –** low power, submicron technology, ITRS.

I. INTRODUCTION

Multipliers are one of the most important arithmetic units in microprocessors and DSPs and also a major source of power dissipation. Reducing the power dissipation of multipliers is key to satisfying the overall power budget of various digital circuits and systems. . Power consumed by multipliers can be lowered at various levels of the design hierarchy, from algorithms to architectures to circuits, and devices. Here we designed multiplier in two different architecture and compare these with conventional general multiplier architecture.

In this paper we designed multiplier architecture in array model and tree style with specially designed novel components to reduce power dissipation and designed these architectures in submicron technology.

II. GATE DIFFUSION INPUT (GDI)

GDI method is based on the use of a simple cell as shown in figure 1. the design is seems to be like an inverter, but the main differences are 1) it Consist of three inputs- G (gate) input to NMOS/PMOS), P (input to source of PMOS) and N (input to source of NMOS). (2) Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with CMOS inverter.

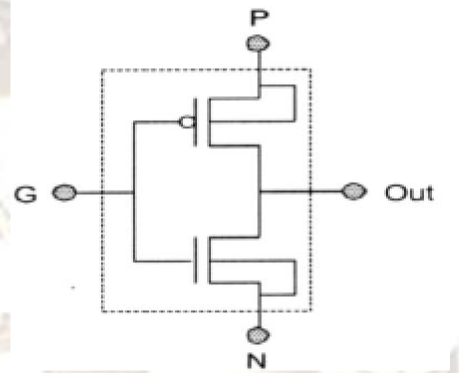

Fig.1 : GDI base cell

N	P	G	Out	Function
'0'	B	A	AB	F1
B	'1'	A	A +B	F2
'1'	B	A	A +B	OR
B	'0'	A	AB	AND
C	B	A	AB+AC	MUX

Table 1. Various logic functions of GDI cell

III. FULL ADDER

A full adder could be a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. In our design, we have designated the three inputs as A, B and C. The third input C represents carry input to the first stage. The outputs are SUM and CARRY. Fig 1 shows the logic level diagram of full adder. The Boolean expressions for the SUM and CARRY bits are as shown below. SUM bit is the EX-OR function of all three inputs and CARRY bit is the AND function of the three inputs. The truth table 2 of a full adder is shown in Table 2. The truth table also indicates the status of the CARRY bit; that is to say, if that c array bit has been generated or deleted or propagated.

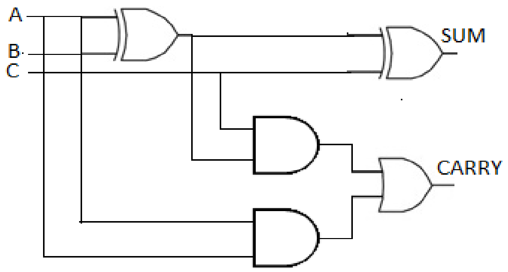

Fig 2. logic diagram of full adder

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
11	1	1	1	1

Table 2. truth table of a full adder.

If either one of A or B inputs is '1', then the previous carry is just propagated, as the sum of A and B is '1'. If both A and B are '1's then carry is generated because summing A and B would make output SUM '0' and CARRY '1'. If both A and B are '0's then summing A and B would give us '0' and any previous carry is added to this SUM making CARRY bit '0'. This is in effect deleting the CARRY.

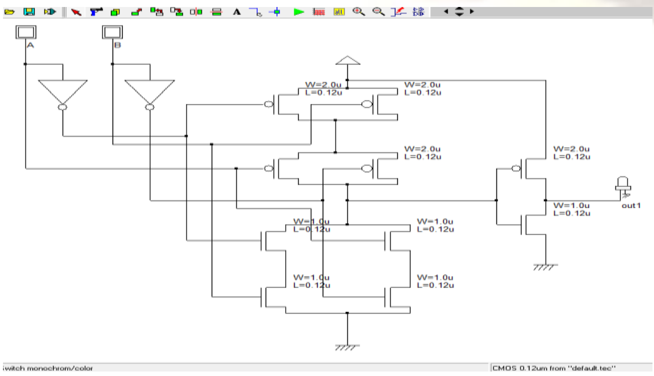

Fig 3. Schematic for XOR-gate

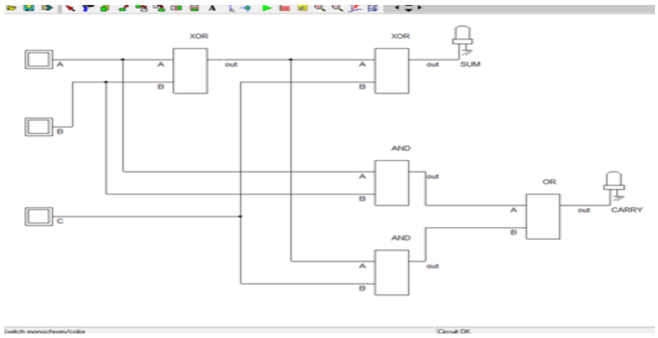

Fig 4. Schematic for full adder

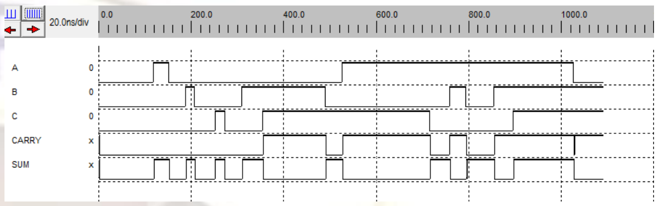

Fig 5. Simulation results for full adder.

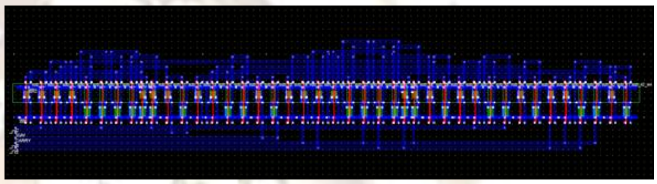

Fig 6. Layout for full adder.

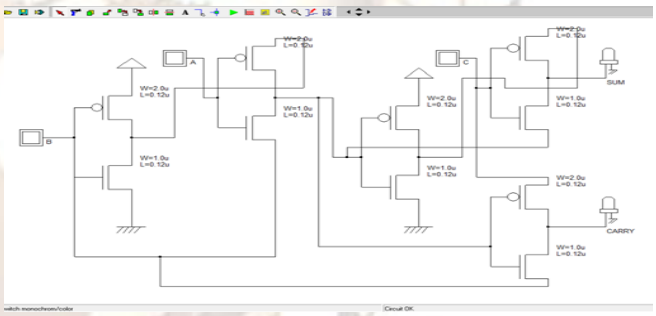

Fig 7. GDI-XNOR FULL ADDER

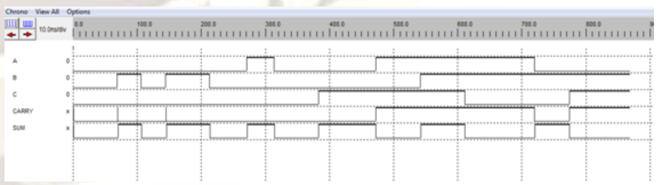

Fig 8. Schematic for GDI-XNOR full adder

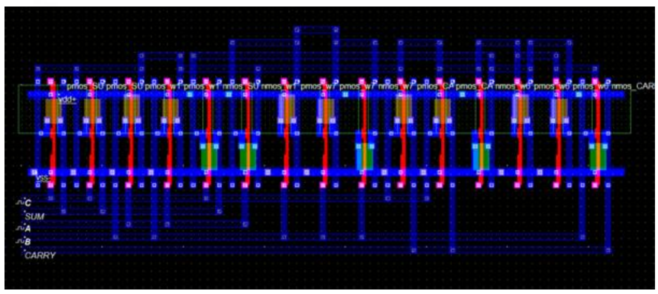

Fig 9. Lay out for GDI-XNOR full adder

III.1 SLLEPY AND GATE

This sleepy technique is used to reduce leakage power in digital circuits. The leakage power reduction is a challenging job low power VLSI designers.

In this technique a PMOS is placed between power supply and pull up network and NMOS is placed between pull down network and ground these two transistors are called sleepy transistors these transistor are reduced leakage power when the circuit is not in active state. This PMOS have high VTH, NMOS have low VTH value.

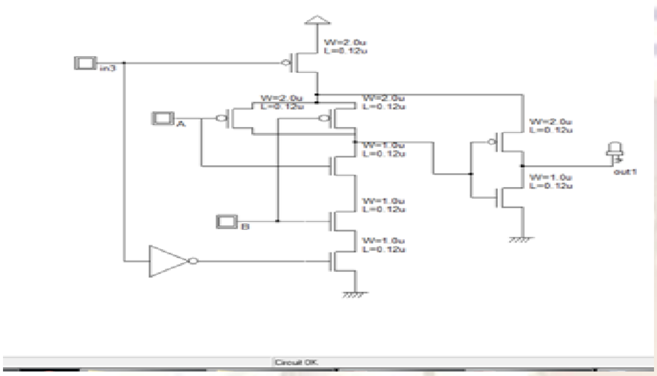

Fig 10. Schematic for SLEEPY-AND circuit.

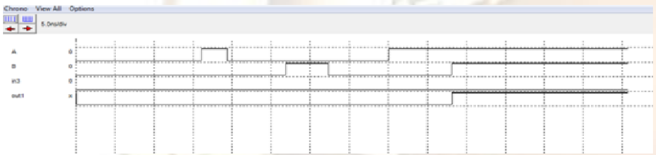

Fig 11. Simulation results for SLEEPY-AND circuit

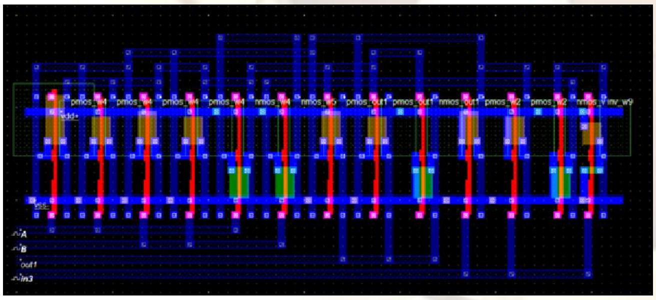

Fig 12. Layout for SLEEPY-AND circuit

IV. MULTIPLIER ARCHITECTURES

The wide-bit addition is vital in many applications such as ALUs,multiply-and accumulates (MAC) units in DSPs,and ,versatile microprocessor. Different types of multiplier implementations are exists Where as some are good for low power dissipation. In multiplication, multiplicand is added to itself a number of times as specified by the multiplier to generate product. In this paper, three different 4-bit multiplier architectures are designed.

IV.I CONVENTIONAL MULTIPLIER ARCHITECTURE

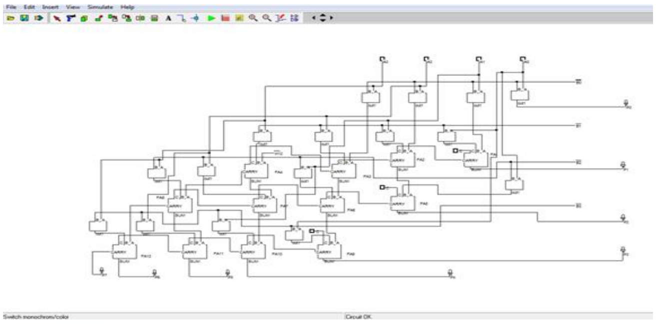

Fig 13. Schematic for basic multiplier architecture

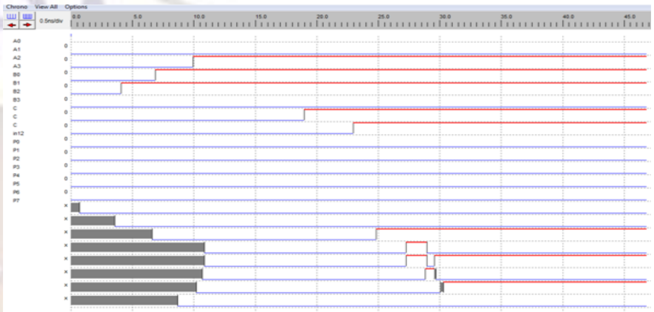

Fig 14. Simulation results for basic multiplier architecture.

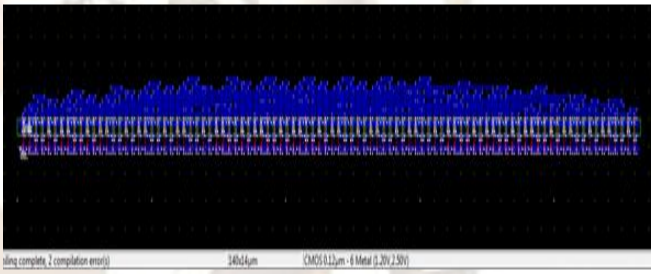

Fig.15 Layout for basic multiplier architecture

IV.2 ARRAY MULTIPLIER ARCHITECTURE

An array multiplier is very regular in structure. It uses short wires that go from one full adder to adjacent full adders horizontally, vertically or diagonally. An n xn array of AND gates can compute all the a b terms simultaneously. The terms are summed by an array of ‘n [n - 2]’ full adders and ‘n’ no of half adders.The number of rows in array multiplier denotes length of the multiplier and width of each row denotes width of multiplicand.The output of each row of adders acts as input to the next row of adders. The advantage of array multiplier is its regular structure. Thus it is easy to layout and has small size. In VLSI designs, the regular structures can be tiled over one another. This reduces the risk of mistakes and also reduces layout design time. This regular layout is widely used in VLSI math co-processors and DSP chips.

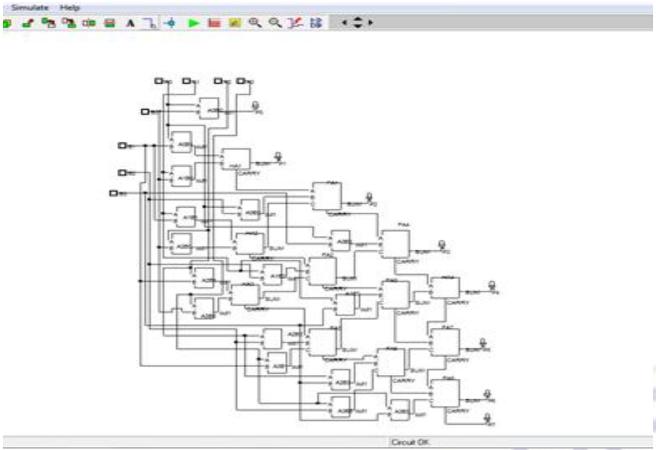

Fig 16. Schematic for array multiplier architecture

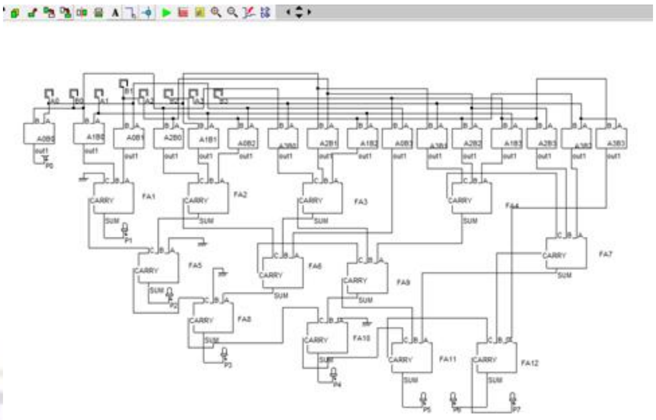

Fig 19. Schematic for tree multiplier architecture

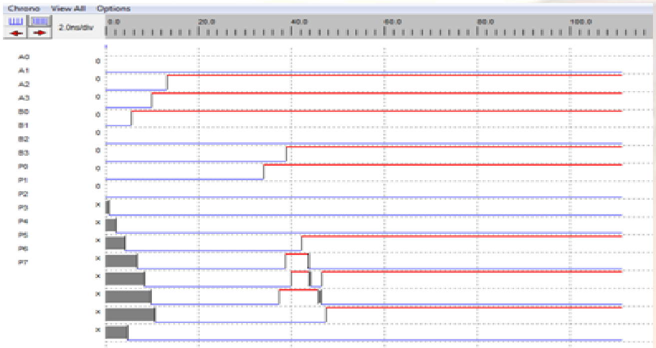

Fig 17. Simulation results for array multiplier architecture

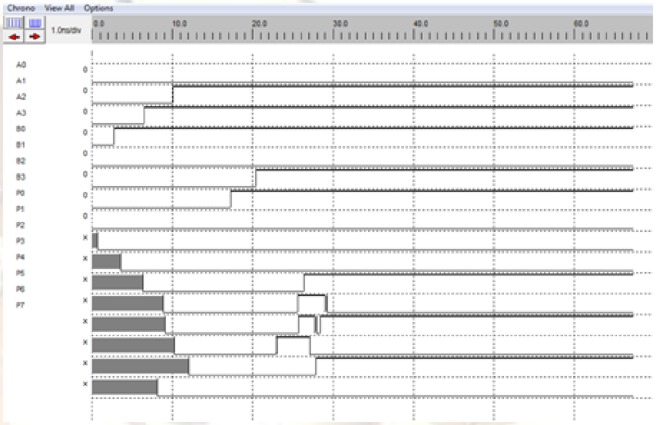

Fig 20. Simulation results for tree multiplier architecture

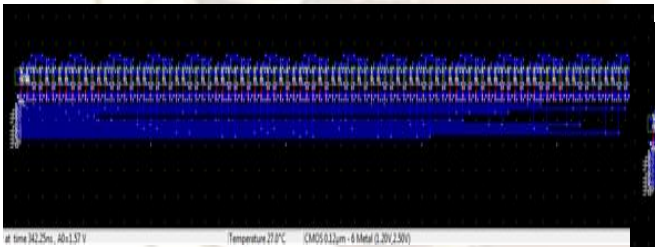

Fig 18. Layout for array multiplier architecture

Fig 21. Layout for tree multiplier architecture

IV.2 TREE MULTIPLIER ARCHITECTURE

This architecture is used where speed is the main concern not the layout regularity. This class of multipliers is based on reduction tree in which different schemes of compression of partial product bits can be implemented. In tree multiplier partial-sum adders are arranged in a treelike fashion, reducing both the critical path and the number of adders needed. The partial products or multiples are generated simultaneously by using a collection of AND Gates. The multiples are added in combinational partial products reduction tree using carry save adders, which reduces them to two operands for the final addition.

V. PROPOSED MULTIPLIER ARCHITECTURE

In this proposed architecture we are using GDI-XNOR full adder and sleepy and gate to design the total architecture with low power dissipation. Here we designed multiplier architectures in array and tree style with these low power components for VLSI and Embedded applications.

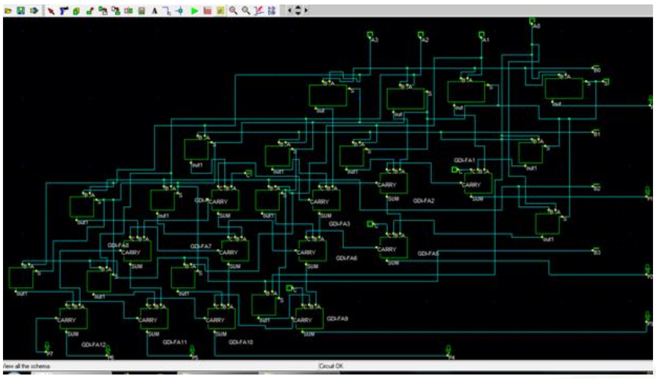

Fig 22. Proposed conventional multiplier architecture

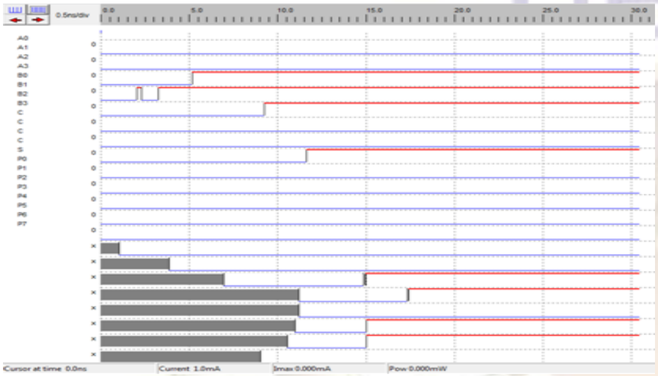

Fig 23. Simulation results for conventional architecture

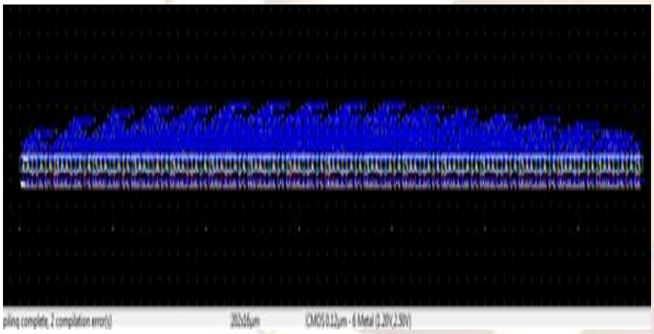

Fig 24. Layout for conventional multiplier architecture

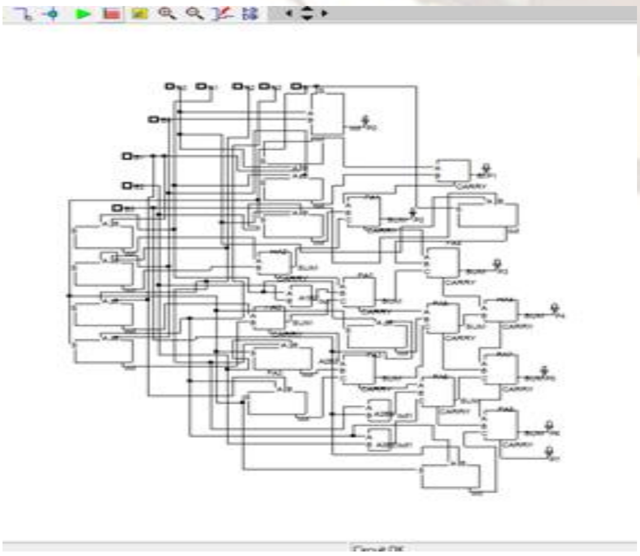

Fig 25. Proposed array multiplier architecture

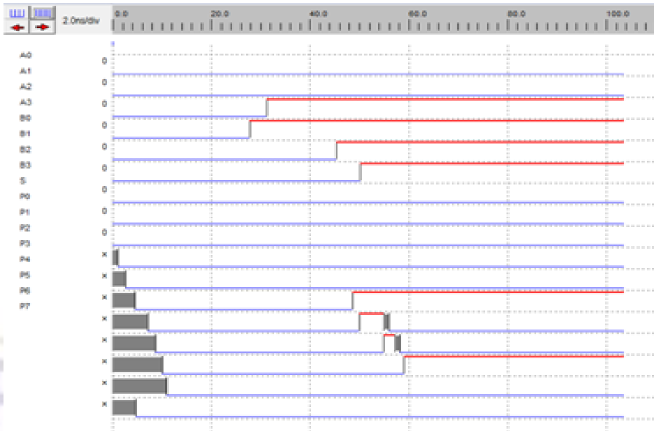

Fig 26. Simulation results for array multiplier architecture

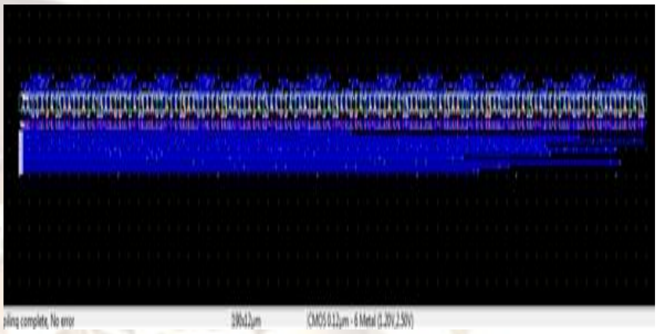

Fig 27. Layout for proposed array multiplier architecture.

POWER ANALYSIS:

TOPOLOGY	180nm (uw)	120nm (uw)	90nm (uw)	70nm (uw)
AND GATE	24.01	10.07	7.27	1.74
SLEEPY-AND GATE	15.43	3.64	2.46	0.98

Table 3. power analysis for AND gate and SLEEPY AND gate

TOPOLOGY	180nm (uw)	120nm (uw)	90nm (uw)	70nm (uw)
FUL ADDER	73.54	40.32	28.62	9.62
GDI-XNOR FA	34.16	5.04	2.91	1.93

Table 4. power analysis for general FULL ADDER and GDI-XNOR FA

TOPOLOGY	180nm (uw)	120nm (uw)	90nm (uw)	70nm (uw)
CONVENTIONAL MULTIPLIER	I.43 E-3	730.20	459.72	143.4
PROPOSED MULTIPLIER	535.8	118.72	74.28	29.04

Table 5. power analysis for conventional and proposed multiplier

TOPOLOGY	180nm (uw)	120nm (uw)	90nm (uw)	70nm (uw)
ARRAY MULTIPLIER	1 E -3	536	368.8	118
PROPOSED ARRAY MULTIPLIER	658.88	153.6	95.6	44.88

Table 6. power analysis for array and proposed array multiplier

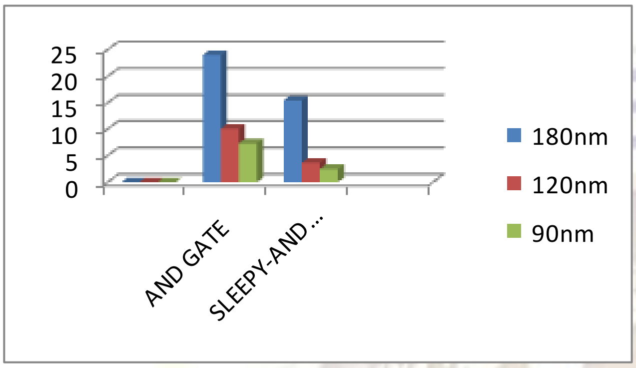

Fig 28. Power analysis graph for AND and SLEEPY AND gate

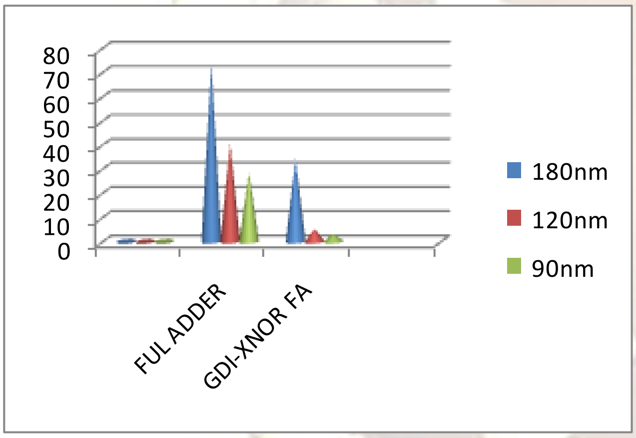

Fig 29. Power analysis graph for FA and GDI-XNOR FA

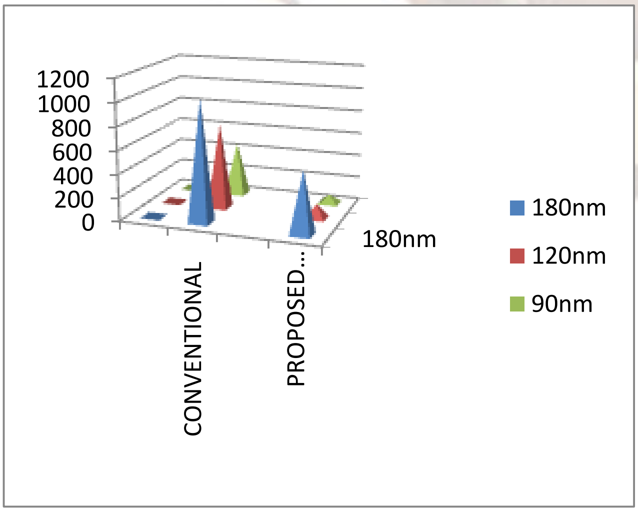

Fig 30. Power analysis graph for CONVENTIONAL and PROPOSED multiplier

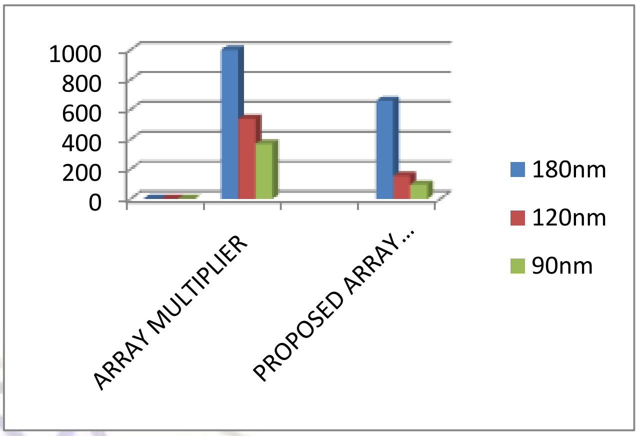

Fig 31. Power analysis graph for ARRAY and PROPOSED ARRAY multiplier

V1.CONCLUSION

It has been observed that the proposed basic multiplier and array multiplier have less power consumption compared to general one. Here we are placing low power full adder namely GDI-XNOR full adder and SLEEPY AND gate to reduce leakage power and we observed that in architectural model tree structural multiplier have less power consumption compared to array structural multiplier.

This newly proposed 4 bit multiplier architecture can be used to design all the low power VLSI and Embedded devices

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