# Design and Implementation of 7 Bit 100 MHz Flash ADC

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**ABSTRACT**
      This paper presents the design and implementation of 7 Bit 100MHz Flash ADC.The circuit is designed in GPDK 90nm CMOS technology, with a supply voltage of 1.2V. The main advantage of flash adc is that it is one of the fastest adc. The reference voltage source is implemented using band gap reference circuit and verified the performance by varying temperature from $-10^0$ C to $70^0$ C.

*Keywords* - Bandgap Reference, Comparator, Resistor Ladder, ROM encoder, Thermometer to Binary encoder

## I.      INTRODUCTION

      The world is getting more and more digital everyday. The need for high speed analog to digital converter is increasing. This paper deals with the design of 7 bit flash adc. The paper also contains various problems associated with the resistor ladder and the comparator.
      Flash ADC is the fastest of all adcs. It employs parallelism and distributed sampling to achieve high conversion speed[1].The different components of flash adc are described in section II. Simulation results are shown in section IV.
      The reference voltages used are 600mV and 1.2V. In order to make these reference voltages and currents independent of temperature, supply voltage and process parameter variations, bandgap reference circuit is used. It is described in section III.

## II.      ADC ARCHITECTURE

      7 bit flash ADC consists of mainly 3 components namely - a.) Resistor ladder which has 128 resistors. The resistor ladder subdivides the reference voltage into 127 voltages
b.) 127 comparators which compares the reference voltage generated by the resistor ladder with the input voltage.
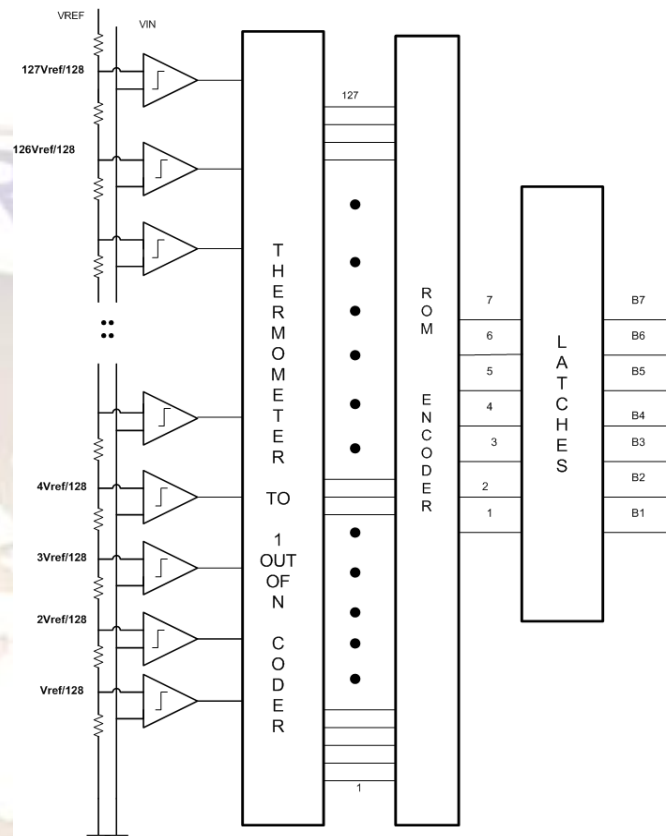c.)  thermometer to binary encoder



Fig 1. Block diagram of flash ADC

### 2.1  RESISTOR LADDER

      The resistor ladder consists of $2^n$ resistors where n is the number of bits. These resistors divides the reference voltage into 127 voltage levels.
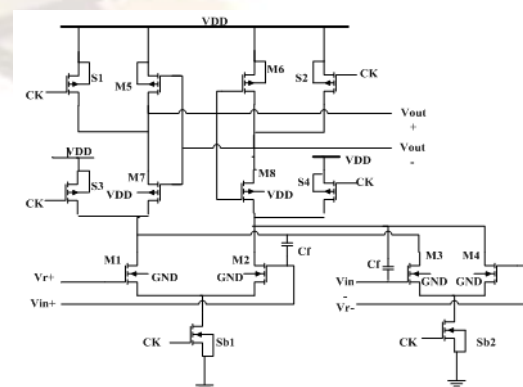
### 2.2  COMPARATOR



Fig 2. Comparator [2]

The comparator compares the input voltage with the reference voltage generated by the resistor ladder. The comparator has certain problems associated with it. One of the main problem is Kickback noise[3] which is due to the parasitic capacitance between the drain and the input of the comparator. This can be avoided by using a neutralizing capacitor in the input of the comparator. There is another problem caused by parasitic capacitance between the input of the comparator to the source and thus to the resistor ladder. It may cause a wide variation in the reference voltages in the resistor ladder. This can be reduced by reducing the value of the resistance.
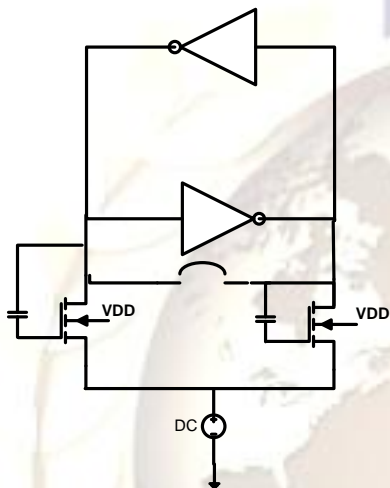


Fig 3. Kickback noise in comparator

## 2.3 THERMOMETER TO BINARY ENCODER

The comparator output is in thermometer code which has to be converted to binary. The thermometer to binary encoder can be implemented in different ways - ROM encoder, fat tree encoder, Wallace tree encoder. Of the three ROM encoder is simpler to implement. To address the ROM encoder lines we need to convert the thermometer code to one shot pulses. For this a one to N coder is used to convert thermometer code to monopulses.
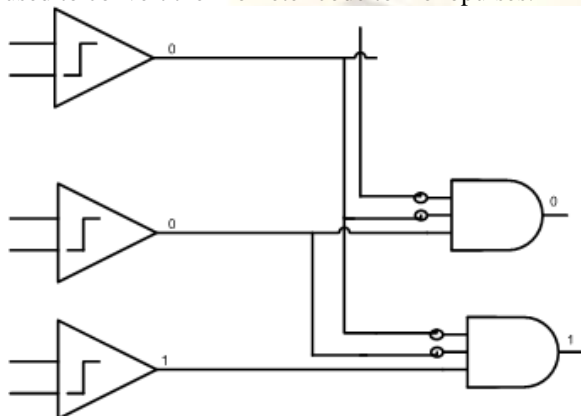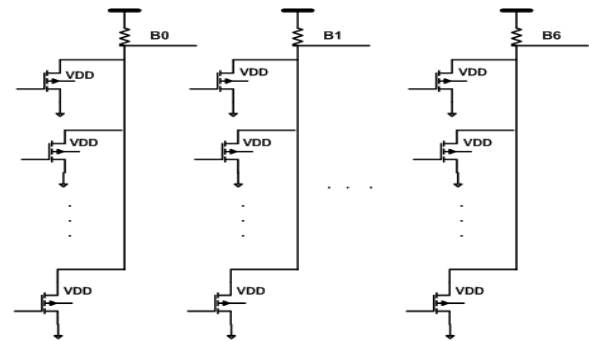


Fig 4. One out of N coder circuit



Fig 5. ROM encoder schematic

| T1 | T2 | T3 | T4 | T5 | T6 | T7 | B1 | B2 | B3 |
|----|----|----|----|----|----|----|----|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Table 1. thermometer to binary code

In order to avoid the effect of sparkles [4][5], the circuit shown in Fig 3. is used.ROM encoder consists of 7 lines with 62 NMOS switches in each lines. The lines are connected to VDD when the switches are off ie, output of that line will be VDD. When any one of the switch in the line turns on, the output of that line will be zero. Thus the output will be in binary form.

## III. BANDGAP REFERENCE CIRCUIT

Analog circuits may contain both voltage and current references. In order to make these reference voltages and currents independent of temperature, supply voltage and process parameter variations [1], bandgap reference circuit is used. Designed a bandgap reference circuit for 600mV and 1.2V and analyzed the circuit for temperature variation from -10°C to +80°C. The variation was seen to be ±20mV.
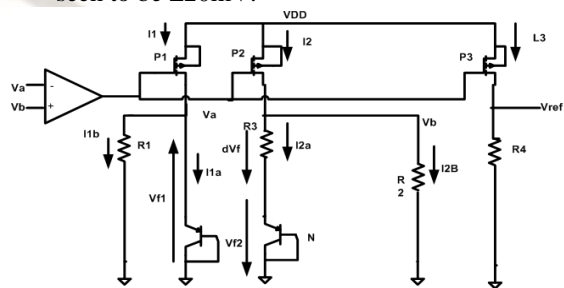


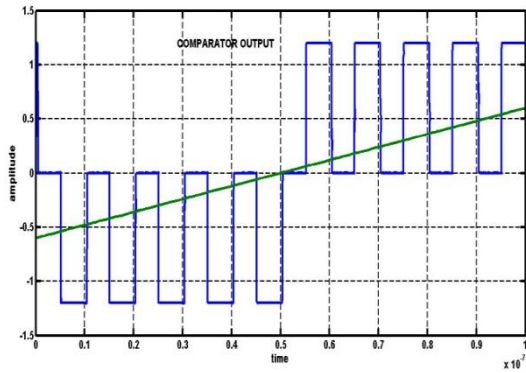Fig 6. bandgap reference circuit

## IV. SIMULATION RESULTS



Fig 7. comparator differential output
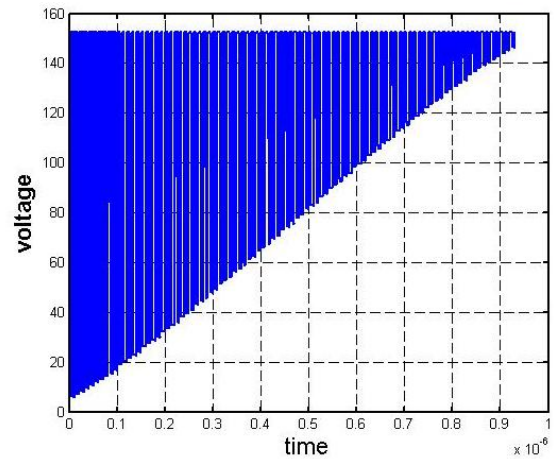
### 4.1 EFFECT OF KICKBACK NOISE
**4.1.1 $C_f$ = 12fF, R = 100 Ω**
**$C_f$ - capacitor at the input of the comparator**
**R - resistance in the resistor ladder**
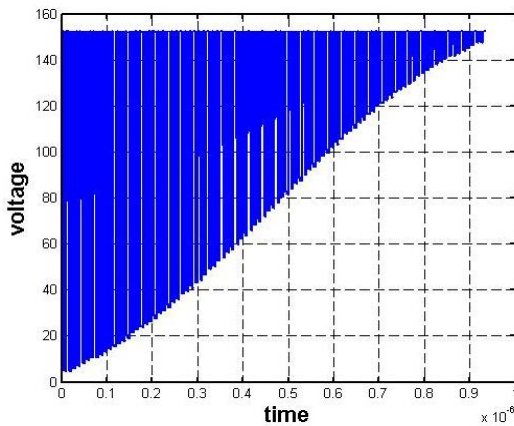
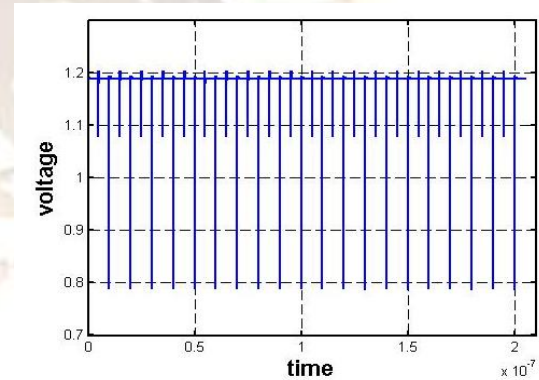

Fig 13. Transient sum of comparator outputs for ramp input



Fig 14. Reference voltage settling

**4.1.2 $C_f$ = 12fF, R = 15 Ω**



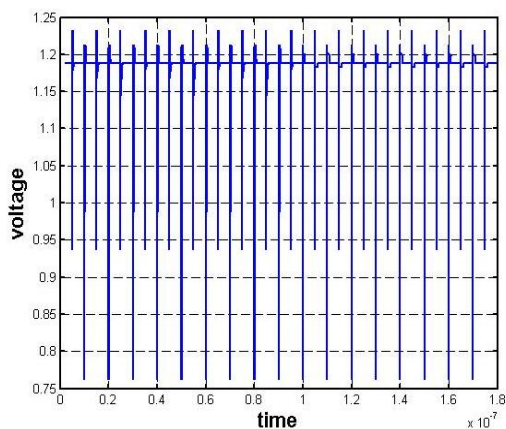Fig 15. Transient sum of comparator outputs for ramp input



Fig 16. Reference voltage settling

The fig 11-16 shows the problems due to kickback noise and high resistance in the resistor ladder as discussed in section 2.2.
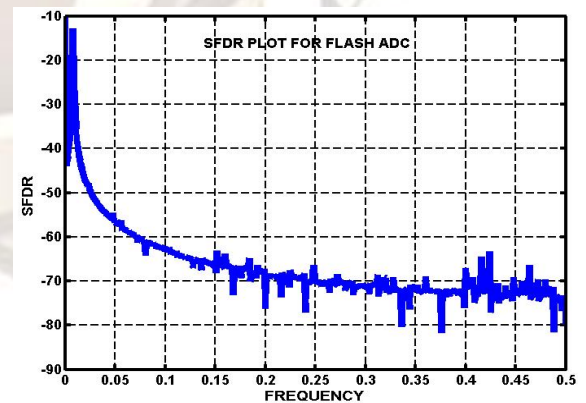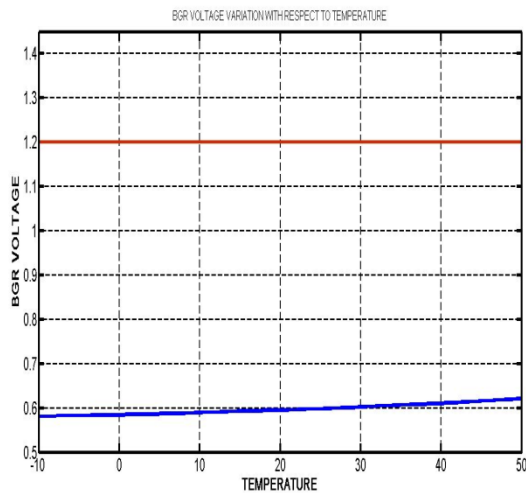


Fig 17. SFDR Plot

Fig 18.  BGR voltage variation with respect to temperature

## V.     RESULTS

|  | FLASH |
|---|---|
| PROCESS | 90nm |
| RESOLUTION | 7 BIT |
| SAMPLING FREQUENCY | 100MHz |
| VDD | 1.2V |
| Fin | 0.8MHz |
| INL | 0.5 LSB |
| SFDR | 51 dB |
| SNDR | 41 dB |

Table 2. Measurement Summary

## VI.     CONCLUSION

A flash ADC design based on a dynamic Differential Comparator and ROM encoder approach has been proposed. The design has been carried out for 90nm technology in cadence environment. Since the reference voltages are generated internally using bandgap reference circuit, the power dissipation is reduced. The converter achieves an integral nonlinearity of 0.5 LSB, and a signal-to-(noise + distortion) ratio of 41 dB at a sampling rate of 100 MHz.

**REFERENCES**
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