

## Design of High Speed Multiplier Using Reversible Logic

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### ABSTRACT

In current scenario, the reversible logic design attracting more interest due to its low power consumption. Reversible logic is very important in low-power circuit design. The important reversible gates used for reversible logic synthesis are Feynman Gate, Fredkin gate, toffoli gate etc. This paper present a basic reversible gate to build more complicated circuits which can be implemented in ALU, some sequential circuits as well as in some combinational circuits. It also gives brief idea to build adder circuits using the basic reversible gate like peres gate This paper proposes a novel 4x4 bit reversible fault tolerant multiplier circuit which can multiply two 4-bit numbers. This based on two concepts. The partial products can be generated in parallel using PG gates and thereafter the addition is done by using reversible parallel adder designed from PFAG gates. Thus, this paper provides idea for building of more complex system which can execute more complicated operations using reversible logic.

*Keywords* - Garbage output, peres gate, PFAG, Reversible logic

### I. INTRODUCTION

Energy dissipation is an important consideration in VLSI design. Reversible logic was first related to energy when Landauer states that information loss due to function irreversibility leads to energy dissipation. This principle is further supported by Bennett that zero energy dissipation can be achieved only when the circuit contains reversible gates [2]. Information is lost when the input vector cannot be uniquely recovered from its output vectors. Reversible logic circuits naturally take care of heating since in a reversible logic every input vector can be uniquely recovered from its output vectors and therefore no information is lost. According to [1,2] zero energy dissipation would be possible only if the network consists of reversible gates. Thus reversibility will become an essential property in future circuit design. Reversible circuits are also interesting because the loss of bits of information implies energy loss. However, reversible logic is suffering from two problems. Firstly, there is a lack of technologies with which to build reversible gates. Work is certainly continuing in this area. Secondly, while there is much research into how

to design combinational circuits using reversible logic, there is little in the area of sequential reversible logic implementations. . "To establish the relevance of reversible and quantum computing it seems appropriate to note that the VLSI industry is moving at high speed towards miniaturization. With miniaturization it faces two issues: i) A considerable amount of energy gets dissipated in VLSI circuits and ii) the size of the transistors are approaching the quantum limits where tunneling and other quantum phenomena are likely to appear. Thus, we need a superior technology that can circumvent these problems. Power dissipation is one of the important parameters in the digital circuit design. In VLSI circuit designing where power dissipation plays an important role, there has been an increasing trend of packing more and more logic elements into smaller and smaller volumes and clocking them with higher frequencies. The logic elements are normally irreversible in nature and according to Landauer's principle irreversible logic computation results in energy dissipation due to power loss. This is because; erasure of each bit of information dissipates at least  $KT \ln 2$  Joules of energy where K is Boltzmann's constant and T is the absolute temperature at which the operation is performed. By 2020 this will become a substantial part of energy dissipation, if Moore's law continues to be in effect which states that processing power will double every 18 months. This particular problem of VLSI designing was realized by Feynman and Bennet in 1970s. In 1973 Bennet [2] had shown that energy dissipation problem of VLSI circuits can be circumvented by using reversible logic. This is so because reversible computation does not require erasing any bit of information and consequently it does not dissipate any energy for computation. . In a short period the reversible computation has emerged as a promising technology having applications in low power CMOS, nanotechnology ,optical computing ,optical information processing, DNA computing, bioinformatics, digital signal processing and quantum computing. It is very clear that reversible circuits will play dominant role in future technologies. These facts motivated many researchers to work in this domain A reversible logic gate must have the same number of inputs and outputs, and for each input pattern there must be a

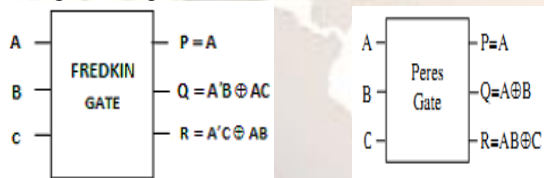
unique output pattern. Thus, Reversible logic circuits avoid energy loss by un computing the computed information by recycling the energy in the system. In the design of reversible circuits two restrictions should be considered; firstly, Fan-out is not permitted and secondly, Feedback from gate outputs to inputs is not permitted. Due to these restrictions, synthesis of reversible circuits can be carried out from the inputs towards the outputs and vice versa . So, there is a one-to-one mapping between input and output vector. A logic synthesis technique using a reversible gate should have the features like minimum gate count along with less use of constants and garbage generation. Reduction of these parameters is the main design focus. Reversible circuits for different purposes like half adder, full adder multiplier[3-11,15] have been proposed recently. Among these reversible circuits, multiplier circuits are of special importance because of the fact that they are the integral components of every computer system, cellular phone and most digital audio/video devices.

**II. REVERSIBILITY AND BASIC REVERSIBLE GATES**

The gate/circuit that does not loose information is called reversible. A Reversible circuit has the facility to generate a unique output vector from each input vector, and vice versa.

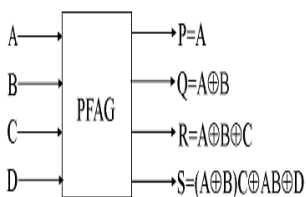
**II.1 Reversible Gates**

Different reversible gates include Fredkin gate, Peres gate, IG gate etc. are shown below

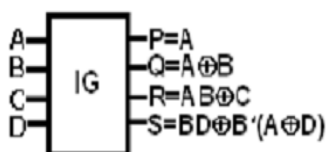


(a.)Feyman Gate

(b)Peres Gate



(c) Peres full adder gate



(d) IG Gate

Fig. 1 Basic Reversible Gate

**II.2. Parity Preserving fault tolerant Reversible Gates**

Fault tolerance is the property that enables a system to continue operating properly in the event of the failure of some its components. If the system itself made of fault tolerant components, then the detection and correction of faults become easier and simple. In communication and many other systems, fault tolerance is achieved by parity. Therefore, parity preserving reversible circuits will be the future design trends to the development of fault tolerant reversible systems in various fields. And a gating network will be parity preserving if its individual gate is parity preserving [11].

**III. PROPOSED WORK**

A logic synthesis technique using a reversible gate should have the features like minimum gate count along with less use of constants and garbage generation. Reduction of these parameters is the main design focus. It is important for every processor to have a high speed multiplier. The design of the multiplier is based on parallel operation .it is done using two steps.

Part i: Partial Product Generation (PPG)

Part ii: Reversible Fault Tolerant Parallel Adder (RFTP)

As mentioned before, the purpose of this paper is the design of reversible fault tolerant multiplier circuit with the aim of optimizing its hardware complexity to make it more economical in terms of number of garbage outputs and constant inputs without losing its efficiency. The multiplier is implemented using PG and PFA gates. The operation of a 4\*4 reversible multiplier in Fig2. It consists of 16 Partial product bits of the four bit inputs X and Y to perform 4 \* 4 multiplications.

Partial Product Generation					$x_3$	$x_2$	$x_1$	$x_0$
		x	$y_3$	$y_2$	$y_1$	$y_0$		
			$x_3y_0$	$x_2y_0$	$x_1y_0$	$x_0y_0$		
		$x_3y_1$	$x_2y_1$	$x_1y_1$	$x_0y_1$			
Multi Operand Addition	$x_3y_2$	$x_2y_2$	$x_1y_2$	$x_0y_2$				
	$x_3y_3$	$x_2y_3$	$x_1y_3$	$x_0y_3$				
	$P_7$	$P_6$	$P_5$	$P_4$	$P_3$	$P_2$	$P_1$	$P_0$

Fig 2. Basic 4\*4 multiplication

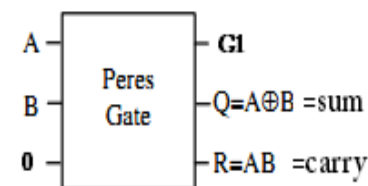


Fig 3. PG Gate as half adder

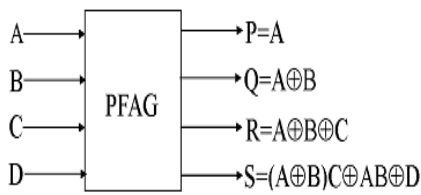


Fig 4. PFAG gate for full adder addition

PG gate used as half adder is shown in Fig.3. It requires one constant inputs of logic 0 and produces the required sum and carry term with one garbage outputs. To implement full adder circuit we can use PFAG gate as shown in fig.4

**III.1 Partial Product Generation (PPG)**

For product term generation the PG gate is used. The PG gate is used to perform AND operation by forcing one constant input as logic 0 whereas it produces required product term along with two garbage outputs. The Fig. 5 shows the implementation of AND operation using PG gates. Multiplier partial products are generated using 16 PG gates as shown in Fig. 5

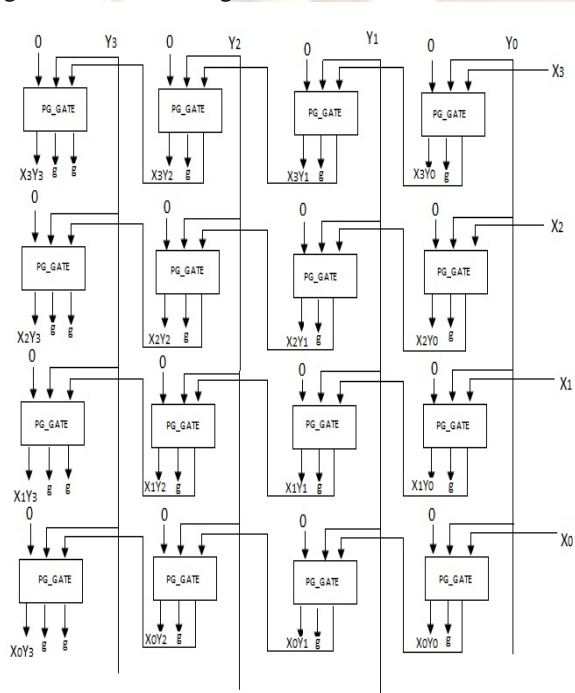


FIG 5. PPG using PG gate

**III.2 Reversible Fault Tolerant Parallel Adder (RFTPA)**

The RFTPA circuit needs reversible fault tolerant full adder (FTFA) and half adder (FTHA). Many reversible full adders have been proposed in the past. For example, TSG, MKG,IG and HNG gates can singly perform the full adder operation. Design of multipliers with these gates indicates the different critical parameters for reversible multipliers.

Experimental results of different reversible multiplier circuits in terms of number of garbage outputs and constant inputs show that multiplier circuits with adders designed using PFAG gates have better results than multiplier circuits with PFAG gates.

**IV. RESULTS**

The entire architecture is modeled using VHSIC hardware description language .The coding is done on Xilinx ISE8.2i For simulation purpose the Modelsim6.2h has been used. The simulation result for proposed multiplier is shown in Fig. 7. The proposed multiplier is efficient in terms of number of reversible gates and garbage output. Reduction in number of gates reduce complexity of circuit

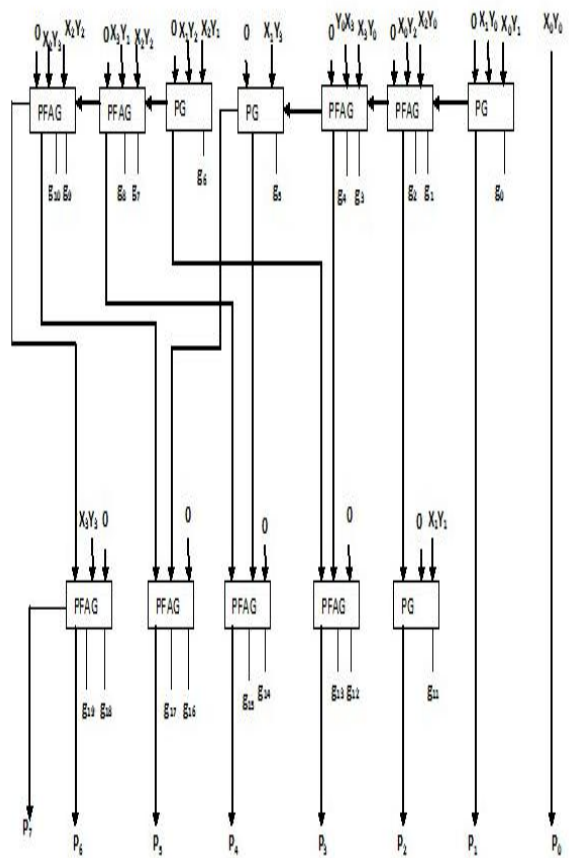


Fig.6 RFTPA Circuit

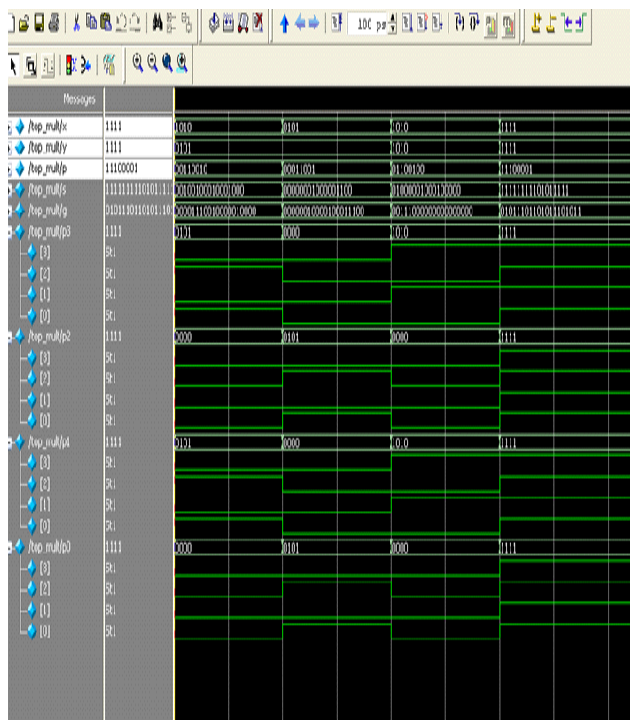


Fig.7 simulation result for proposed system

	Garbage output	Constant input	No. of gates
Fault tolerant multiplier	64	37	36
Proposed multiplier	40	28	28

Table1.Comparison table for the system

## V. CONCLUSION

Multiplier is a basic arithmetic cell in computer arithmetic units. The energy consumption in computation turns out to be deeply linked to the reversibility of the computation. In the proposed work, we designed a reversible multiplier using pg and pfg gate with reduced gate count and reduced garbage output. The comparison table shows clear idea of the system with the existing one. Reduction in number of gate can reduce the circuit complexity. The chance for further research includes the reversible implementation of more complex arithmetic circuits such as function evaluation and multiplicative division circuits using this multiplier.

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