Comparison of Converter Fed Pmbldc Drive Systems with and Without Snubber

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Abstract

Permanent Magnet Brushless DC Motor has become a popular electrical drive because of its advantages such as high efficiency, increased reliability, quick dynamic response and very low maintenance. Due to this competitive edge it has stirred a lot of interest in simulating a PMBLDC Motor and its associated drive system in a comparatively simple manner. This paper elaborates the proposal of developing an inverter fed drive system with and without snubber in the circuit. This said snubber contains a resistor and a capacitor, where in the resistor is parallel connected with a diode. The voltage increases exponentially however the capacitance cannot change instantly therefore the critical rate of the rise in voltage slows down. Since the capacitor stores the required energy the same output is obtained even for reduced input ultimately increasing the motor efficiency. The snubber circuit can be credited with the advantages of reduced switching losses; it has a better impact on control of dv/dt and di/dt, reduction in the heating of the device, ripples and voltage transients. with the aid of MATLAB/SIMULINK software package the simulation of the PMBLDC motor drive system with and without snubber can be developed. The paper exploring the operating principle of the snubber circuit and also analyses its simulation results to verify and substantiate the theoretical analysis.

Keywords : BLDC, Converters, Snubbers, Matlab / Simulink.

I. Introduction

Permanent magnet brushless DC (BLDC) motor is increasingly used in automotive, industrial, and household products because of its high efficiency, high torque, ease of control, and lower maintenance (P C K Luk et al., 1994), (R.Krishnan., 2003). A BLDC motor is designed to utilize the trapezoidal back EMF with square wave currents to generate the constant torque. A conventional BLDC motor drive is generally implemented via a six-switch, three phase inverter (R.Krishnan et al., 1997), (Byoung- Kuk Lee et al., 2003) and three Hall-effect position sensors that provide six commutation points for each electrical cycle. Cost minimization (Rahul Khopkar et al., 2003) is the key factor in an especially fractional horse-power BLDC motor drive for Home applications. It is usually achieved by elimination of the drive components (F.L.Luo et al., 2005), (AtefSalehOthman et al., 2009) such as power switches and sensors. The switching losses are to be reduced and the power dissipation towards the switching techniques is analyzed and so a snubber circuit is implemented. snubbers are used in electrical systems to reduce the transient across the device while switching ON/OFF the device. While having a transient this may cause electromagnetic disturbance which in turn creates interference with nearby circuits (Muhammad Rashid ., 2009), (J.Michael Jacob ., 2009). The snubber prevents this undesired voltage by conducting transient current around the device. Therefore effective algorithms should be designed for the desired performance and the relevant drive system (Tan Chee Siong et al., 2011) which in turn controls the motor for all its defined applications with high efficiency, as well as good in maintaining the speed for variable torque (Lin Bai et al ., 2011). The above literature does not deal with comparison of converter fed PMBLDC drive systems with and without snubber. This work aims to compare the drive systems with and without snubber.

II. Design of Snubber

Semiconductor switch turns on in 10µs to 100µs. At that time the voltage across them falls and the current through the switch rises. These extremely large and fast edges create massive amount of trouble, as a result semiconductor switch may actually burns itself and the EMI contaminates the entire power distribution system. The solution is to add a few components to snub these transients, slowing them or diverting them while protecting the power system from interference.(Jennifer Bauman et al ., 2011). In general snubbers used for load line shaping, to reduce switching losses, reduces turn off dv/dt, controllable working current is much greater, device heating is minimized, reduces the peak power and average power dissipate, power dissipation is avoided, reduces voltage transients.

Snubber circuit basically consists of a series connected resistor and capacitor placed in shunt with semiconductor switch. Generally snubbers to slow the rate of rise of this current. Inductor oppose a change of current, so placing an inductor in series with the semiconductor switch as shown in fig 2.1

$$V_L = L\frac{di}{dt} \qquad [1]$$

$$L = \frac{V_L}{\frac{di}{dt}} \qquad [2]$$

So, V_L is the line peak voltage, di/dt is a specification given by the manufacturer.

$$L > \frac{V_{P\ line}}{\frac{di}{dt\ spec}} \qquad [3]$$

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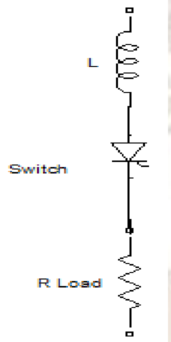

Fig 2.1

Critical rate of rise of voltage

Between main terminal of a semiconductor switch and its gate is a considerable parasitic capacitance as shown in fig 2.2. Any noise on the line is coupled into the semiconductor switch and through this capacitance to the gate; it turns on the semiconductor switch. It is quite possible that the switch can be fired by the noise even without a gating pulse.

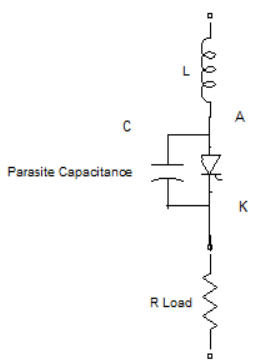

Fig 2.2

To short the noise around the semiconductor switch in a capacitor large enough to divert the energy from the parasitic anode to gate capacitance. As a result we have to choose a capacitor that assures the response to a step is slowed below that critical rate of rise of voltage. Voltage across a snubbing capacitance cannot change instantaneously; instead it rises exponentially as Csnub charges through R load is shown in fig 2.3.

$$C_{snub} = \frac{V_{p\ noise}}{R_{load}} \times \frac{dv}{dt} \qquad [4]$$

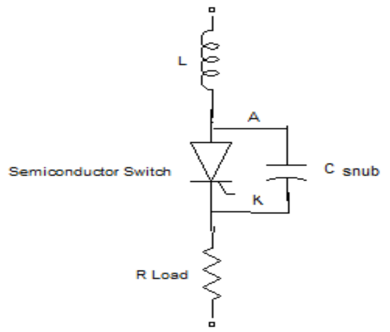

Fig 2.3

For simplicity [7] the value of the snubber resistance and snubber capacitance can be calculated by using the formulae:

$$R = 2.\delta\sqrt{\frac{L}{C}} \qquad [5]$$

and

$$C = L\left(\frac{I_r}{K.V_s}\right)^2 \qquad [6]$$

The values are as follows:

a. Snubber Resistance R_{snub} = 0.4 ohms
b. Snubber Capacitance C_{snub} = 5 µ farads
c. The optimum damping factor δ = 0.4
d. The optimum current factor K = 0.75
e. Recovery current of diode Ir = 20 amps
f. Source voltage is Vs = 230 volts
g. Circuit Inductance L = 1.25 µ Henrys

III. Simulation Results

A basic inverter fed PMBLDC system is simulated using Matlab Simulink. The Simulink model of inverter fed PMBLDC drive system with and without snubber shown in fig 3a and 3b. Here 230V DC is given as input and , the inverter produces three phase voltage required by the PMBLDC motor. The technical specifications of the drive systems are as follows :

Input voltage : 230 V DC
Inverter output voltage : 216.37 V
Pulse width (33%) to Inverter Ideal Switch : 120° mode of operation.
Pulse Amplitude = 5 Volt D.C. and Time period = 0.02 Secs.

Parameters of BLDC Motor

The inverter is a MOSFET bridge.

Stator resistance R_s	:	18.70 ohms
Stator Inductance L_s	:	8.5e-3 Henrys
Flux induced by magnets	:	0.17 Weber's
Inertia	:	$9.68x10^{-3}$
Friction factor	:	$3.24x10^{-3}$
Pole pairs	:	2

Stator windings are connected in star to an internal neutral point.

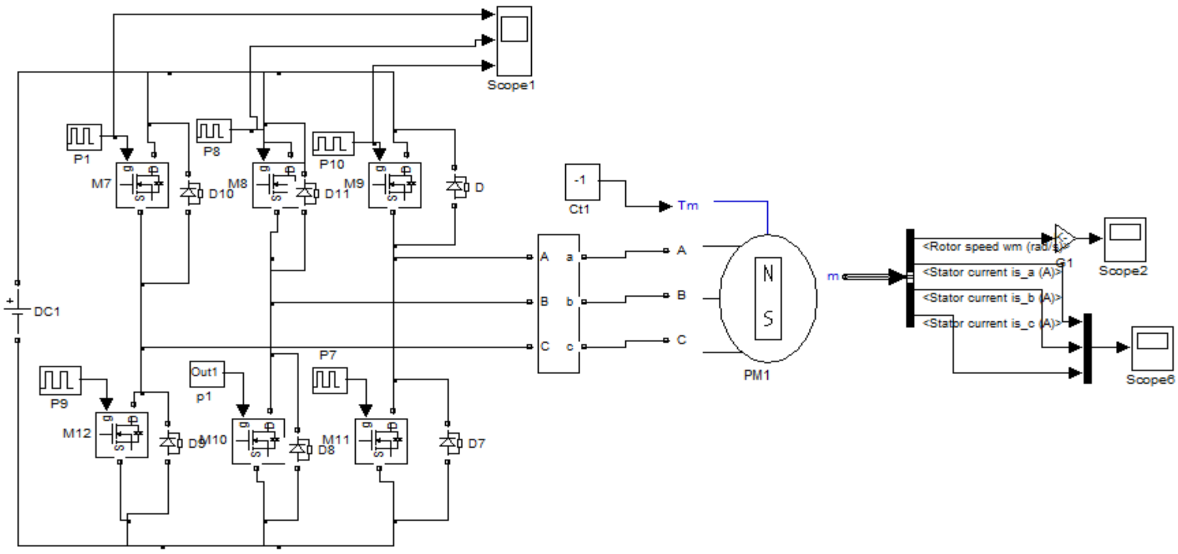

Fig 3a Simulink Diagram of Inverter Fed PMBLDC motor without Snubber.

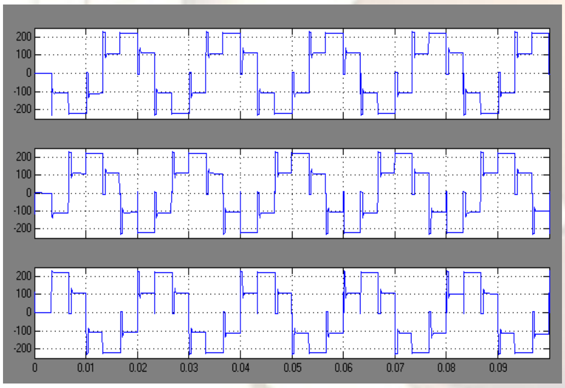

Fig 3b Inverter Output Voltage

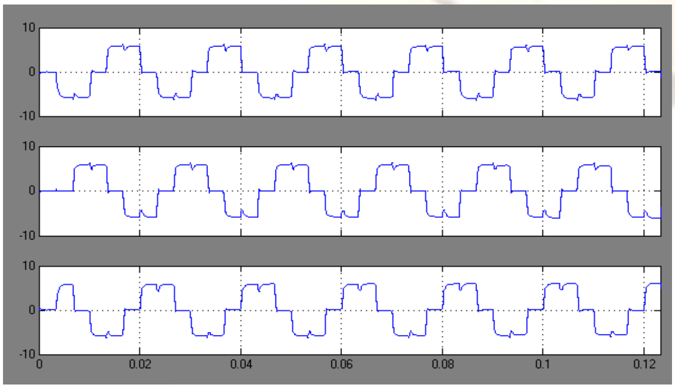

Fig 3c Inverter Output Current

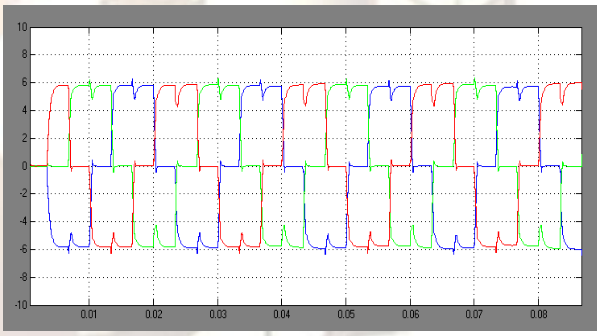

Fig 3d PMBLDC Stator Current

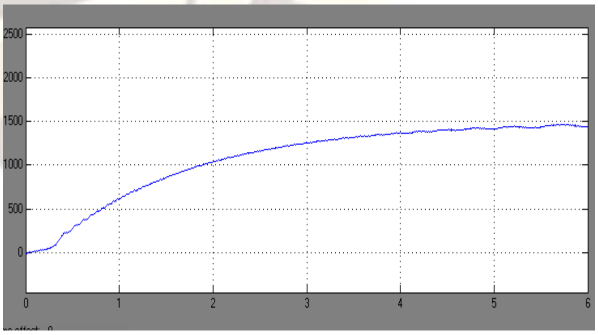

Fig 3e Rotor Speed in rpm

D.C.input voltage given is230V D.C., the inverter output voltage is 216.37. Volts as shown in Fig 3b and the corresponding inverter output current is shown in Fig 3c. Its value is 7.26 amps. The stator current in the PMBLDC motor is shown in Fig 3d.

The response of speed is shown in Fig 3e. The speed oscillates and settles at 940 rpm.

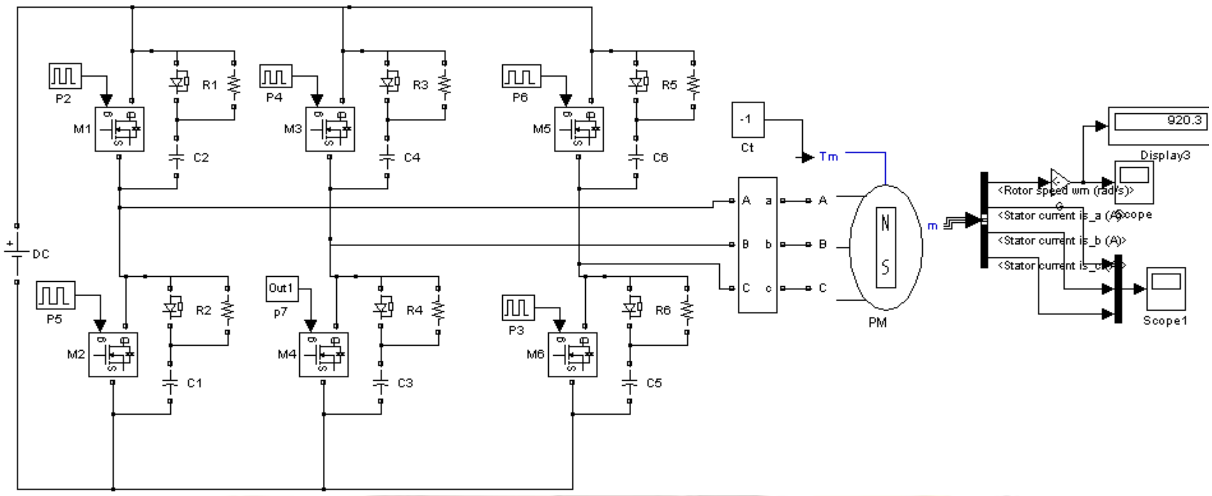

Fig 3f Simulink Diagram of Inverter Fed PMBLDC motor with Snubber.

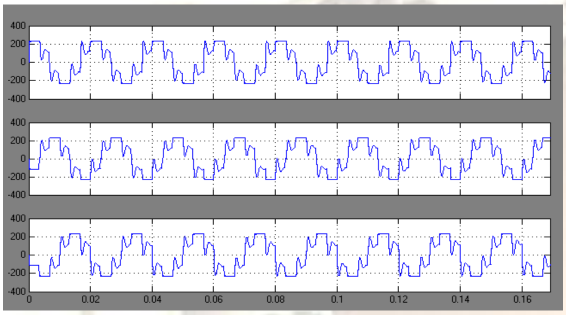

Fig 3g Inverter Output Voltage with snubber

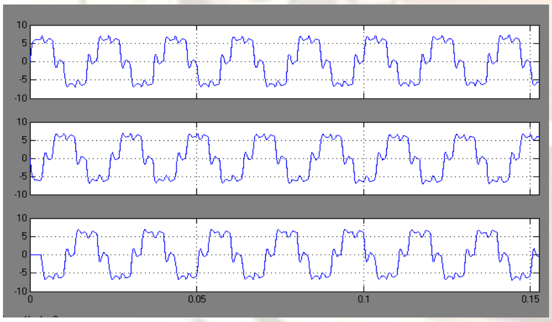

Fig 3h Inverter Output Current with snubber

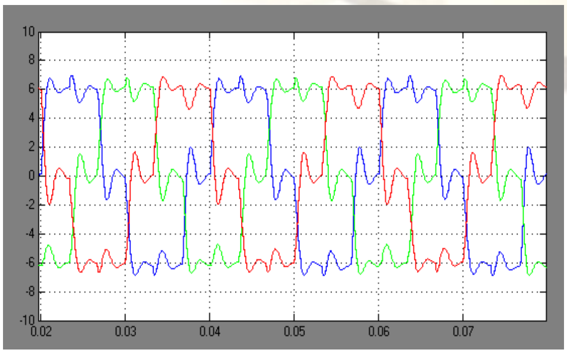

Fig 3i PMBLDC Stator Current with snubber

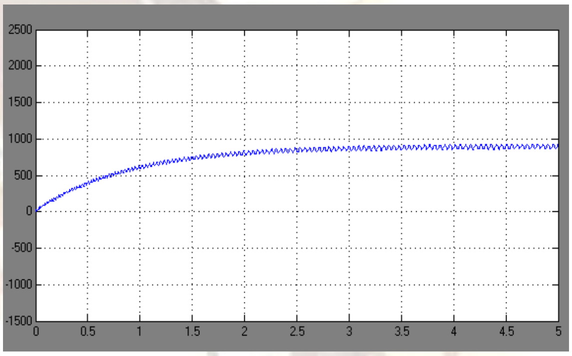

Fig 3j Rotor Speed in rpm with snubber

By taking the ideal switch and inserting the snubber circuit with R of 0.4 ohms and Capacitance C of $5x10^{-6}$ farads, inverter and associated gate circuit are constructed as shown in Fig 3f. The D.C.input voltage given is 230V D.C., the inverter output voltage is 216.37. Volts as shown in Fig 3g and the corresponding inverter output current is shown in Fig 3h. Its value is 7.26 amps. The stator current in the PMBLDC motor is shown in Fig 3i. The response of speed is shown in Fig 3j. The speed settles at 920 rpm.

IV. COMPARISON OF SIMULATION RESULTS

The comparison of the Inverter voltage and current is shown in fig 3k and 3l. The voltage and current waveforms are smoothened. The speed oscillations are reduced by adding snubber.

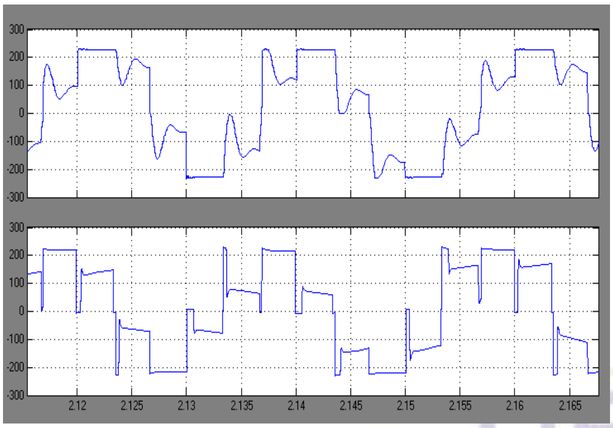

Fig 3k Inverter Output Voltage with Snubber and without Snubber

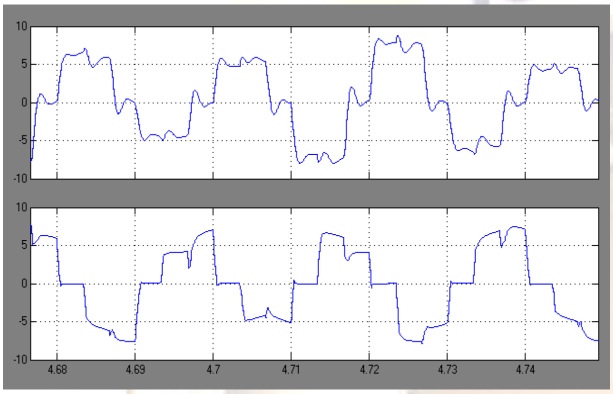

Fig 3l Inverter Output Current with Snubber and without Snubber

V. Conclusion

MATLAB/SIMULINK has been used to simulate the inverter fed PMBLDC drive system with and without snubber and its results are presented. It can be clearly seen that the snubber circuit enables the reduction in the switching stress. The snubber circuit also reduces the ripples in the inverter voltage and current. The greatest advantages are the reduced switching losses and improved response derived due to this drive system. The scope is well defined; it is for modeling and for simulation of inverter fed PMBLDC drive system with and without snubber. However the hardware implementation is yet to be done.

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