Lalit Mishra, Nitin Meena / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 3, Issue 4, Jul-Aug 2013, pp. 462-465

A Novel Approach to Design a High Performance Domino Cmos Logic

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Abstract

In this paper a Domino Cmos logic circuit is design with aim to reduction in power consumption, time delay and energy efficient. Due to rapid growth in VLSI Technology, an integrated circuit has demand with low power, high performance, compatible, small in size and easy to recodify. Dynamic cmos gates are inherently less resistance to noise than static cmosgate. Sothis approach allow low power , noise tolerant and high performance. Domino cmos logic is a form of dynamic logic that gives output in cascaded form and it consume higher dynamic switching speed, leakage power and weaker noise immunity.This design has Simulated and analyzed on 0.12 Microwind2 tool technology .

Keyword – Domino Logic, Dynamic circuit,Delay, Low Power ,Noise Tolerant,

I. Introduction

Due to continuously increasing chips complexity and number of transistors, circuit's power consumption is growing . Technology trends shows that circuit delay is scaling down by 30%, performance and transistor density are doubled approximately every two years, and the transistor's threshold voltage is reduced by almost 15% every generation. These entire technology trend leads to higher and higher power in circuits .Domino logic is a CMOS-based evolution of the dynamic logic techniques which were based on either PMOS or NMOS transistors. It allows a rail-to-rail logic swing. It was developed to speed up circuits.Domino CMOS logic circuit family finds a wide variety of applications in microprocessors, digital signal processors, and dynamic memory due to their high speed and low device count. However, for wide fan in domino logic, that is when there is a long chain of NMOS transistors.(6)

II. Review of Domino logic circuit

The basic dynamic domino logic gate is shown in Fig 1. As shown in the figure, it consists of a pull-down network (PDN) that realizes the desired logic function and there are two switches in series that are periodically operated by the clock signal, *CLK*. *CL* denotes the total parasitic capacitance between the dynamic node and ground. When *CLK* is low, *QP* is turned on, and the circuit is in the precharge phase where the dynamic node charges to *VDD*.

Also, during precharge, the inputs are allowed to change and settle to their proper values. Because *Qe*is off, no path to ground exists. When *CLK* is high, *QP* is off and *Qe*turns on, and the circuit is in the evaluation phase.

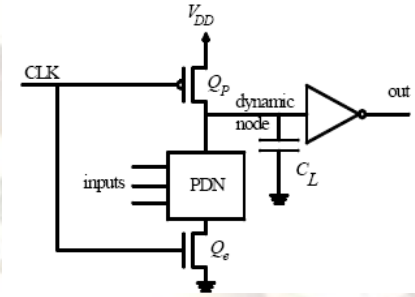

Fig.1. Circuit of domino logic circuit

During the evaluation phase; there are two possibilities for the dynamic-node voltage. If the input combination is one that corresponds to a low output, the dynamic-node voltage must be maintained at the supply voltage, *VDD*. On the other hand, if the input combination is one that corresponds to a high output, the dynamic-node capacitor, *CL* must be discharged to ground through the conducting NMOS transistors of the PDN. The inverter at the output node is put for allowing this stage to be cascaded with another one. Specifically, if the dynamic node of this stage is connected directly to the gate of an NMOS transistor in the PDN of the next stage and is at logic "1", then this transistor will conduct during the time interval from the time of application of this "1" to the time at which the dynamic-node capacitor, *CL* discharges below the threshold voltage of this transistor. This causes the dynamic-node capacitor of the second stage to discharge as it mustn't be. The conventional problem that arises during the evaluation phase is that the leakage current through the PDN of *CL*. Also, the charge of *CL* may be shared with any of the internal capacitors associated with the NMOS transistors of the PDN. So, a PMOS keeper must be used to replenish the lost charge as show in Fig.2. This keeper must be week so that its current during the evaluation phase is relatively small so that the discharging of *CL* will not be slowed down.

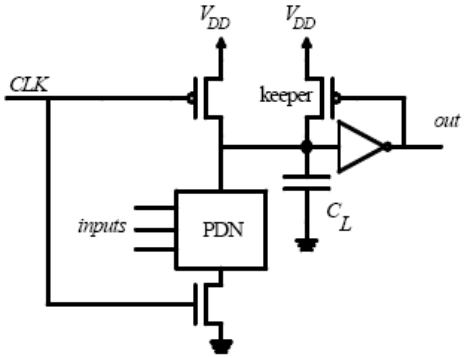

Fig.2. Use of PMOS keeper in domino CMOS

This problem will be more tactile for the case when there is a large number of serially connected NMOS transistors in the PDN. In this case, discharging of *CL* will be very slow due to the keeper contention current.

III. Proposed Domino CMOS circuit

Our proposed technique to speed up the discharging process of the dynamic-node capacitor. The technique uses current mirror of suitable mirroring ratio to achieve the motive and it results in remarkable advances in reducing the time delay as compared to other well known designs

The proposed circuit is designed for two input AND gate with long chain of NMOS transistors and current mirror draws the keeper contention current and speeds up the discharging process.

IV. Working of proposed circuit

The proposed circuit works in following manner that during the precharge phase, Qewill be deactivated, thus the current through the transistor, M1 will be zero. By the effect of the current mirror formed from M1 and M2, the current of M2 will also be zero allowing CL to charge to VDD. During the evaluation phase, the CLK signal will be at logic "1", thus closing the path to ground. If the inputs status is such that there is no current path through the PDN, the current through M1 and M2 will remain zero, thus leaving CL charged at VDD.

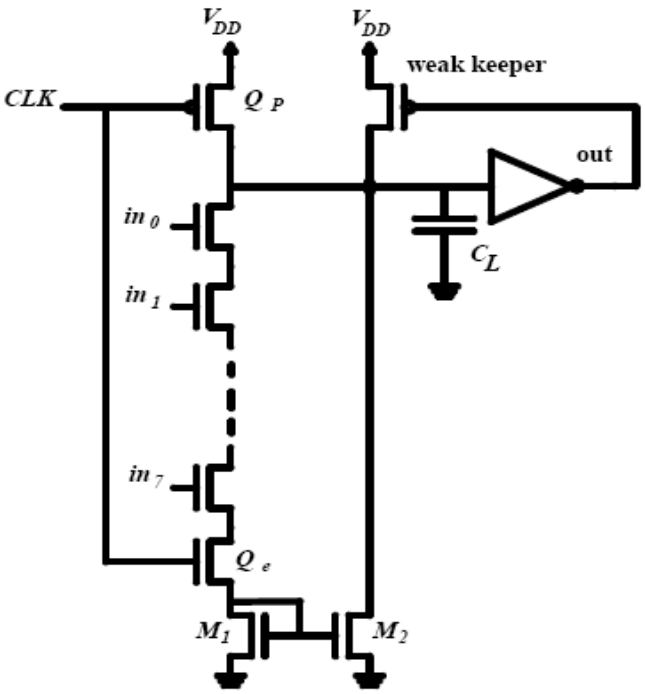

Fig 3 Proposed circuit having current mirror

Likewise, if the inputs status is such that there is a current path through the PDN, the relatively small current through M1 will be mirrored through M2, thus speeding up the discharging process of CL. Increasing the current-mirroring ratio will speed up the discharging process further. The speed improvement gained from this method increases when the number of the series-connected NMOS transistors increases. In case of noise margin, the dynamic-node voltage, VCL will be discharged not to 0 V; instead, it discharges to the threshold voltage of the transistor, M1. So, the threshold voltage of this transistor will be put equal to 0 V. Even if there is an external noise on the gate of this transistor, it will not conduct as the other NMOS transistors of the chain are not conducting.

So for very long chain of series-connected NMOS transistors in the PDN, the discharging current through M1 will be relatively small and will decrease with increasing the number of NMOS transistors in the chain. In such circuits, to obtain a significant increase in speed, the current mirroring ratio, iM2/iM1= (W/L)2/(W/L)1 needs to be increased to a large value, typically 20. Achieving this relatively large current-mirroring ratio by the conventional current mirror will result in an increased capacitance at the gate terminal of M1 and M2, thus slowing down the operation. Also, increasing the current-mirroring ratio to such a large value using the rudimental method causes the dynamic-node capacitance, CL to increase, thus degrading the speed further.

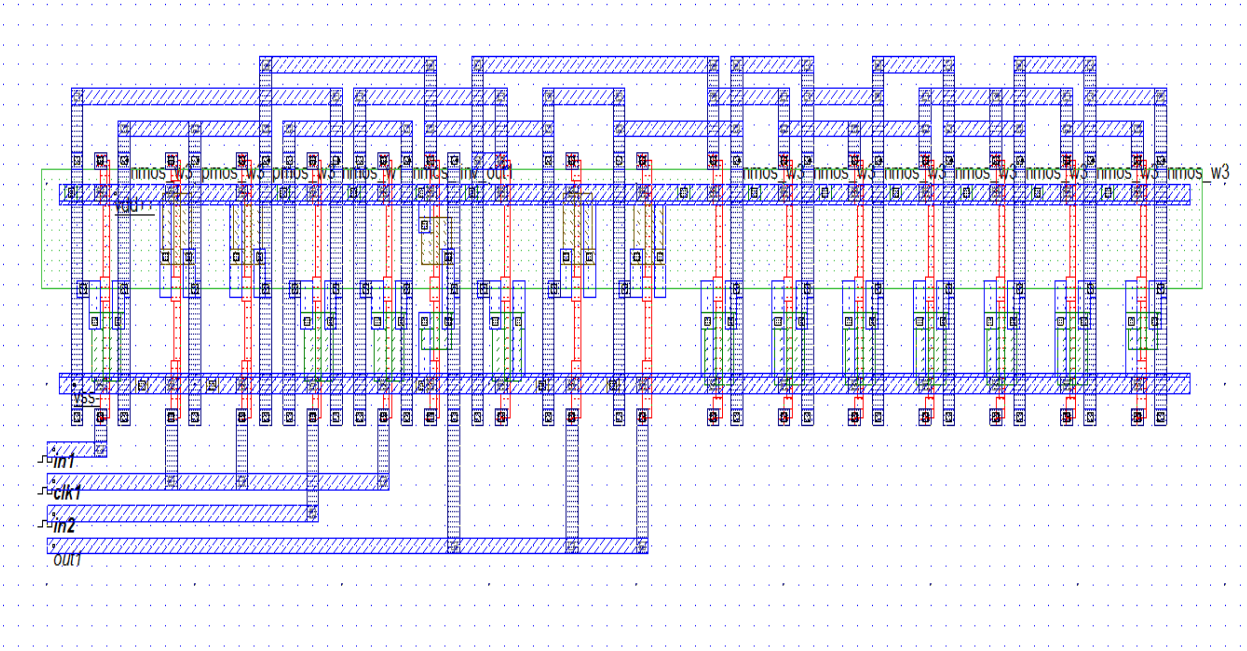

Fig 4 LAYOUT OF Proposed Cicuit

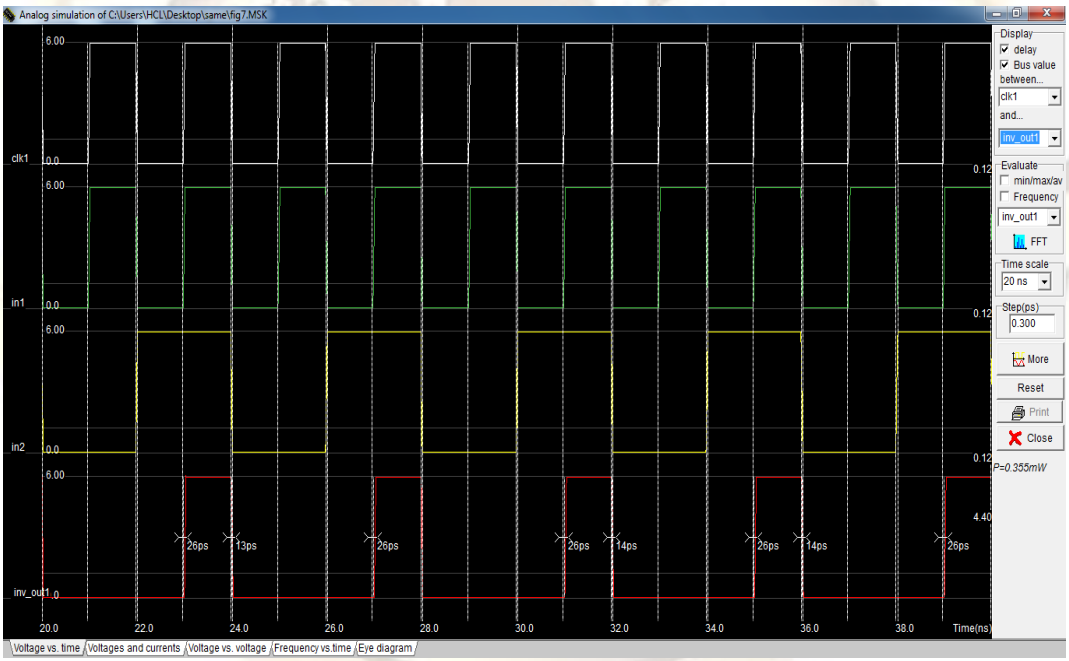

Fig 5 Voltagevs Time Analysis

V. Conclusion

It will be found that the current mirroring ratio, *m* of the current mirror must lie within a certain range so that the discharging process will not be adversely affected by the addition of the current mirror. Domino circuits have offered an improved performance in speed and power when compared with CMOS circuit. This range will be determined quantitatively. The simulation results for comparing the conventional and proposed techniques for the 0.12 µm technology are presented. There are an increasing number of applications that require the use of a large number of NMOS transistors in series in the pull-down network of the CMOS domino logic.

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