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Reduction Of Common Mode Voltage In Ac Drives Using Multilevel Inverter

Jayant M. Parkhi[1], R.K.Dhatrak[2]
[1,2] (Department of Electronics and Power Engg, R.C.E.R.T., Chandrapur

Abstract

In this paper, an approach to reduce common-mode voltage (CMV) at the output of multilevel inverters using a phase opposition disposed (POD) sinusoidal pulse width modulation (SPWM) technique is proposed. The SPWM technique does not require computations therefore, this technique is easy to implement on-line in digital controllers. A good tradeoff between the quality of the output voltage and the magnitude of the CMV is achieved in this paper. This paper realizes the implementation of a POD-SPWM technique to reduce CMV using a five-level diode clamped inverter for a three phase induction motor. Experimental and simulation results demonstrate the feasibility of the proposed technique.

I. INTRODUCTION

Energy saving has never been more important than it is today. In industrialized countries, about 70% of all of the generated electric energy is used by electrical motors. In addition, more than 60% of all the electric energy converted into mechanical energy is consumed by pump and fan drives with induction motors. This fact points out the importance of energy savings in these types of drives. High power pumps and fans need medium-voltage (MV) Drives. At this rating, MV machine designs offer significant cost savings and improvements in the thermal performance of their power components. The switching devices are connected in series to raise the blocking capacity in conventional two-level MV inverters. The simultaneous switching of series connected fast devices generates voltage with a high dv=dt at the output terminal of the inverter. The combination of a short rise time of the inverter output voltage and a long cable are potentially hazardous for the motor insulation and the cable itself. The phenomenon, which is worsened with a shorter rise time, appears on motors as a leakage current. In motor drive applications, this may lead to electromagnetic interference noise that causes a nuisance trip of the inverter drive, problems with the protection scheme of the supply transformer and interference with other electronic equipment in the vicinity [1]. In addition, a conventional two-level inverter based drive faces problems with the CMV. The CMV is responsible for the shaft voltage and the premature failure of the bearings [2]. It is very important to reduce CMV itself or to limit this voltage to within certain bounds. Some approaches have been presented to cope with the CMV issue include four leg inverters, passive filters, passive elements with active circuitry and dual bridge inverters [3]–[6].

A multilevel inverter can reduce as well as eliminate the CMV. Multilevel inverters have a high number of switching states so that the output voltage is stepped in smaller increments. This allows mitigation of the harmonics at low switching frequencies thereby reducing switching losses. Further, the leakage current is reduced because of the lower dv=dt. The H-bridge multilevel inverter presented in literature has been implemented successfully in industrial applications for high power drives. However, the drawback is that these inverters need a large number of dc sources or isolation transformers on the ac side. The diode clamped multilevel structure is more suitable for high and medium voltage drives which are directly connected to the utility power system (direct to drive topology). This topology requires only one ac power supply (with a front end active converter and an inverter at the drive end) therefore; it is very attractive for industrial adjustable speed drives (ASD). The CMV reduction technique is well discussed in many papers using a higher level cascaded H Bridge multilevel inverter and a three-level diode (neutral) clamped inverter.

The application of a five-level diode clamped inverter to reduce common mode voltage using POD-PWM has not been reported in literature.

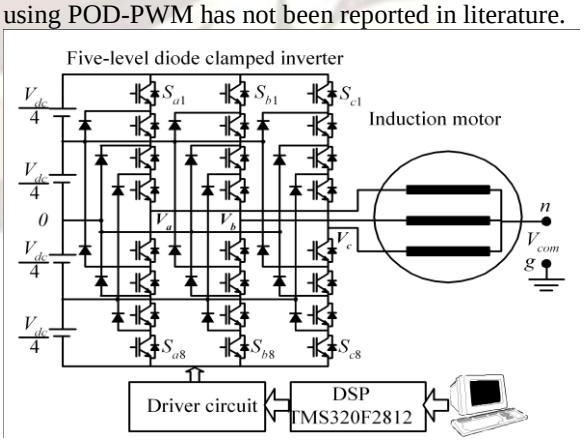


Fig. 1. Five-level diode clamped inverter and induction motor.

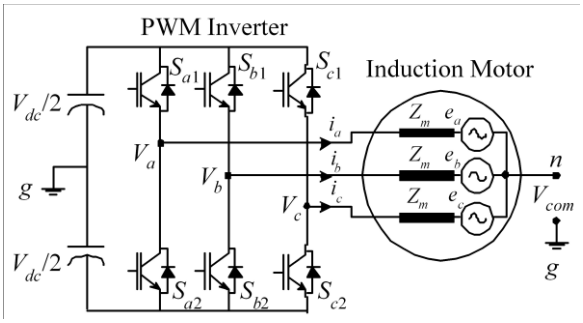


Fig. 2. Three-phase VSI inverter and induction motor.

Recently, several methods to implement SVM for multilevel converters have been presented. These techniques have been successfully used to reduce as well as cancel the CMV. In [7], a five-level inverter is used to eliminate CMV but the levels of the phase voltages of the star connected load are reduced from five to three and the magnitude of the line voltage transition increases.

The same source also reported that the trade off between the magnitude of the CMV and the switching states gives rise to lower order harmonics in the phase voltage. In this paper CMV reduction is proposed using the POD SPWM technique. A five level diode clamped multilevel inverter is fabricated for a three-phase, 3 hp, 400 V induction motor (Fig. 1). Sinusoidal PD-SPWM and PODSPWM techniques are implemented using a Texas Instruments DSP TMS320F2812. For a switching frequency of 1050 Hz and a modulating index, ma =0:9; simulation and experimental results are provided to validate the implement of the five-level diode clamped inverter.

II. COMMON-MODE VOLTAGE

CMV is defined as the voltage at the star point of the load and the system ground. The magnitude of the CMV depends on grounding system. In this paper, CMV is defined with respect to the dc midpoint (Vcom in Fig. 2) because this definition of CMV consists of the well defined edges that are responsible for common mode current.

$$v_{com} = \frac{1}{3}(v_{ag} + v_{bg} + v_{cg})v_{dc} = v_{ng}. \quad (1)$$

Since the VSI cannot provide purely sinusoidal voltages and has discrete output voltages synthesized from the fixed dc bus voltage Vdc, the CMV is always different from zero and

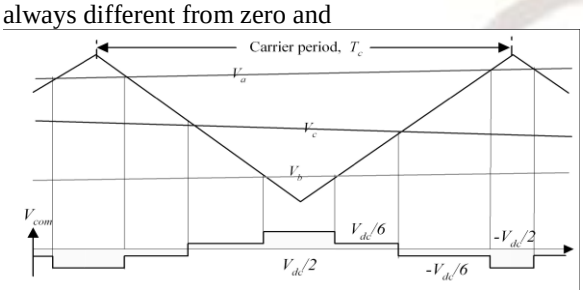
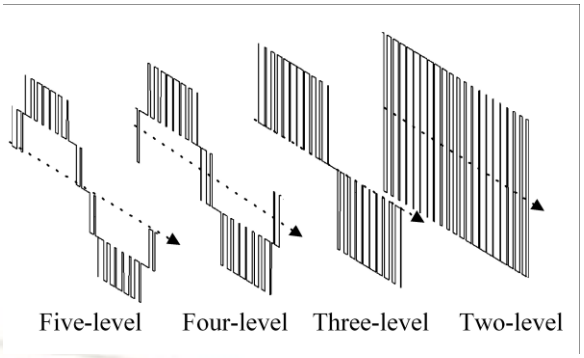


Fig. 3. Reference voltages carrier waveforms and CMV when SPWM applied to two-level inverter.



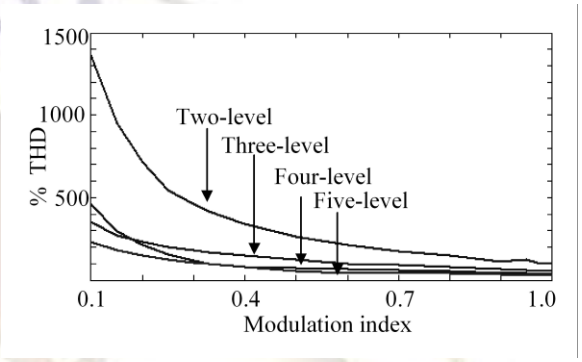


Fig. 4. Output of inverters. (a) Voltage waveform and (b) THD.

may take the values of _Vdc=6 or _Vdc=2, depending on the inverter switch states selected. During the switch state changes,
the CMV changes by _Vdc=3, regardless of the changing states. The CMV transitions are shown in Fig. 3. The change in CMV from -Vdc=2 to -Vdc=6 constitutes step of Vdc=3. When the level changes from -Vdc=6 to Vdc=6, the change is
again Vdc=3.

III. FIVE-LEVEL DIODE CLAMPED INVERTER

The multilevel inverters have become a research hotspot in high-voltage and high-power applications because of their many merits. With the trade off between complexity of implementation and improved performance, multilevel inverters are usually chosen to be between three-level to nine-level [8]. The PWM output voltages of two-, three-, four- and five level inverter are shown in Fig. 4 (a). Fig. 4 (b) shows the THD in the output voltages of these inverters with the SPWM technique for a modulating index of 0.1 to 1.0. The THD in the output voltage of a multilevel inverter decreases as the levels (N) of the output voltage increase.

Medium and high power drives designed for conventional two-level topologies use six switching devices in each pole as shown in Fig. 5(a) [9]. This configuration can be converted into a four-level inverter by simply adding clamping diodes as shown in Fig. 5(b) which reduces voltage equalization circuit as well as the dv=dt of inverter

output voltage. The output voltage of a four-level inverter is shown in Fig. 4 (a). From Eq. (1), the CMV is one third of the summation of the instantaneous voltages in a three phase system. From Eq. (1), the CMV is one third of the summation of the instantaneous voltages in a three phase system. A N-level inverter produces a N-level output voltage and a three phase system has N3 voltage combinations. A two-level inverter has eight voltage combinations without zero common mode voltage [7]. A four level inverter has 64 combinations of three-phase voltage without zero common mode voltage. A five-level inverter has 125 combinations of three-phase voltage. Out of these 125 combinations, only 19 combinations can generate zero CMV. In a four-level three phase inverter, the summation of the instantaneous voltages has a definite value other than zero. Therefore a four-level inverter is unable to eliminate the CMV because zero CMV exists only in multilevel inverters with an odd number of levels. If the circuit is modified to a three-level diode clamped, eight switching devices (two additional) are required in each pole of the inverter (Fig. 5 (c)). Three-level inverters can be fabricated using four devices but in medium voltage drives to achieve the required output voltages of 3.4 kV and 4.16 kV, which means a dc-link voltage above 6.0 kV, the use of three-level technology with existing device ratings is not sufficient, therefore, internal series connection is necessary [10]. A five-level inverter can also be configured using eight switching devices in each pole as shown in Fig. 5(d). This configuration gives the advantages of a low dv=dt, a low harmonics magnitude and a high quality output at a low switching frequency.

The drawback of the additional requirement of a clamping diodes can be justified by eliminating the equalization circuit, the lower magnitude of the harmonics at a low switching frequency, less THD at a low switching frequency, low switching losses, a low dv=dt, a reduced or zero CMV and a smaller size sine filter, dv=dt filter and/or CMV filter. This topology is also suitable for retrofitting. In this paper, a five-level diode clamped multilevel inverter is explored to reduce CMV.

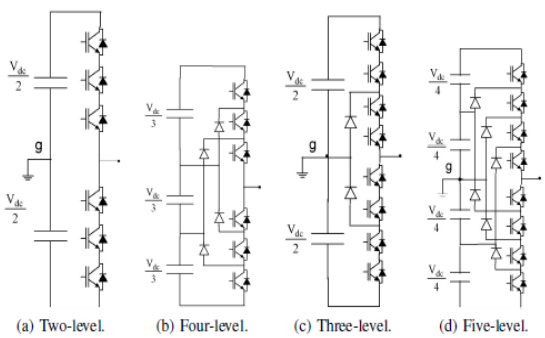


Fig. 5. Inverter configurations.

IV. PROPOSED SYSTEM

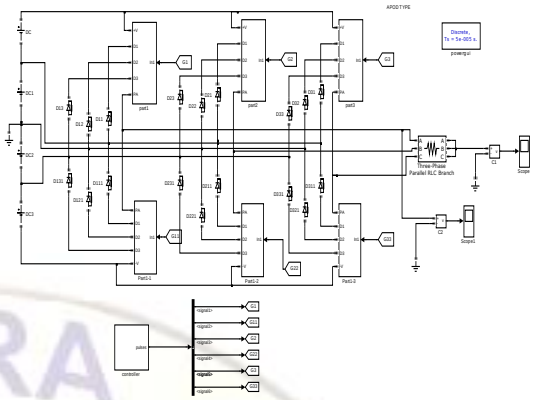


Fig 5.a. Five level diode clamped inverter with resistive load

The diode clamped inverter also known as neutral clamped inverter. The diode clamped inverter delivers the staircase output voltage using several levels of DC voltages developed by DC capacitors. If m is the number of level, then the number of capacitors required on the DC bus are (m-1), the number of power electronic switches per phase are 2(m- 1) and the number of diodes per phase are 2(m-2). This design formula is most common for all the diode clamped multilevel inverters. The DC bus voltage is split into three levels using two capacitors C1 and C2, for five levels using four capacitors C1, C2, C3 and C4 are shown in Fig . 1 and Fig .2. The voltage across each capacitor is $Vd_c/4$ and the voltage stress across each switch is limited to one capacitor voltage through clamping diodes. The switching sequences of three phase 3-level and 5-level diode clamped multilevel inverter are shown in table. I and II. As the number of levels increase the harmonic distortion decreases and efficiency of the inverter increases because of the reduced switching losses. The number of levels in multilevel inverters is limited because of the large number of clamping diodes required. The reverse recovery of these diodes is especially with multicarrier PWM techniques in a high voltage application is a major design challenge.

Multicarrier PWM techniques involves the natural sampling of single modulating reference waveform typically being sinusoidal, through several carrier signals typically being triangular waveforms This modulation method is the logical extension of sine-triangle PWM for multilevel inverters, in which (m-1) carriers are needed for m-level inverter. They are arranged in vertical shifts in continuous bands defined by the levels of the inverter. Each carrier has the same frequency and amplitude. A single voltage reference is compared to the carrier arrangement and the generated pulses are associated to each switching devices.

5.1. Phase Disposition (PD)

This technique involves a number of carriers (m-l) which are all in phase accordingly. In 5 -level inverter all the four carrier waves are in phase with each other and compared with reference signal. According to that, the gate pulses are generated and are associated to each switching devices. The phase disposition PWM technique is illustrated in Fig. 5.1

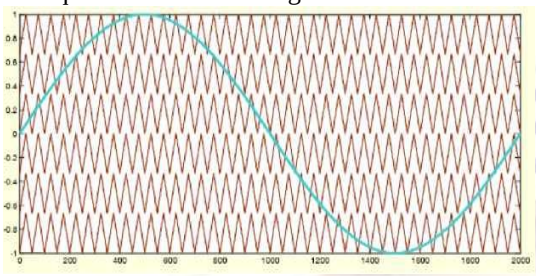


Fig.5.1. Phase disposition PWM technique

5.2. Phase Opposition Disposition (POD)

This technique employs a number of carriers (m-1) which are all in phase above and below the zero reference. In 5-level converters all the four carrier waves are phase shifted by 180 degrees between the ones above and below zero reference. The reference signal is compared with all four carrier waves there by gate pulses are generated and are associated to each switching devices. The phase opposition disposition PWM technique is illustrated in Fig.5.2.

Fig.5.2. Phase opposition disposition PWM technique

5.3. Alternative Phase opposition Disposition (APOD)

This technique requires number of carriers (m-1) which are all phase displaced from each other by 180 degrees alternatively. The alternative phase opposition disposition PWM technique is illustrated in Fig. 5.3

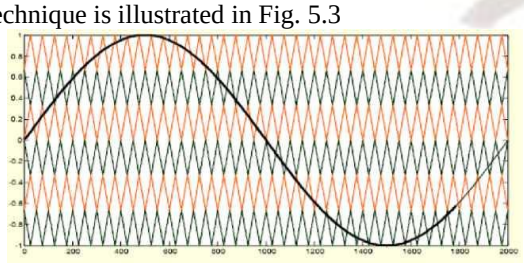


Fig.5.3. Alternative phase opposition disposition.

V. CMV REDUCTION BY POD-SPWM

In this section the POD SPWM technique is discussed to reduce common mode voltage. The multilevel carrier based PWM for a N-level inverter uses a set of N-1 adjacent level triangular carrier waves with the same peak-to-peak amplitude and frequency. Each carrier wave has a distinct dc bias level such that the disposition of all of the waveforms together fit the vertical span of the modulating signal and none of them overlaps each other. As shown in Fig. 9, four carriers are used for a five-level inverter. The modulating/reference waveform is compared with the carrier waveforms and the switching patterns are generated using (2). The minimum step size of the CMV is Vdc/(3(N-1)) with the SPWM technique.

In PD-SPWM, the CMV is reduced in the step of Vdc/12 at the crossing of each reference wave with the rising edge of the carrier signal as shown in Fig. 9. The CMV changes in three steps (maximum) and has four (maximum) distinct CMV levels in a half period of Ts during the rising edge of the carrier waveform. Similarly, the CMV is increased in the step

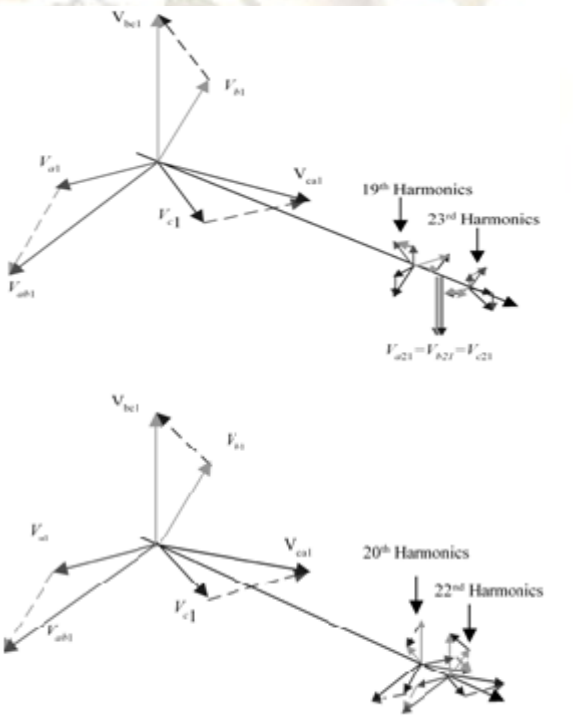


Fig. 8. Three dimensional phasor representation of fundamental and harmonics voltage in three-phase system. (a) PD-SPWM. (b) POD-SPWM.

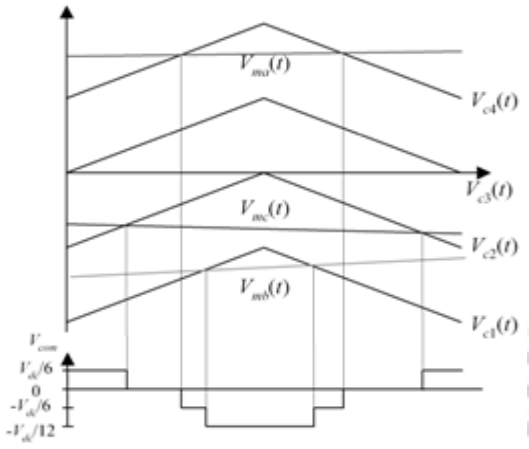


Fig. 9. Reference phase voltages, carrier waveforms and CMV when PD-SPWM is applied switching to five-level inverter.

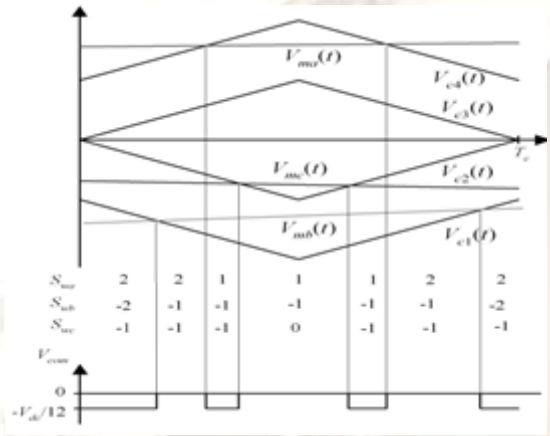


Fig. 10. Reference phase voltages, carrier waveforms and CMV when POD-SPWM is applied to five-level inverter.

of Vdc/12 while crossing the reference wave with the falling edge of the carrier signal. The maximum CMV can be -Vdc/6 at the positive peak of the carrier wave and +Vdc/6 at the negative peak. In a five-level inverter, the maximum CMV with the PD-SPWM technique is observed to be _Vdc/6. It is possible to limit the magnitude of the CMV to _Vdc/12 with POD-SPWM.

In POD-SPWM, in the first half of the carrier wave, the carrier waves have a positive slope (rising edge) above the reference axis where as below the reference axis the carrier waves have a negative slope (falling edge). Similarly, in the second half of the carrier wave, the carrier waves have a falling edge above the reference axis and a rising edge below the reference axis. In a three-phase system, there are three reference signals; therefore, three crossings with the carrier signals are expected in every half cycle of the carrier wave.

In each half cycle of the carrier wave, there are either two crossings above the reference axis and one crossing below the reference axis or one crossing above the reference axis and two crossings below the reference axis. The CMV is reduced in the step of Vdc/12 at the crossing of each reference wave with the rising edge of the carrier signal above the reference axis as shown in Fig. 10 and it is reduced in the step of Vdc/12 at the crossing of each reference wave with the falling edge of the carrier signal below the reference axis. In PD-SPWM, the CMV increases in same direction (positive or negative) at the crossing of the reference wave with the carrier signal in each half cycle of a carrier period. Whereas, in PODSPWM, the CMV has two transitions in one direction and one transition in the other. The CMV varies within the band of (_2Vdc/6) _ (Vdc/6) in POD-SPWM as shown in Fig. 10.

The POD-SPWM technique is implemented for a five-level inverter.

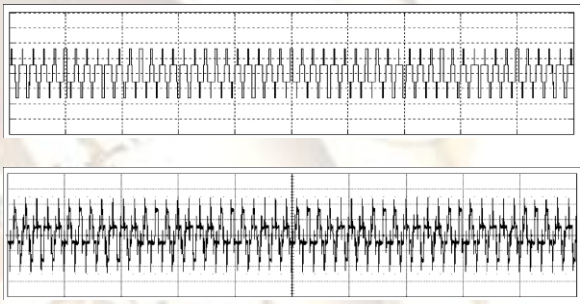


Fig. 11. CMV with two-level inverter: (a) Simulation results. (b) Experimental results. Scale: 200V/div, 5ms/div.

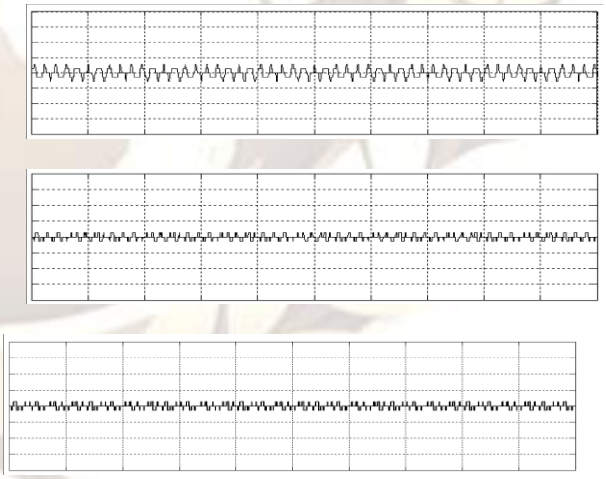


Fig. 12. CMV with five-level inverter: simulation result (a) PD-SPWM technique (b) APOD-SPWM technique (c) POD-SPWM technique. Scale: 200V/div, 5ms/div.

VI. SIMULATION AND XPERIMENTAL RESULTS

Simulation results using MATLAB are provided in this section to verify the concepts and experimental results are provided to confirm the value of the proposed algorithms. A three phase

five-level diode clamped multilevel inverter is fabricated in the laboratory for a three-phase, 400V, 50Hz, 3 hp, star/delta induction motor. The output voltage of each rectifier is 162.5 V. This inverter is controlled by the SPWM technique for ma = 0.9, mf = 21 at 50 Hz using asymmetrical sampling. A DSP TMS320F2812 is used as a controller and it has a 32 bit fix point, 150 MHz processor which performs 150 MIPs. A LeCroyWaveRunner 6030 digital storage oscilloscope (DSO) is used for measurements and analysis. Initially the five-level inverter is operated as a two-level inverter by switching all of the upper switches simultaneously to get a +Vdc/2 voltage at the output terminal and all of the lower four switches are turned on simultaneously to get –Vdc/2

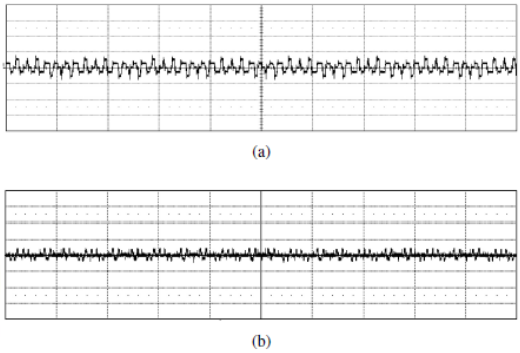


Fig. 13. CMV reduction by with five-level inverter: experimental result (a) PD-SPWM (b) POD-SPWM. Scale: 200V/div, 5ms/div.

TABLE I
COMPARISION OF THD IN POLE VOLTAGE, LINE VOLTAGE AND CMV

SPWM Technique	THD		CMV
	Pole Voltage	line voltage	
PD	24.97%	15.01%	$\pm V_{dc}/6$
POD	24.25%	20.03%	$\pm V_{dc}/12$
APOD	26.24%	24.44%	$\pm V_{dc}/12$

at the output. Multilevel inverters have an inherent ability to reduce common mode voltage. Fig. 11 shows the CMV developed within an induction motor when connected to a five level diode clamped inverter. The inverter is controlled by the PD-SPWM technique with a carrier frequency of 1050 Hz and a modulating index of 0.9. In comparison, the experimental results with a two-level inverter, from Fig. 12, show a significant reduction in the magnitude of CMV and have good agreement with the simulation results. The maximum magnitude of the CMV is found to be within the band of _Vdc/6 as presented in Fig. 12 (a) using the PD-SPWM technique. It changes with a step of Vdc/12. The PD-SPWM technique cannot further reduce the CMV because its switching states are not controllable. The magnitude of the CMV (maximum) is reduced to _Vdc/12 using the APOD-SPWM (Fig. 12.(b)) and POD-SPWM (Fig.12.(c)) techniques. It changes with a step of Vdc/12. However, the THD in the line voltage is higher with the APOD-SPWM technique. Comparisons of the THD in the pole voltage and the line voltage, and the CMV are given in Table I.

Fig. 13 shows the experimental result with the PD-SPWM and POD-SPWM techniques. This is implemented in software without adding any hardware. With the PD-SPWM technique, the CMV changes a maximum of six times with a maximum of seven segments and four discrete levels with two zero voltage levels during a carrier period. The POD-SPWM technique reduces the nonzero CMV levels and increases the zero CMV levels in a carrier period.

VII. CONCLUSION

A conventional two-level inverter generates CMV which is responsible for a leakage current and the premature failure of motor bearings. A multilevel inverter has the inherent ability to reduce CMV. Simulation and experimental results prove that the PD-SPWM technique reduces the magnitude of CMV to Vdc/6 and that it has a minimum THD in the line voltage and current. The POD-SPWM technique further reduces the magnitude of CMV to Vdc/12 at the cost of an increase in the THD in the line voltage and current. A multilevel inverter reduces the dv/dt in its output voltage and therefore the leakage current is also reduced.

REFERENCES

[1] Yoshihiro Murai, Takehiko Kubota, and Yoshiriro Kawase, “Leakage current reduction for a high-frequency carrier inverter feeding an induction motor,” IEEE Trans. Ind. Appl., Vol. 28. No. 4, pp. 858-863, Jul./Aug. 1992.

[2] Doyle F. Busse, Jay M. Erdman, Russel J. Kerkman, David W. Schlegel, and Gray L. Skibinski, “Bearing current and their relationship to PWM drives,” IEEE Trans. Indl. Electron., Vol. 12, No. 2, pp. 243-252, Mar. 1997.

[3] Hirofumi Akagi, and Shunsuke Tamura, “A Passive EMI filter for eliminating both bearing current and ground leakage current from an inverter-driven motor,” IEEE Trans. Power Electron., Vol. 21, No. 5, pp. 982-989, Sep. 2006.

[4] Chenggang Mei, Juan Carlos Balda, and William P. Waite, “Cancellation of common-mode voltages for induction motor drives using active method,” IEEE Trans. Energy Conversion, Vol. 21, No. 2, pp. 380-386, Jun. 2006.

[5] Haoran Zhang, Annette Von Jouanne, and Shaoan Dai, “A reducedswitched dual bridge inverter topology for the mitigation of bearing current, EMI, and dc voltage

variation", IEEE Trans. Ind. Appl., vol. 37. No. 5, pp 1365-1372, Sep./Oct. 2001.

[6] Gopal Mondal, K. Gopakumar, P. N. Tekwani, and Emil Levi, "A reduced-switch-count five-level inverter with common-mode voltage elimination for an open-end winding induction motor drive," IEEE Trans. on Indl. Electron., Vol. 54, No. 4, pp. 2344-2351, Aug. 2007.

[7] M. M. Renge, and H. M. Suryawanshi, "Five-level diode clamped inverter to eliminate common mode voltage and reduce dv=dt in medium voltage rating induction motor drives," IEEE Trans Power Electron., Vol.23, No. 4, pp. 1598-1607, Jul. 2008.