

FPGA Based Digital Controllers for BLDC Motors

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Abstract

Permanent Magnet Brushless DC (PMBLDC) machines have found immense applications in automobile, automation, consumer electronics, medical and industrial applications due to their high efficiency, long operating life ratio of torque delivered to the size and fast dynamic response. In a brushless motor, the rotor incorporates the magnets, and the stator contains the windings. Commutation is implemented electronically with a drive amplifier that uses semiconductor switches to change current in the windings based on rotor position feedback. Commutation is implemented on FPGA as it provides greater flexibility and higher resources for implementing control algorithms. The paper thereby deals with the development of a virtual BLDC motor controller in FPGA. Various other digital controllers are also discussed. A model of the BLDC motor is simulated, and its controller is implemented on a FPGA system.

Keywords- BLDC Digital Controller, FPGA, Virtual motor, Verilog HDL

1.INTRODUCTION

The power electronic converter in the BLDC motor drive system consists of two parts: a front-end rectifier and a three-phase full-bridge inverter as shown in Figure 1. The front-end rectifier is a full-bridge diode rectifier. The inverter is usually responsible for the electronic commutation and current regulation. For the six-step current control with star connected motor winding and no neutral connection, the inverter current flow is restricted two of the three phases. This leads to the DC link current and phase currents always being equal in magnitude.

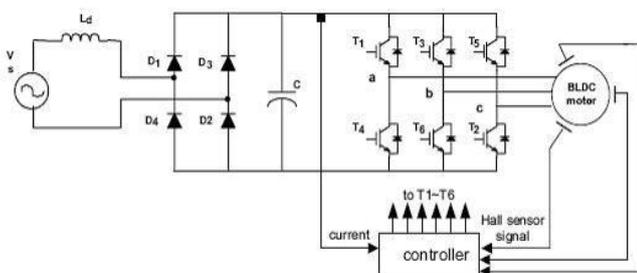


Figure 1: BLDC Motor Control System

The inverter consists of two switches, upper and lower, per leg, which conduct at any moment. Pulse width modulation current controllers are typically used to regulate the actual machine currents in order to match the rectangular current reference waveforms shown in Figure 2.

Each of the upper switches is always chopped for one 120° interval and the corresponding lower switch is always turned on per interval. The freewheeling diodes provide the necessary paths for the currents to circulate when the switches are turned off and during the commutation intervals.

There are two types of sensors for the BLDC drive system: a current sensor and a position sensor. In six-step current control, the dc link current is measured instead of the phase current as they are equal. For current sensor, shunt resistor in series with the inverter, is used. Hall-effect position sensors typically provide the position information needed to synchronize the stator excitation with rotor position in order to produce constant torque. The rotor magnets are used as triggers for the Hall sensor. A TTL-compatible pulse with sharp edges and high noise immunity is produced by signal conditioning circuit for connection to the controller [1].

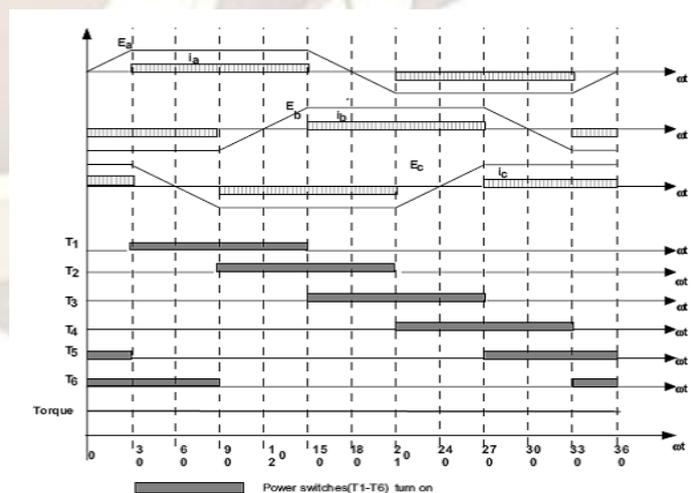


Figure 2: Three phase trapezoidal back EMF

II. BACKGROUND

A. Analog Vs Digital

For the six-step control algorithm, rotor position needs to be detected at only six discrete points in each electric motor drives are traditionally designed with relatively inexpensive analog components. The weakness of analog systems is their susceptibility to temperature variations and component aging. Also analog systems cannot be easily upgraded.

Digital control modules on the other hand, can be easily upgraded through software, and are resilient for temperature drifts. There has been a continuous demand to reduce the control hardware and thus the cost of this drive. There are various controllers like microcontrollers, DSPs, dedicated chips and FPGAs which are used for implementing control logics for speed and position control of BLDC motor. The controller tracks these six points so that the proper switches are turned on or off for the correct intervals. Three Hall-effect sensors, spaced 120 electrical degrees apart, are mounted on the stator frame. Hall sensors produce digital signals which are then used to determine the rotor position and switch gating signals for the inverter switches. The controller of BLDC drive systems reads the current and position feedback, implements the required algorithm, and generates the gate signals [2].

B. Classification of the Digital Control Schemes

A. Microcontroller

Some of the desirable features that a microcontroller must have for PMBLDC control are high speed analog to digital converter (ADC) with sample and hold circuit, capture units, PWM channels with high resolution, timers and interrupts. A high speed ADC with sample and hold circuits are a must for speed control of BLDC machine as the analog current and speed signals have to be converted to digital signals so that they can be processed in the microcontroller. The input capture unit captures the position signals available from the Hall sensor integrated in the motor. The counter mode of the timer is used for velocity measurement. The PWM output channels with good resolution are used for giving triggering pulses to the inverter switches in turn increasing or decreasing the voltage applied to the motor. Interrupt signals are used for detecting the direction change [3].

B. DSP controller

The DSP controllers used for motor speed control has inbuilt features like the capture units for getting position feedbacks, QEP units to sense the speed and ADC units to digitize the current and speed analog signals. Closed loop control is implemented using the event manager units with PWM generators which allow the variation of

voltage applied to the motor in accordance to the required speed [4].

C. Dedicated chip

These chips have functions which are built in for specific purposes. They are designed so as to provide highly reliable and optimized performances. Though manufacturers provide wide arrays of chips, their operations cannot be modified suiting to the user needs. Thereby for the purposes of testing new algorithms they fail miserably. ICs used for speed control have the functions required to implement a full featured motor control system. They contain a rotor position decoder and provide functionalities like open-loop speed control, forward or reverse rotation, run enable and dynamic braking [5].

D. FPGA

A field-programmable gate array (FPGA) is a reconfigurable digital logic platform. Due to its high density of LUTs it supports parallel execution of considerable amount of bit level operations. With an FPGA, calculations that would normally consume large amounts of CPU time are accelerated. The FPGAs have an added advantage of embedded multipliers which allows faster multiply-accumulate operations. FPGA also contains CPU soft core, floating point unit, associated memory subsystems and SPI communication interface. For this paper Xilinx Spartan series FPGA was utilized.

III. PREVIOUS RESEARCH

The present day research is mainly based on motor drives and controllers for PMBLDC. The design by Bogdan Alecsa and Alexandru Onea describes a method to implement a digital BLDC motor speed controller inside an FPGA device [6]. The controller design is a classical PI type implemented using System Generator and Simulink. The work by Alain Cassat, Christophe Espanet, and Nicolas Wavre deals with the computation and modeling of the whole iron losses and thermal behavior analysis of the motor [7]. Design by Jiancheng Fang, Xinxu Zhou, and Gang Liu propose a novel way to control the torque ripple in small inductance motors [8]. W. Hong, W. Lee and B.K. Lee paper proposed an advanced permanent magnet (PM) motor drive modeling for dynamic analysis of automotive control systems with PM motor drives. A multi-level modeling strategy was used, which helps make a compromise between model accuracy and simulation speed without structural modification of the system model. This strategy allowed for a comprehensive analysis of each component and dynamic analysis of the total system [9]. Thomas Schulte and Jörg Bracker presented novel simulation system which enables hardware in-the-loop testing for electronic control

units which drive BLDC motors. It allows testing by connecting the control unit as is, without manipulations. Furthermore it is also suitable for control units which use sensorless control. It was developed to meet the growing importance of BLDC drives in the automotive field where hardware-in-the-loop testing is a standard step in today's development process [10]. Sh. Kazemlou and M.R. Zolghadri discussed direct torque control (DTC) of the induction motor fed by four switch three phase inverter (FSTPI). A modified space vector modulation (SYM) approach with optimal voltage vector sequence was proposed to compensate the effect of de-link voltage variations caused by circulating phase current through the capacitor bank [11]. K. R. Rajagopal and Ajay Nair talk about their development of BLDC motor controller using Texas Instrument F281x series DSP. The DSP controller mimics the hardware counterpart. The drive can be utilized for development of advanced control strategies [12]. A microprocessor based electrical machines control using PWM modulation was implemented by using PMACP16-200 microprocessor for induction motor and results were supported by the experimental setup [13]. Cheng-Tsung Lin, Chung-Wen Hung, and Chih-Wen Liu in 2008 proposed a position sensorless control scheme for four-switch three-phase (FSTP) brushless dc (BLDC) motor drives using a field programmable gate array (FPGA). Using pulse width modulation and sensorless control with six commutation modes FSTP BLDC motor was driven. Due to no hall sensors, reduction in number of switch, a low cost BLDC driver was achieved [14]. In their paper, groundwork for the development of a low-cost IC for control of BLDC motors is discussed using digital PWD control for a trapezoidal BLDC motor drive system. The proposed controller was capable of regulating speed without utilizing an observer under dynamic load conditions. This led to considerable reduction of size and the cost of the system [15]. In Dagbagi, M. And Idkhajine, L. paper, a general framework is presented for effective use of FPGA machine drive modeling when the state-space approach is used. Floating point representation was used and computations were performed using commercial cores. This framework led to that time steps well below 1s [16]. Atef Saleh Othman and Al-Mashakbeh made a study on Proportional Integral and Derivative Control of Brushless DC Motor. Here modelling and simulation of the BLDC motor was done using the software package Matlab/Simulink. A speed controller was designed successfully for closed loop operation of the BLDC motor so that the motor runs close to the reference speed [17]. Albert Rajan and Dr. S. Vasantharathna made a study on a reconfigurable controller for the BLDC motor drive using fuzzy logic technique and minimized

harmonics by varying the switching frequency and duty ratio without affecting the voltage to the drive. The performance of the motor was improved by the controller by reconfiguring the controller using VHDL language for optimal performance [18].

IV. SIMULATION AND RESULT

For the implementation of digital controller, we chose Xilinx Spartan 3E FPGA board. The digital controller algorithm was written using Verilog HDL and was dumped on the FPGA. For this purpose we used Xilinx ISE and iMPACT tools. The digital controller was tested for virtual BLDC motor along with the real one.

A. Virtual Motor Implementation

The virtual motor mimics the characteristics of the real motor and was implemented on another FPGA board. The experimental setup is shown in Figure 3. The output of decoder element, which produces gate pulses based on the hall sensor output are shown in Figure 4. The output of inverter module is shown in Figure 5. The MSB and LSB correspond to sign and magnitude respectively. All the outputs of virtual motor is shown in Figure 6. Utilizing the inbuilt DAC in the FPGA kit, waveforms were observed in an oscilloscope. The waveform showing the inverter phase voltage of all the three phases are shown in Figure 7, back EMFs in Figure 8 and phase currents in Figure 9.



Figure 3. FPGA based virtual motor experimental setup

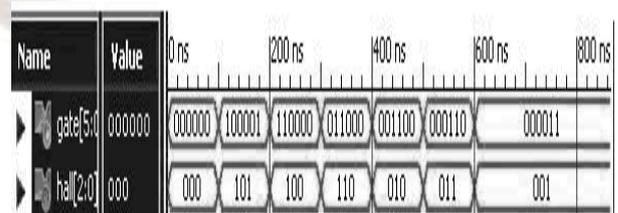


Figure 4. Decoder output.

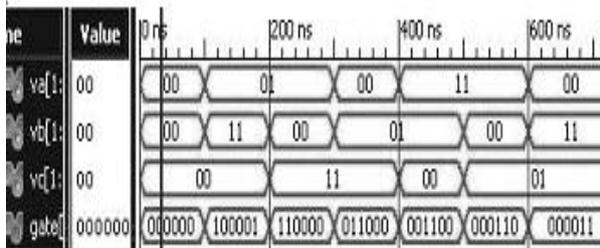


Figure 5. Inverter output

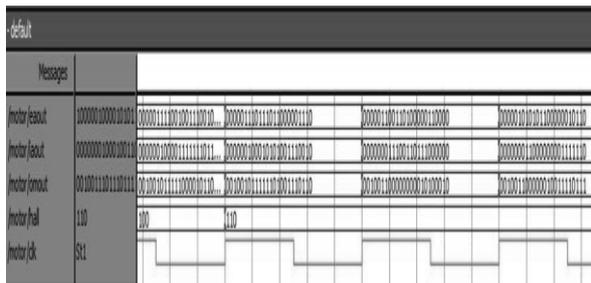


Figure 6. Motor output

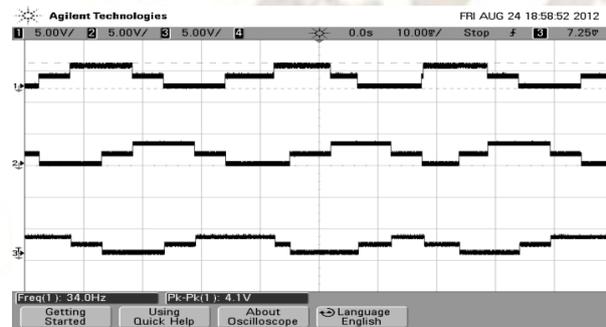


Figure 7. Phase voltage waveform.

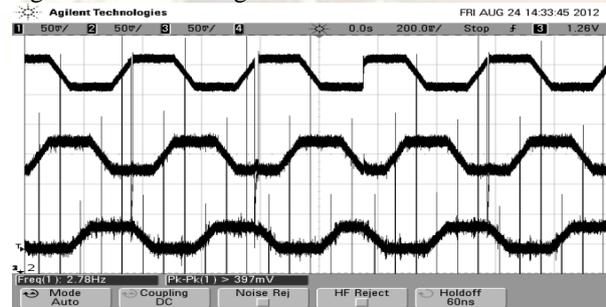


Figure 8. Back emf waveform

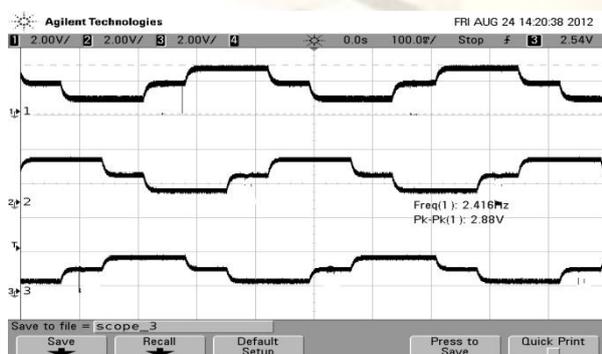


Figure 9. Phase current waveform

B. Hardware Implementation

The experimental setup is as shown in Figure 10. FPGA receives hall sensor output from BLDC motor and generates the gate pulses which drive the IGBT switches. In accordance with the required reference speed, a ramp voltage is generated which is applied to the controller. As the motor rotates, hall sensor signals are produced in accordance with rotor position. Three phase voltages are produced from the gates of IGBT switches after they receive the decoded signals. These voltages are fed as input to the motor and it rotates. The stator currents and three phase voltages are shown in Figure 11 and 12 respectively.

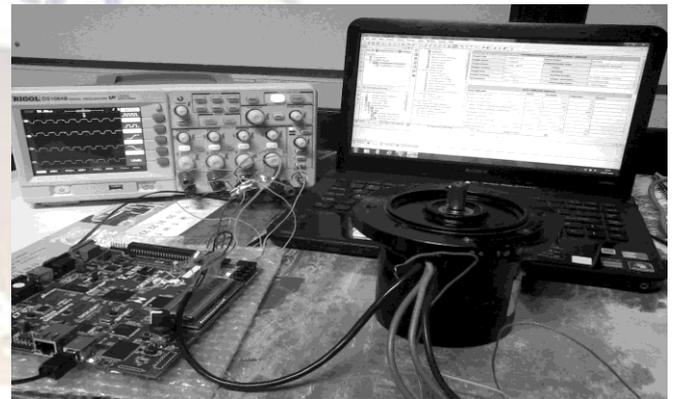


Figure 10. BLDC hardware experimental setup

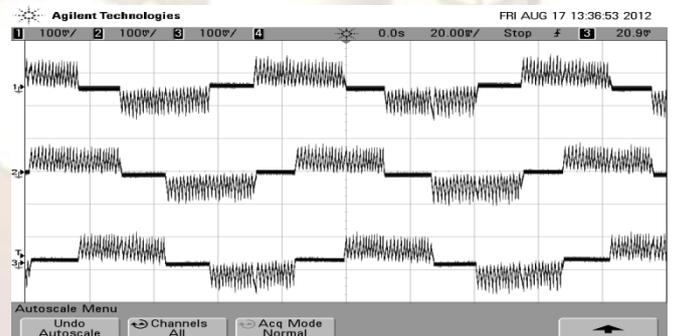


Figure 11. Stator Currents

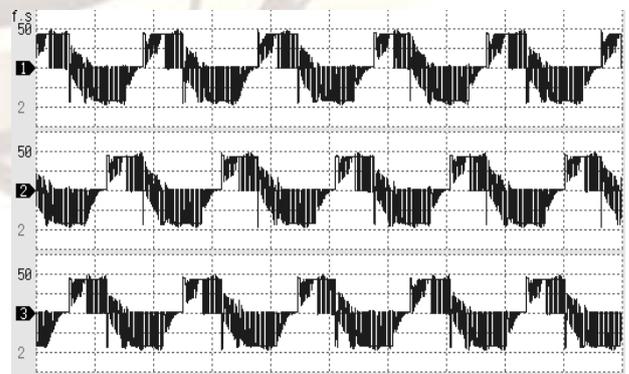


Figure 12. Three phase Line voltages.

V. CONCLUSION

In this paper implementation of digital control algorithm for BLDC motor through FPGA is

discussed. The digital controller works well with real as well as virtual motor. Virtual motor can thereby be utilized for testing the algorithms before implementing on real motors. Using FPGAs gives us flexibility of implementing different algorithms quickly and without complications. Moreover FPGAs are more powerful than microcontrollers and can implement complex algorithms with relative ease.

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