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Area Efficient Parallel Fir Digital Filter Structures Based On Fast Fir Algorithm

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ABSTRACT

Many algorithms are known to reduce the arithmetic complexity of FIR filtering. This paper proposes new parallel FIR filter structures, which are beneficial to symmetric coefficients in terms of the hardware cost, under the condition that the number of taps is a multiple of 2 or 3. The proposed parallel FIR structures exploit the inherent nature of symmetric coefficients reducing half the number of multipliers in sub filter section at the expense of additional adders in preprocessing and post processing blocks. Exchanging multipliers with adders is advantageous because adders weigh less than multipliers in terms of silicon area; in addition, the overhead from the additional adders in preprocessing and post processing blocks stay fixed and do not increase along with the length of the FIR filter, whereas the number of reduced multipliers increases along with the length of the FIR filter.

Index Terms- **Digital Signal Processing (DSP), Fast Finite Impulse Response (FIR) Algorithms (FFA), Parallel FIR, Very Large Scale Integration (VLSI).**

1. INTRODUCTION

Due to the explosive growth of multimedia application, the demand for high performance and low power DSP is getting higher and higher. Most widely used fundamental device performed in DSP system is FIR digital filter. Being the critical part of the theoretical advancement and implementation, FIR filter design continues to be a critical area of on-going research activities. There are many studies which have looked into the hardware simplification requirements.

Many algorithms are known to reduce the arithmetic complexity of FIR filtering. In this paper we have presented a new class of algorithms for FIR filtering in which the multiplications are replaced by adders. We provide new parallel FIR filter structures, based on Fast FIR Algorithm (FFA). It can reduce the amount of multiplications in the sub-filter section. Exchanging multipliers with adders is advantageous because adders weigh less than multipliers in terms of silicon area. This algorithm is very efficient in reducing the hardware cost.

In FIR filters, multipliers play an important role, and in a well-designed CMOS circuit, switching component is a dominant term. Many methods have been reported for the reduction of power dissipation in FIR filter. A multiplier in a FIR filter is most power consuming component and its implementation in VLSI is also very expensive. In our proposing system, exchanging multipliers with adders is advantageous because adders weigh less than multipliers in terms of silicon area.

2. PREVIOUS RESEARCH

There have been a few papers proposing ways to reduce the complexity of parallel FIR filter.

One important research study that demonstrates this was conducted by Jin-Gyun Chung and Keshab K.Parhi, who found that parallel FIR digital filters can be used either for high speed or low power(with reduced supply voltage) applications. Traditional parallel filter implementations cause linear increase in the hardware cost with respect to the block size. The paper makes two contributions. First, the filter spectrum characteristics are exploited to select the best fast filter structures. Second, a novel block filter quantization algorithm is introduced using filter benchmarks; it is shown that the use of the appropriate fast FIR filter structures and the proposed quantization scheme can result in reduction in the number of binary adders up to 20%.

In a research article by Chao Cheng and Keshab K.Parhi, when it comes to symmetric convolutions, the symmetry of coefficients has not been taken into consideration for the design of structures yet, which can lead to significant saving in hardware cost. This paper presents an Iterated Short Convolution (ISC) algorithm based on the mixed Radix algorithm and Fast convolution algorithm. This ISC-based linear convolution structure is transposed to obtain a new hardware efficient fast parallel finite-impulse response (FIR) filter structure, which saves a large amount of hardware cost, especially when the length of the FIR filter is large. For example, for a 576-tap filter, the proposed structure saves 17% to 42% of the multiplications, 17% to 44% of the delay elements, and 3% to 27% of the additions, of those of prior fast parallel

structures, when the level of parallelism varies from 6 to 72.The irregular structures also facilitate automatic hardware implementation of parallel FIR filters.

A similar study was conducted by same Chao Cheng and Keshab K.Parhi who argued low cost parallel FIR filter structures with two stage parallelisms. Based on recently published low-complexity parallel finite-impulse response (FIR) filter structures, this paper proposes a new parallel FIR Filter structure with less hardware complexity. The sub filters in the previous parallel FIR structures are replaced by a second stage parallel FIR filter. The proposed 2-stage parallel FIR filter structures can efficiently reduce the number of required multiplications and additions at the expense of delay elements. For a 32-parallel 1152-tap FIR filter, the proposed structure can save 5184 multiplications (67%), 2612 additions (30%), compared to previous parallel FIR structures, at the expense of 10089 delay elements(-133%). The proposed structures will lead to significant hardware savings because the hardware cost of a delay element is only a small portion of that of a multiplier, not including the savings in the number of additions.

In a research article by Yan Sun and Min Sik Kim they present an approach to implement a high-performance 8-tap digital FIR (Finite Impulse Response) filter using the Logarithmic Number System. In the past, FIR filters were implemented by a conventional number system; their speed was limited because of the multiply-accumulate operations. We realize a fast FIR filter by utilizing the Logarithmic Number System, which allows a simple implementation of multiplication using a fixed-point adder. And the serious demerit of Logarithmic Number System's algorithm, conversions to and from the conventional number representations, is effectively overcome by pipelining to reduce the delay and complexity of the filter. The critical path was reduced from a multiply-accumulate operation to an add operation. Our FIR filter requires 27% less area than the original FIR filter.

In this project we provide new parallel FIR filter structures based on FFA consisting of advantageous poly phase decompositions, which can reduce amounts of multiplications in the sub-filter section by exploiting the inherent nature of the symmetric coefficients, compared to the existing FFA fast parallel FIR filter structure.

3. OVERVIEW OF THE FFA ALGORITHM

With the continuing trends to reduce the chip size and integrates multichip solution into a single chip solution it is important to limit the silicon area required to implement parallel FIR digital filter in VLSI implementation. The Need for high performance and low power digital signal processing is getting increased. Finite Impulse Response (FIR) filters are one of the most widely used fundamental devices performed in DSP system.

3.1 General Form (FFA Algorithm)

Consider an N-tap FIR filter which can be expressed in the general form as

$$Y_n = \sum_{i=0}^{N-1} h_i \, x_{n-i}, \quad n=0,1,2,\ldots,\infty \qquad (1)$$

Where {x (n)} is an infinite-length input sequence and {h (i)} are the length-N FIR filter coefficients.

This block FIR filtering equation shows that the parallel FIR filter can be realized using L^2-FIR filters of length N/L. This linear complexity can be reduced using various FFA structures.

3.2. 2 X 2 FFA (L = 2)

According to polyphase decomposition, a two-parallel FIR filter can be expressed as

$$Y_0 + Z^{-1} = (H_0 + Z^{-1}H_1)(X_0 + Z^{-1}X_1)$$
$$= H_O X_0 + Z^{-1}(H_0 X_1 + H_1 X_0) + Z^{-2} H_1 X_1 \qquad (2)$$

implying that

$$Y_0 = H_0 X_0 + Z^{-2} H_1 X_1$$

$$Y_1 = H_0 X_1 + H_1 X_0 \qquad (3)$$

Equation (4) shows the traditional two-parallel filter structure, which will require four length-N/2 FIR sub filter blocks, two post processing adders, and totally 2N multipliers and 2N-2 adders. However, (4) can be written as

$$Y_0 = H_0 X_0 + Z^{-2} H_1 X_1$$

$$Y_1 = H_{0+1} X_{0+1} - H_0 X_0 - H_1 X_1 \qquad (4)$$

The implementation of (4) will require three FIR sub filter blocks of length N/2, one pre-processing and three post processing adders, and 3N/2 multipliers and 3(N/2-1)+4 adders, which reduces approximately one fourth over the traditional two-parallel filter hardware cost from (3). The two-parallel (L = 2) FIR filter implementation using FFA obtained from (4) is shown in Fig. 1.

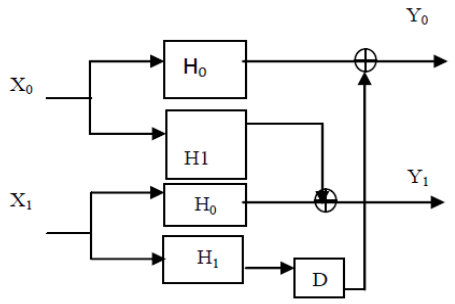

Fig.1 Traditional 2 parallel FIR filter implementation

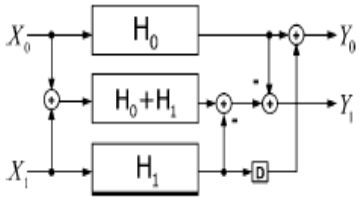

Fig.2 Two parallel FIR implementation using FFA

3.3. 3X3 FFA (L = 3)

By the similar approach, a three-parallel FIR filter using FFA can be expressed as

$$Y_0 = H_0X_0 + Z^{-3}(H_IX_2 + H_2X_1)$$

$$Y_1 = (H_0X_1 + H_1X_0) + Z^{-3}H_2X_2$$

$$Y_2 = H_0X_2 + H_1X_1 + H_2X_0 \qquad (5)$$

The hardware implementation of (5) requires six length-N=3 FIR sub-filter blocks, three pre-processing and seven post processing adders, and three N multipliers and 2N + 4 adders, which has reduced approximately one third over the traditional three-parallel filter hardware cost.

The implementation obtained from (5) is shown in Fig.

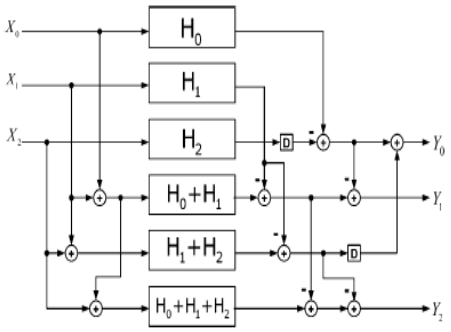

Fig.3 3 parallel FIR filter implementation using FFA

4. PROPOSING FFA ALGORITHM

The main objective of the proposed structures is to earn as many sub-filter blocks as possible which contain symmetric coefficients so that half the number of multiplications in the single sub-filter block can be reused for the multiplications of whole taps, which is similar to the fact that a set of both odd and even symmetric coefficients would only require half the filter length of multiplications in a single FIR filter. Therefore, for an N-tap L-parallel FIR filter the total amount of saved multipliers would be the number of sub-filter blocks that contain symmetric coefficients times half the number of multiplications in a single sub-filter block (N/2L).

4.1 2*2 PROPOSED FFA (L=2)

When it comes to a set of even symmetric coefficients, this can earn one more subfilter block containing symmetric coefficients than (4), the existing FFA parallel FIR filter. Fig. shows implementation of the proposed two-parallel FIR filter.

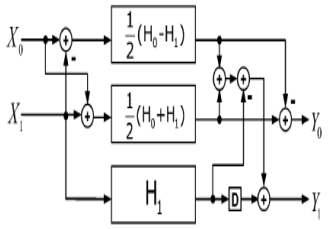

Fig.4 Proposed 2 parallel FIR filter implementation

4.2 3*3 PROPOSED FFA (L=3):

With the similar approach, from (6), a three-parallel FIR filter can also be written as (9). Fig. shows implementation of the proposed three-parallel FIR filter.

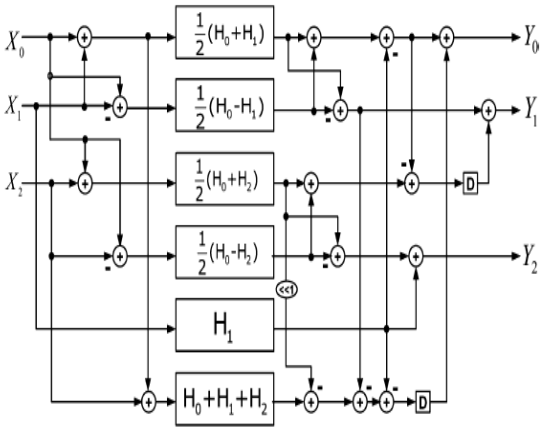

Fig.5 Proposed 3-parallel FIR implementation

When the number of symmetric coefficients N is the multiple of 3, the proposed three-parallel FIR filter structure presented in (9) enables four subfilter blocks with symmetric coefficients in total, whereas the existing FFA parallel FIR filter structure has only two ones out of six subfilter blocks. A comparison figure is shown in Fig. 6, where the shadow blocks stand for the subfilter blocks which contain symmetric coefficients. Therefore, for an N-tap three-parallel FIR filter, the proposed structure can save N/3 multipliers from the existing FFA structure. However, again, the proposed three-parallel FIR structure also brings an overhead of seven additional adders in pre-processing and post processing blocks.

5. Complexity Analysis And Comparison:

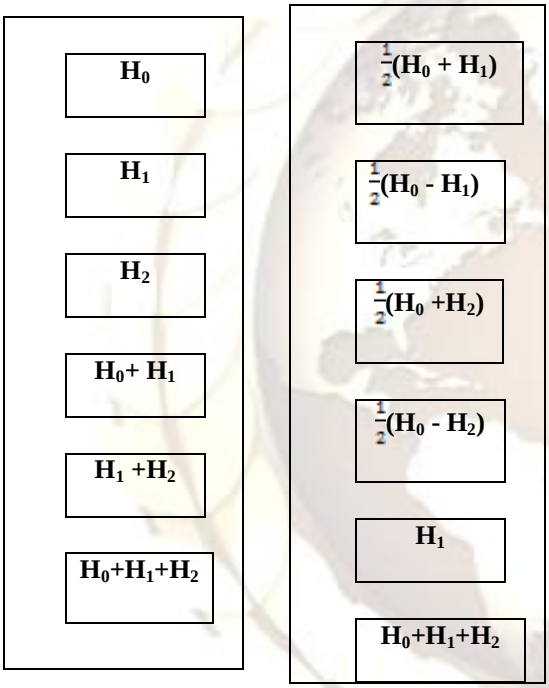

Fig.6 comparison of sub filter blocks between existing FFA and proposed FFA 3-Parallel FIR structures

Fig. 6 shows the comparison of subfilter blocks between FFA and proposed FFA structures. The number of subfilter blocks didn't increase in our new approach.

5.2 Comparison of proposed and existing FFA structures

Length		24-tap	72-tap	144tap
Multipliers	FFA	30	90	180
	Proposed	24	72	144
	Reduced multiplier	6	18	36
Adders	FFA	4	4	4
	Proposed	6	6	6
	Increased adders	2	2	2

Table 1: for L=2

Length		24-tap	72-tap	144tap
Multipliers	FFA	40	120	240
	Proposed	32	96	192
	Reduced multiplier	8	24	48
Adders	FFA	10	10	10
	Proposed	17	17	17
	Increased adders	7	7	7

Table 2: for L=3

Length		24-tap	72-tap	144tap
Multipliers	FFA	51	153	306
	Proposed	42	126	252
	Reduced multiplier	9	27	54
Adders	FFA	20	20	20
	Proposed	31	31	31
	Increased adders	11	11	11

Table 3: for L=4

Table 1,2,3 shows the comparison between the proposed and existing FFA structures. The additional adders in preprocessing and postprocessing blocks stay fixed and do not increase along with the length of the FIR filter.

5.3 Implementation And Result

We are implementing the proposed FFA structures and the existing FFA structures in Verilog HDL. Table shows the result interms of preprocessing and post processing adders and interms of area and power.

Length	Structure	Area		
		L=2	L=3	L=4
24-Tap	FFA	22726	34467	39629
	Proposed	22356	34255	38984
72-Tap	FFA	226702	299815	366798
	Proposed	201901	273491	334168

Table 4: Comparison of Area

Length	Structure	Power (mW)		
		L=2	L=3	L=4
24-Tap	FFA	9.6	10.1	16.01
	Proposed	9.74	14.34	14.92
72-Tap	FFA	129.59	163.01	197.63
	Proposed	108.94	127.24	169.97

Table 5: Comparison of Power

6. CONCLUSION

In this paper, we have presented new parallel FIR filter structures, which are beneficial to symmetric convolutions when the number of taps is the multiple of 2 or 3. Multipliers are the major portions in hardware consumption for the parallel FIR filter implementation. The proposed new structure exploits the nature of even symmetric coefficients and save a significant amount of multipliers at the expense of additional adders. Since multipliers outweigh adders in hardware cost, it is profitable to exchange multipliers with adders. Moreover, the number of increased adders stays still when the length of FIR filter becomes large, whereas the number of reduced multipliers increases along with the length of FIR filter. Consequently, the larger the length of FIR filters is, the more the proposed structures can save from the existing FFA structures, with respect to the hardware cost. Overall, in this paper, we have provided new parallel FIR structures consisting of advantageous polyphase decompositions dealing with symmetric convolutions comparatively better than the existing FFA structures in terms of hardware consumption.

7. ACKNOWLEDGMENT

Apart from our efforts, the success of our work depends largely on the encouragement and guidelines of many others. We take this opportunity to express our gratitude to the people who has been instrumental in the successful completion of this work. We would like to extend our sincere thanks to all of them. We owe a sincere prayer to the LORD ALMIGHTY for his kind blessing and giving us full support to do this work, without which this would have not been possible. We wish to take this opportunity to express our gratitude to all, who helped us directly or indirectly to complete this work.

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