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# Dynamic Random Access Memory with Self-controllable Voltage Level to reduce low leakage current in VLSI

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**Abstract –**

**Today trend is circuit characterized by reliability, low power dissipation, low leakage current, low cost and there is required to reduce each of these. To reduce device size and increasing chip density have increase the design complexity. The memories have provided the system designer with components of considerable capability and extensive application. Dynamic random access memory (DRAM) gives the advantage for high-density data storage. DRAM basically a memory array with individual bit access refers to memory with both Read and Write capabilities. Here 3T DRAM is implementing with self controllable voltage level (svl) technique is for reducing leakage current in 0.12um technology. The simulation is done by using microwind 3.1 & dsch2 and gives the advantage of reducing the leakage current up to 57%.**

***Keywords* – low leakage power, high performance, self controllable voltage level technique, low cost, low power.**

## I. Introduction

DRAM designers have opted for a multiplexed addressing scheme. In this model the lower and upper halves of the address words are presented sequentially on a single address bus. This approach reduces the number of package pin and has survived through the subsequent memory generation. DRAMS are generally produced in higher volumes. Lowering the pin count reduces the cost and size at the expense of performance. The presence of new address word is asserted by raising a number of strobe signals. Raising the row access strobe signal assert the MSB part of the address is present on the address bus, and that word decoding process cam be initiated. The LSB part of the address is applied next and the column access strobe signal is asserted .To ensuring the correct memory operation a careful timing of the signal interval is necessary. Basically the signals are used as a clock input to the memory module and are used to synchronize memory event such as decoding memory core access and sensing. DRAM (Dynamic Random Access Memory) must be refreshed periodically. It's a Volatile in nature means loses data when power is removed. DRAM requires more peripheral circuitry. In 1T DRAM Cell with a single access NMOS and storage capacitor and control input like word line (WL), data I/O, bit line. Number of activity in DRAM like a Random read/write operation possible, Small cell area compared to SRAM, Highly integrated, Very low production cost, Widely used for main memory, Stored data is volatile, Cyclic refresh necessary, Medium speed. Dynamic random access memory (DRAM) is the most common kind of random access memory (RAM) for personal computers and workstations. The network of electrically-charged points in which a computer stores quickly accessible data in the form of' 0's and '1's is called memory. Random access means that the PC processor can access any part of the memory directly rather than having to proceed sequentially from some starting place. DRAM is dynamic in that, unlike static RAM (SRAM), it needs to have its storage cells refreshed or given a new electronic charge every few milliseconds. that DRAM is much cheaper per storage cell and because each storage cell is very simple, DRAM has much greater capacity per unit of surface than SRAM.

In this research paper implementing the 3T DRAM with Self-controllable Voltage Level technique. In the implementation of 3T DRAM using three NMOS M1, M2 and M3. M1 and M3 are the access transistor and by using these control the read and write operation. If the write operation is performed in that time M1 is on and M3 is off. The data is stored by charging the capacitor. If the read operation is performed in that time M1 is off and M3 is on, than the data is also available in that time also. When the 3T DRAM is implementing with Self-controllable Voltage Level technique one inverter is used in the upper part and the lower part. If we add this inverter in the circuit then the leakage power is less as compared to conventional 3T DRAM.. By using microwind 3.1 software, layout diagram have done. In this the word and VDD lines are implemented in poly, the connection to the MOSFETs occurs when poly runs over the active n+ area. The bit line is implemented in metal1 and metal2. The PMOS is implemented by using P+ diffusion layer and the NMOS is implemented by using n+ diffusion layer.

## II. History of work

Most of the works in leakage current analysis and reduction have stressed in a combinatorial circuits and sequential circuit. Memory circuits need more attention to design if leakage

current is there. Various gate leakage reduction methodologies have been described in the literature such W. K. Luk et. al. gives a A Novel Dynamic Memory Cell With Internal Voltage Gain[1]. H. J. Yoo et. al. have developed A low voltage high speed self-timed CMOS logic for the multi-gigabit synchronous DRAM application[2]. JOHN E. et al give the idea of dram Design Using the Taper-Isolated Dynamic RAM Cell [3]. G. W. Taylor et al have developed A punch-through isolated RAM cell [4] .the idea about Leakage Model Including Source-Drain Partition shown in [5]. Power Dissipation Analysis and Optimization for Deep Submicron CMOS Digital Circuits shown in [6]. The basic Fundamentals of Modern VLSI Devices [7] and Principles of CMOS VLSI Design [8] have developed. The device design guidelines for floating channel type surrounding gate transistor (FC-SGT) DRAM cells with high soft-error immunity described in this [9]. The three structure studied, only SSMSL is a viable for the 0.6pm -pitch isolation of 256Mbit DRAM [10]. Two leakage control transistors (a p-type and a n-type) within the logic gate for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other shown in [11]. Transient effects of the floating body must be considered when designing for long data retention time [12]**.** The use of the minimum idle time parameter, as a metric for evaluating different leakage control mechanisms, is shown [13]**.** The experimental and simulation data of GIDL current as a function of 0.35-µm CMOS technology parameters and layout of CMOS standard cells is shown [14]. The CMOS leakage current at the process level can be decreased by some implement on deep sub micron method shown [15].

## III. Proposed work

Dynamic random access memory (DRAM) is a type of random-access memory that stores each bit of data in a separate capacitor within an integrated circuit. The capacitor can be either charged or discharged; these two states are taken to represent the two values of a bit, conventionally called ‘0’ and ‘1’. Since capacitors leak charge, the information eventually fades unless the capacitor charge is refreshed periodically. Because of this refresh requirement, it is a dynamic memory as opposed to SRAM and other static memory. The main memory (the "RAM") in personal computers is dynamic RAM (DRAM). It is also used in the laptop and workstation computers as well as video game.

### *A.* 3T Dynamic memory cell

The cell is written to by placing the appropriate data value on BL1 and asserting the write word line (wwl) . The data is retained as charge on the capacitance once wwl is lowered. When reading the cell the read word line RWL is raised. The storage transistor M2 is either ON or OFF depending upon the stored value. The bit line BL2 is either clamped to vdd with the aid of load device.
The former approach necessitates careful transistor sizing and causes static power consumption. Therefore the pre charged approach is generally preferable. The series connection of M2 and M3 pulls BL2 low when a 1 is stored. BL2 remains high in opposite case.

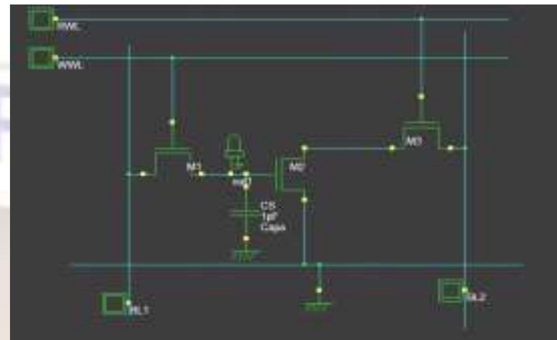


Figure 1 shows schematic of 3T DRAM

The inverse value of the stored signal is sensed on the bit line. the most common approach to refreshing the cells to read the stored data ,put its inverse on bit line 1(BL1) and assert write word line(WWL) in consecutive order.
Figure 1 shows the circuit diagram of the 3T DRAM. In this used a three NMOS transistor. M1 and M3 are access transistor.
Layout diagram of 3T DRAM shown in figure 2 in this n+ diffusion layer, polysilicon , metal1 and metal2 is used. Figure 3 shows a waveform of 3T DRAM voltage versus time. In this when write operation performed, output is high. When read operation performed, output is not affected.
When read operation is performed in that time write word line is low and when write operation is performed read word line is low. Bit line is high means you get data which you want. Bit line 1 used for write operation and bit line 2 help the read operation.
Leakage current analysis of 3T DRAM shown in figure 4. The leakage current is about 0.164ma.

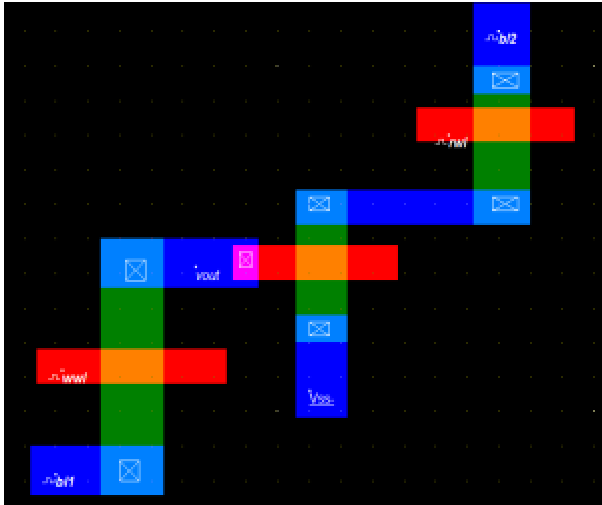


Figure 2 shows a layout of 3T DRAM

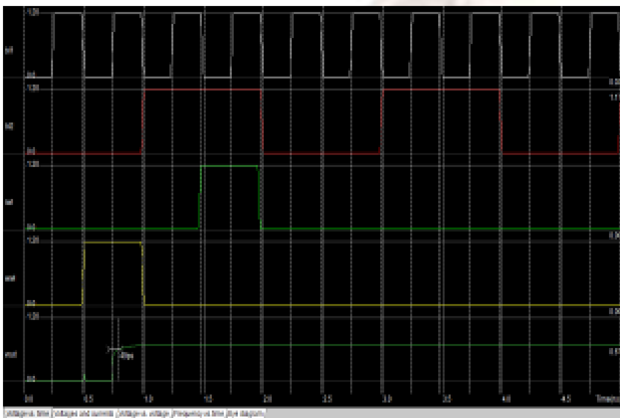

Figure 3 shows a waveform of 3T DRAM voltage versus time

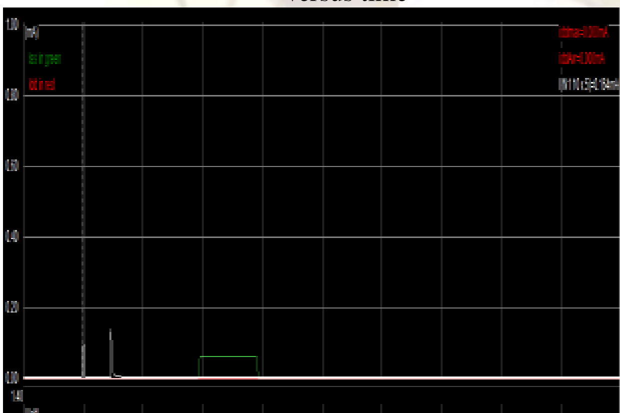

Figure 4 shows the leakage current waveform of 3T DRAM

The SVL circuit consists of an upper SVL (U-SVL) circuit and a lower SVL (L-SVL) circuit where a single inverter has been used as the load circuit. The SVL circuit is applied to the 3T DRAM memory cell. Figure 5 shows the circuit diagram of the 3T DRAM with self controllable voltage level (svl). In this used a three NMOS transistor. M1 and M3 are access transistor. Lower self controllable voltage level is implementing by using NMOS and PMOS .the upper self controllable voltage level is implementing by using a NMOS and PMOS. Write word line (wwl) is high when written operation is performed. Read word line (rwl) is performed when operation read is performed. Layout diagram of the 3T DRAM with self controllable voltage level (svl) shown in figure 6, in this n+ diffusion layer, p+ diffusion layer , polysilicon, metal1 and metal2 is used. Gate is implemented by using polysilicon and source and drain is implemented by n+ diffusion and metal1. by using metal 2 connection is done. VDD is also done by metal 1 and VSS gives in metal1. PC1 and PC2 input gives to the polysilicon .

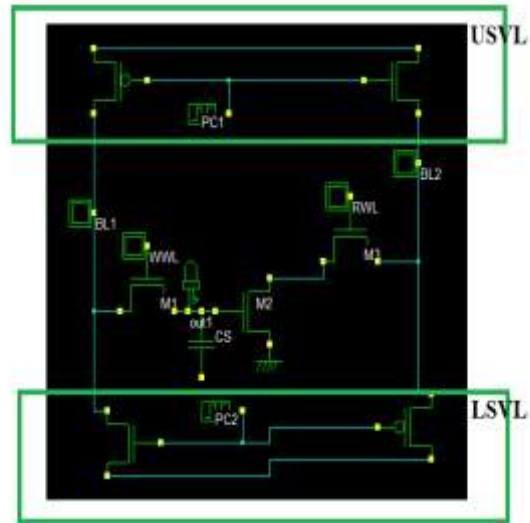


Figure 5 shows schematic of 3T DRAM with self controllable voltage level

Figure 7 shows a waveform of 3T DRAM with self controllable voltage level in which write operation is performed when write word line is high and output is not affected by read operation.

Leakage current analysis of the 3T DRAM with self controllable voltage level (svl) shown in figure 8. The leakage current is about 0.071ma. the peak current is shown in figure 8.

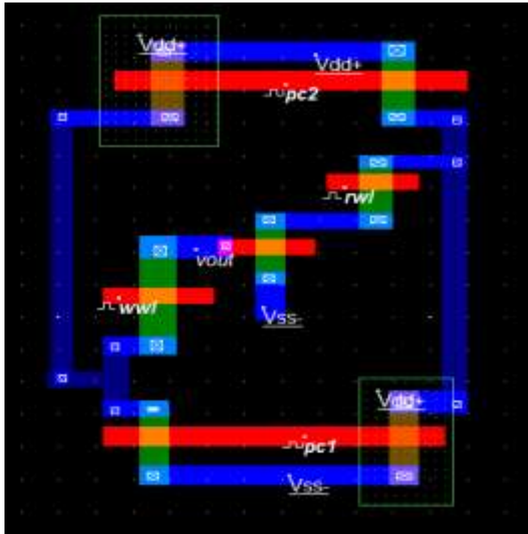


Figure 6 shows a layout of 3T DRAM with self controllable voltage level

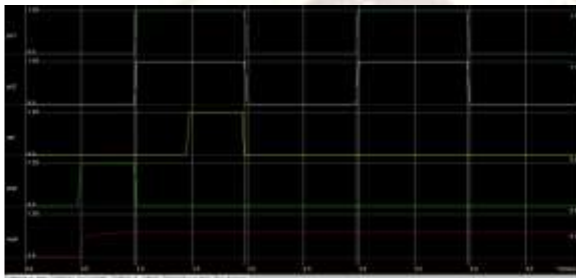

Figure 7 shows a waveform of 3T DRAM with self controllable voltage level

Figure 8 shows the leakage current waveform of 3T DRAM with self controllable voltage level

## IV. Circuit simulation result

In this research paper self controllable voltage level is used to implement the 3T DRAM and simulation is done by using a microwind 3.1 and DSCH 2. Table – I shows the parameter of 3T DRAM. table – II shows the simulation of 3T DRAM with self controllable voltage level.

Table –I Parameter of 3T DRAM

| *Process technology* | *0.12um* |
|---|---|
| Power supply voltage | 1.2v |
| Pre charge voltage | 1v |

Table –II Simulation result of SVL based 3T DRAM

| *Circuit* | *Leakage current* |
|---|---|
| 3T dram during write operation | 0.164ma |
| 3T DRAM with SVL | 0.071ma |

## V. Conclusions

In this work we presented a 3T DRAM with self controllable voltage level. To implement 3T DRAM with self controllable voltage level gives the advantageous of reduction up to 57%. The layout of Simulation is done by using a microwind 3.1. VDD is used in this 1.2v. here 0.12µm technology is used.

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## References

1. W. K. Luk And R. H. Dennard, "A Novel Dynamic Memory Cell With Internal Voltage Gain," Ieee Journal Of Solid-State Circuits, Vol. 40, No. 4, April 2005.
2. H. J. Yoo, "A Low Voltage High Speed Self-Timed Cmos Logic For The Multi-Gigabit Synchronous Dram Application," Ieice Trans. Electron., Vol. E80-C, No. 8, Pp. 1126–1128, Aug. 1997..
3. John E. Leiss, Pallab K. Chatterjee, And Thomas C. Holloway, " Dram Design Using The Taper-Isolated Dynamic Ram Cell,'' Ieee Transactions On Electron Devices, Vol. Ed-29, No. 4, April 1982.
4. G. W. Taylor, P. K. Chatterjee, H-S. Fu, And A. F. Tasch, Jr., "A Punch-Through Isolated Ram Cell," In Ieee Iedm Tech. Dig., P. 352, 1978.
5. K. M. Cao, W. –C. Lee, W. Liu, X. Jin, P. Su, S. K. Fung, J. X. An, B. Yu, C. Hu, "Bsim4 Gate Leakage Model Including Source-Drain Partition," Iedm Meeting 2000, Iedm Technical Digest, Pp. 815-818, December, 2000.
6. R. X. Gu, And M. I. Elmasry, "Power Dissipation Analysis And Optimization For Deep Submicron Cmos Digital Circuits," Ieee Jssc, 31(5):707–713, May 1996.
7. Y. Taur And T. H. Ning, "Fundamentals Of Modern Vlsi Devices," (1998), Pp 200-202.
8. N. H. E. Weste, And K. Eshraghian, Editor. "Principles Of Cmos Vlsi Design", A Systems Perspective, 2nd Ed. Addison-Wesley, 1993.
9. Fumiyoshi Matsuoka, Hiroshi Sakuraba, Member, Ieee, And Fujio Masuoka, Fellow, Ieee, "Device Design Guidelines For Fc-Sgt Dram Cells With High Soft-Error Immunity," Ieee Transactions On Electron Devices, Vol. 52, No. 6, June 2005.

10. I.-C. Chen, M. Rodder, And J.-M. Hwang, "A Comparative Study Of Locos-Type Isolations For 256mbit Dram," Semiconductor Process And Device Center Texas Instruments Usa.
11. Narender Hanchate And N. Ranganathan, " A New Technique For Leakage Reduction In Cmos Circuits Using Self-Controlled Stacked Transistors," Nanomaterials And Nanomanufacturing Research Center Department Of Computer Science And Engineering University Of South Florida, Ieee 2004.
12. J.E. Banh. J.K. Debrosse, R.H. Dennard, H.L. Kalter, J. Gautief And H.I. Hanafi , "Floating Body Concerns For Soi Dynamic Random Access Memory(Dram)," Ibm Semiconductor Research And Development Center, Hopewell Junction, Ny , Ieee International So1 Conference, Oct. 1996.
13. Yuh-Fang Tsai, Student, Ieee, David E. Duarte, Member, Ieee, N. Vijaykrishnan, Member, Ieee, And Mary Jane Irwin, Fellow, Ieee, "Characterization And Modeling Of Run-Time Techniques For Leakage Power Reduction," Ieee Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 12, No. 11, November 2004.
14. Oleg Semenov, Andrzej Pradzynski, Member, Ieee, And Manoj Sachdev, Senior Member, Ieee, "Impact Of Gate Induced Drain Leakage On Overall Leakage Of Submicrometer Cmos Vlsi Circuits," Ieee Transactions On Semiconductor Manufacturing, Vol. 15, No. 1, February 2002.
15. Shipra Mishra*, Amit Dubey, Shelendra Singh Tomar, Shyam Akashe, "Design And Simulation Of High Level Low Power 7t Sram Cell Using Various Process & Circuit Techniques," 2012 Ieee.

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