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# Managing the Traffic in Multipath Switching system using Flow Slice

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## ABSTRACT

**Multipath switching system are used in as core routers.These routers provide terabit or even petabit switching capacity. The most difficult issues in designing the multipath switching system is how to manage the traffic across its multipath. On the same way that is not disturbing the flow packet orders.Resulting of the previous solution was suffer from delay penalities or load hardware algorithm was used previouslythey perform badly due to the heavy-failed flow size distribution.In this paper,we develop a novel schemeNamely flow slice that cuts the each flow into flow slice at every intraflow interval larger than the slicing threshold and manages the traffic on a finer granularity.The flow slice scheme achieves comparative managing the traffic to a optimal one . it also limits the probability of out-of-order packet to a negligible level, on three popular Mpsec at the cost of little hardware complexity and an internal speedupto two. In this paper the resultsare proven by theoretical analyses and also validated through trace-drivenprotype simulation.**

**Keywords**: Flowslice,traffic management,switching system.

## I. INTRODUCTION

The MultipathSwitching systems (MPS) plays a major rolein fabricating the high performance corerouters. A well-known paradigm is the deployment of Benes multistage switches in Cisco CRS-1 . Other examples include the Vitesse switch chip family implementing the Parallel Packet Switch (PPS), and the Load-balanced Birkhoff-von Neumann (LBvN) switches [1]. In general, MPS is built by aggregating several lower speed switches and,therefore, exhibits multiple internal data paths.

## II. LITERATURE SURVEY

The various findings say the following types of methods are used for managing the traffic in multipath switching systems. They are uniform load sharing, it has the traffic destined for each output should be dispatched to all the switching paths uniformly; intraflow packet ordering,it has the packets in the same flow should depart MPS as their arrival orders;low complexitythe load-balancing and the additional resequencing mechanisms should work fast enough to catch up with the switch fabric's line rate.

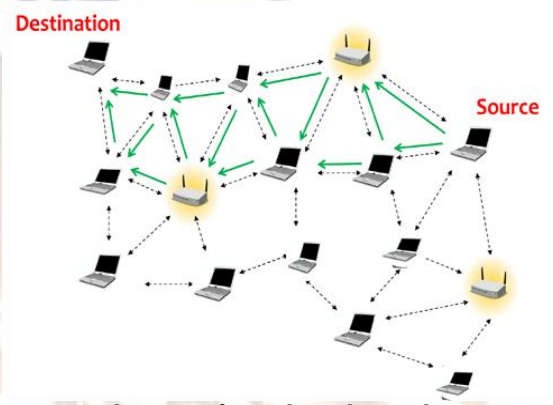


Fig. 1: Architecture for multi path switching

## III.FLOW SLICE

A flow-slice is a sequence of packets in a flow, whereevery intra-flow interval between two consecutive packets issmaller than or equal to a slicing threshold ST [2].Flow slices can be seen as miniflows created by cutting off every intraflow interval larger than .we depict the Cumulative Distribution Functions (C.D.F) of intraflow intervals in our traces [3].Flow-slices can be seen as mini-flows created by cutting off everyintra-flow interval larger than ST. Compared with the original 5-tuple flows, three specific properties are observed for flow-slice in all the traces.

- Small Size). Both the average packet count (FC) and the average size (FS) of flow slice are much smaller than those of the original flow.
- (Light-Tailed Size Distribution). Flow-slice packet count/size distributions are light tailed while it is well-known that original flow-size distribution is heavy tailed. (Fewer Active Flow Slices). The active flow-slice number is 1-2 magnitudes smaller than that of active flow

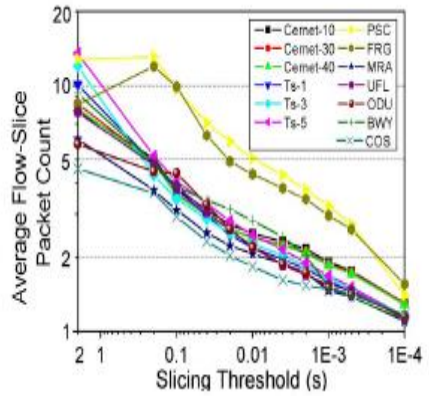


Fig 3.1: Flow Slice Packet Count

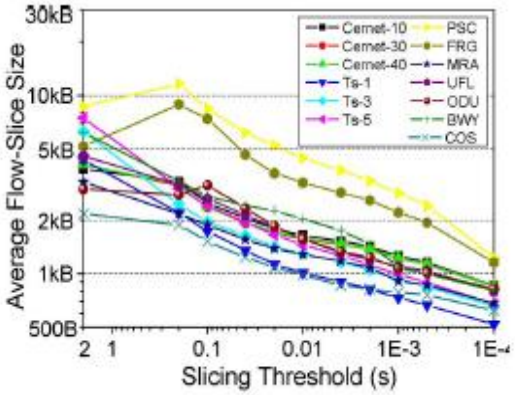


Fig 3.2: Flow Slice Size

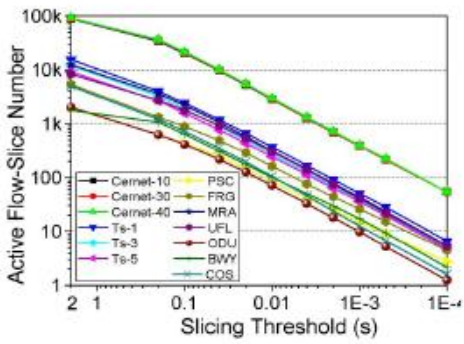


Fig 3.3:Active Flow Slice Number

## V. SWITCHING SYSTEM

Our major improvement over the existing works is to tailor the approach in the scenario by introducing the offline delay bound calculation, while the previous solutions either use an empirical slicing threshold or maintain flow context to facilitate the slicing. The traces here are collected at backbone links of one of the largest commercial backbones worldwide [4].

The disadvantages are our major improvement over the existing works is to tailor the FS approach in the MPS scenario by introducing the offline delay bound.

## VI.MANAGINGTHE TRAFFIC PERFORMANCE

In this paper a novel load-balancing scheme, namely, Flow Slice, based on the fact that the intraflow packet interval is often, larger than the [5]. Due to three positive properties of flow slice, our scheme achieves good load-balancing uniformity with little hardware overhead and timing complexity. By calculating delay bounds at three popular, we show that when the slicing threshold is set to the smallest admissible value at, the FS scheme can achieve optimal performance while keeping the intraflow packet out-of-order probability negligible given an internal speedup up to two. Our results are also validated through trace-driven prototype simulations under traffic patterns.The advantages are immune to packet loss, while other solutions like the resequencer require additional loss detection Mechanisms.The Load Balancing can be deployed using the following modules.

1. Load-Balancing Scheme
2. MULTIPATH SWITCHING SYSTEM
3. Multistage Multiplane Clos Switches

**1)Load-Balancing Scheme**: Interflow packet order is natively preserved besetting slicing threshold to the delay upper bound at any two packets in the same flow slice cannot be disordered as they are dispatched to the same switching path where processing is guaranteed; and two packets in the same flow but different flow slices will be in order at departure, as the earlier packet will have depart from before the latter packet arrives [6]. Due to the fewer number of active flow slices, the only additional overhead in, the hash table, can be kept rather small, , and placed on-chip to provide ultrafast access speed. This table size depends only on system line rate and will stay unchanged even if scales to more than thousand external ports, thus guarantees system scalability.

**2) Multipath switching system:** Through lay-aside Buffer Management module, all packets are virtually queued at the output according to the flow group and the priority class in a hierarchical manner. The output scheduler fetches packets to the output line using information provided by. Packets in the same flow will bevirtually buffered in the same queue and scheduled in discipline. Hence, intraflow packet departure orders holdas their arriving orders at the multiplexer. Central-stage parallel switches adopt an output-queued model [7]. By Theorem, we derive packet delay bound at firststage. We then study

delay at second-stage switches. Define native packet delay at stage m of an be delay experienced at stage m on the condition that all the preceding stages immediately send all arrival packets out without delay.

**3) Multistage Multiplane Clos Switches:** We consider the Multistage Multiplane Clos-networkbased switch by Chao et a . It is constructed of five stages of switchmodules with top-level architecture similar to a external input/output ports [8]. The first and last stages Clos are composed of inputdemultiplexers and output multiplexers, respectively, having similar internal structures as those in PPS. Stages 2-4 of M2Clos are constructed by parallel switching planes; however, each plane is no longer formed by a basic switch, but by a three-stage Clos Network to support large port count. Inside each Clos Network, the first stage is composed by k identical Input Modules [9]. Each IM is an packet switch, with each output link connected to a Central Module. Thus, there are a total of m identical in second stage of the Close networks

## VIII.CONCLUSION

We propose a novel load-balancing scheme, namely, FlowSlice, based on the fact that the intraflow packet interval isoften, say in 40-50 percent, larger than the delay upperbound at MPS. Due to three positive properties of flow slice,our scheme achieves good load-balancing uniformity withlittle hardware overhead and O(1) timing complexity. Bycalculating delay bounds at three popular MPSes, we showthat when the slicing threshold is set to the smallestadmissible value at 1-4 ms, the FS scheme can achieveoptimal performance while keeping the intraflowpacketout-of-order probability negligible, given aninternal speedup up to two. Our results are also validatedthrough trace-driven prototype simulations under highlybursty traffic patterns.

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