

Read stability and Write ability analysis of different SRAM cell structures

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ABSTRACT

SRAM cell read stability and write-ability is major concerns in nanometer CMOS technologies, due to the progressive increase in intra-die variability and VDD scaling. This paper analyzes the read stability and write ability of 6T, 8T, 9T SRAM cell structures. SRAM cell stability analysis is typically based on Static Noise Margin (SNM) investigation. This paper represents the simulation of three SRAM cell topologies and their comparative analysis on the basis of read noise margin (RNM), write noise margin (WNM). Both 8T SRAM cell and 9T SRAM cell provides higher read noise margin as compared to 6T SRAM cell. Although the size of 9T SRAM cell is higher than that of the 8T SRAM cell but it provides higher write stability. In this paper we propose a methodology to characterize the DC noise margin of 6T, 8T and 9T SRAM. All simulations of the SRAM cell have been carried out in 130nm CMOS technology.

Keywords -Noise margin, read stability, read noise margin (RNM), SRAM cell, Static Noise Margin (SNM), write ability, Write noise margin (WNM).

1. INTRODUCTION

A SRAM cell consist of a latch, therefore the cell data is kept as long as power is turned on and refresh operation is not required for the SRAM cell. SRAM is mainly used for the cache memory in microprocessors, mainframe computers, engineering workstations and memory in hand held devices due to high speed and low power consumption. Each bit in an SRAM is stored on four transistors that form two cross coupled inverters.

With increased device variability in nanometer scale technologies, SRAM becomes increasingly vulnerable to noise sources. The wider spread of local mismatch leads to reduced SRAM reliability. For the demand of minimizing power consumption during active operation, supply voltage scaling is often used. However, SRAM reliability is even more suspect at lower voltages. VCCmin is the minimum supply voltage for an SRAM array to read and write safely

under the required frequency constraint. Therefore, the analysis of SRAM read/write margin is essential for low-power SRAMs. In recent years, research on sub-threshold SRAMs has shown the promise of SRAM design for energy-efficient and ultra-low-power applications. The most challenging issue for sub threshold SRAM is increasing reliability during read/write. A good metric for read/write margin is critically important to all kinds of SRAM designs. Moreover, the stability of the SRAM cell is seriously affected by the increase in variability and by the decrease in supply voltage. Furthermore, new SRAM cell circuit designs have been developed to maximize the cell stability for future technology nodes.

In this paper, we will emphasize SRAM read margin and write margin analysis and compare the different SRAM cells configurations on the basis of the stability analysis. Static noise margins (SNMs) [1] are widely used as the criteria of stability. SNM is defined as the minimum DC noise voltage [2] needed to flip the cell state, and is used to quantify the stability of a SRAM cell using a static approach.

2. LITERATURE REVIEW OF DIFFERENT SRAM CELLS

2.1 6T SRAM CELL

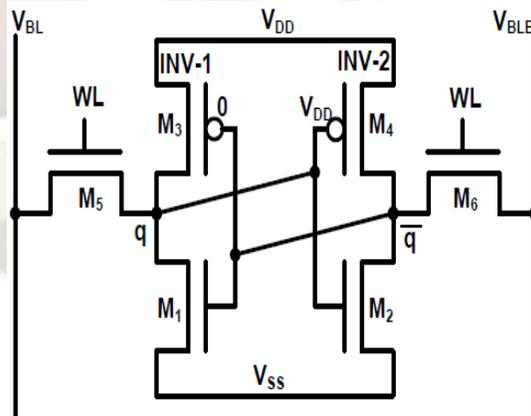


Figure 1: Standard 6T SRAM cell.

The schematic diagram of 6T SRAM cell is shown in Fig.1. The conventional 6T SRAM memory cell is composed of two cross-coupled CMOS inverters with

two pass transistors connected to complementary bit-lines. Fig. 1 shows this well known architecture, where the access transistors M5 and M6 are connected to the word-line (WL) to perform the access write and read operations through the column bit-lines (BL and BLB). Bit-lines act as input/output nodes carrying the data from SRAM cells to a sense amplifier during read operation, or from write circuitry to the memory cells during write operations. All transistors have minimum length (L_{min}), while their widths are typically design parameters.

6T SRAM cell implementation has the advantage of low static power dissipation. However, the potential stability problem of 6T SRAM cell as shown in figure 1 is such that during the read operation, a stored "0" can be overwritten by a "1" when the voltage at node Q reaches the V_{th} of NMOS M1 to pull node QB down to "0" and in turn pull node Q up even further to "1" due to the mechanism of positive feedback.

To overcome the problem of data storage destruction during the read operation [3], an 8T-cell implementation was proposed, for which separate read/write word signal lines are used as shown in fig (2) to separate the data retention element and the data output element.

2.2 8T SRAM CELL

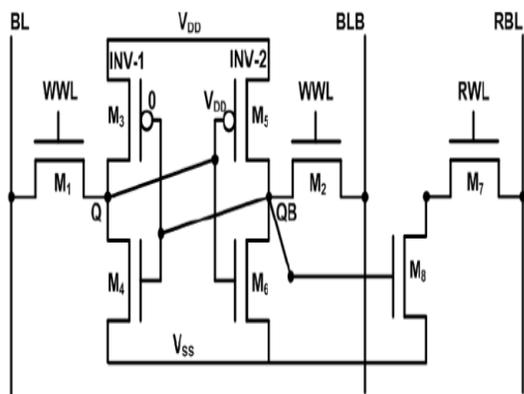


Figure 2: 8T SRAM cell

A dual-port cell (8T-cell) is created by adding two data output transistors to 6T-cell, as shown in Fig. 2. Separation of data retention element and data output element means that there will be no correlation between the read SNM cell and I cell. These separate read and write ports are controlled by read (RWL) and write (WWL) word lines and used for accessing the bit cell during read and write cycles, respectively. In 8T bit cell topology, read and write operations of a standard 6T SRAM bit cell are de-coupled by creating an isolated read-port or read buffer (comprised of two transistors, M7 and M8). De-coupling of read and

write operations yields a non destructive read operation or SNM-free read stability.

An additional leakage current path is introduced by the separate read-port which increases the leakage current as compared to standard 6T bit cell. Therefore, an increased area overhead and leakage power make this design rather unattractive, since leakage power is a critical SRAM design metric, particularly for highly energy constrained applications.

2.3 9T SRAM CELL

The schematic of the new 9T SRAM cell is shown in Fig.3. Standard 6T bit cell along with three extra transistors were employed in nine-transistor (9T) SRAM bit cell to bypass read-current from the data storage nodes.

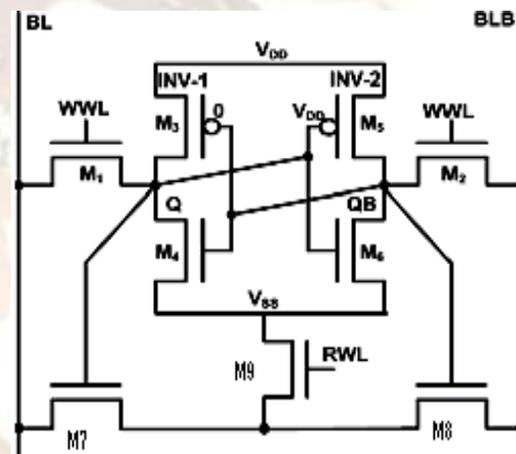


Figure 3: 9T SRAM cell.

A novel 9T SRAM cell with enhanced data stability and reduced leakage power consumption is presented in this section. The upper sub-circuit of the new memory cell is essentially a 6T SRAM cell. The two write access transistors (M1 and M2) are controlled by a write signal (WWL). The data is stored within this upper memory sub-circuit. The lower sub-circuit of the new cell is composed of the bit-line access transistors (M7 and M8) and the read access transistor (M9). The operations of M7 and M8 are controlled by the data stored in the cell. M9 is controlled by a separate read signal (RWL).

3. STATIC NOISE MARGIN (SNM)

SNM is the measure of stability of the SRAM cell to hold its data against noise. SNM of SRAM is defined as minimum amount of noise voltage present on the storing nodes of SRAM required to flip the state of cell.

There are two methods to measure the SNM of SRAM cell. First method is a graphical approach in which SNM can be obtained by drawing and mirroring the inverter characteristics and then finding the maximum possible square between them. The second approach involves the use of noise source voltages at the nodes as shown in figure 4 (a).

SNM Dependences [4] includes cell ratio (CR), supply voltage and also pull up ratio .Cell ratio [5] is the ratio between sizes of the driver transistor to the load transistor during the read operation. Pull up ratio [5] is the ratio between sizes of the load transistor to the access transistor during write operation.

With reference to figure (1),

$$CR = \frac{W/L(M1)}{W/L(M5)} \text{ (During Read Operation)}$$

$$PR = \frac{W/L(M4)}{W/L(M6)} \text{ (During Write Operation)}$$

If the cell ratio increases, size of the driver transistor also increases, consequently increasing the current. As current increases, the speed of the SRAM cell also increases.

4. READ STABILITY AND WRITE-ABILITY OF THE SRAM CELL

4.1 The SRAM cell read stability

Data retention of the SRAM cell, both in standby mode and during a read access, is an important functional constraint in advanced technology nodes. The cell becomes less stable with lower supply voltage increasing leakage currents and increasing variability, all resulting from technology scaling. The stability is usually defined by the SNM [6] as the maximum value of DC noise voltage that can be tolerated by the SRAM cell without changing the stored bit.

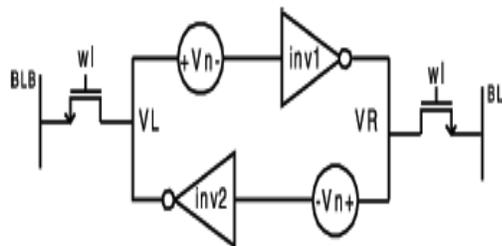


Figure 4: (a) The standard setup for the SNM definition.

In Fig. 4(a), the equivalent circuit for the SNM definition [6] is shown. The two DC noise voltage sources are placed in series with the cross-coupled inverters. The minimum value of noise voltage (V_n) which is necessary to flip the state of the cell is recorded as SNM.

The graphical method to determine the SNM uses the static voltage transfer characteristics of the SRAM cell inverters.

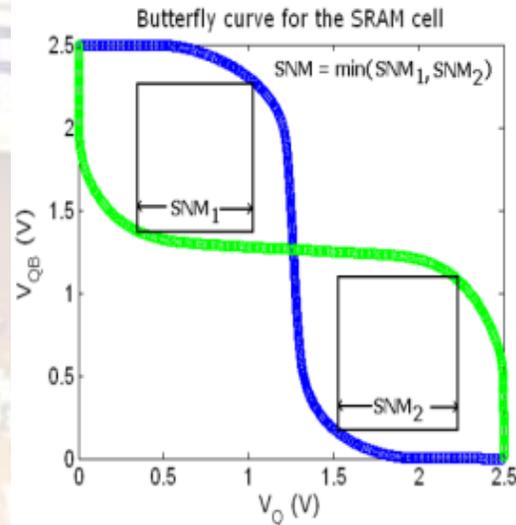


Figure 4: (b) Butterfly curve for the SRAM cell

Fig.4 (b) superposes the voltage transfer characteristic (VTC) of one cell inverter to the inverse VTC of the other cell inverter. The resulting two-lobed graph is called a "butterfly" curve and is used to determine the SNM. Its value is defined as the side length of the largest square that can be fitted inside the lobes of the "butterfly" curve.

More the value of SNM, higher is the read stability of the SRAM cell. A cell with lower RSNM has poorer read stability.

4.2 Write ability of the SRAM cell

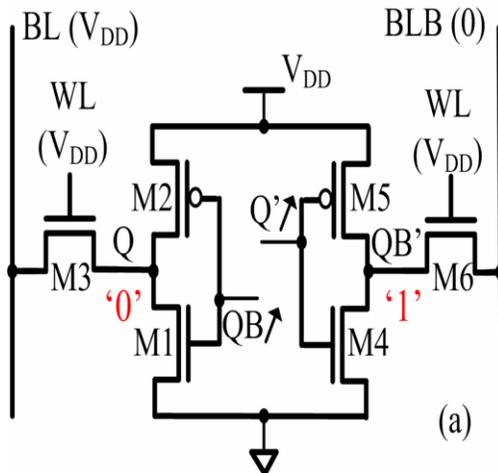


Figure 5: (a) Circuit for WSNM [7] of writing '1'.

Write margin is the measure of the ability to write data into the SRAM cell. Write margin voltage is the maximum noise voltage present at bit lines during successful write operation. When noise voltages exceeds the write margin voltage, then write failure occurs. In this section, we introduce static approach for measuring write margin. The most common static approach uses SNM as a criterion.

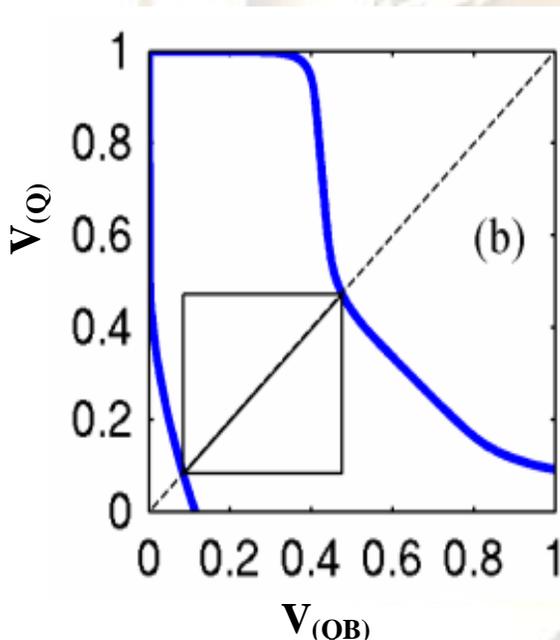


Figure 5: (b) WSNM [7] of writing '1' is the width of the smallest embedded square at the lower-right side

The cell is set in the write operation. Figure 5(a) shows the circuit for writing a '1' into the cell. Write SNM (WSNM) is measured using butterfly or VTC [8] curves (Figure5 b), which are obtained from a dc

simulation sweeping the input of the inverters (QB and Q').

For a successful write, only one cross point should be found on the butterfly curves, indicating that the cell is mono-stable. WSNM for writing '1' is the width of the smallest square that can be embedded between the lower-right half of the curves. WSNM for writing '0' can be obtained from a similar simulation. The final WSNM for the cell is the minimum of the margin for writing '0' and writing '1'. A cell with lower WSNM has poorer write ability.

5. SIMULATION AND RESULTS

All simulations are done using 130nm CMOS logic process technology in Hspice environment.

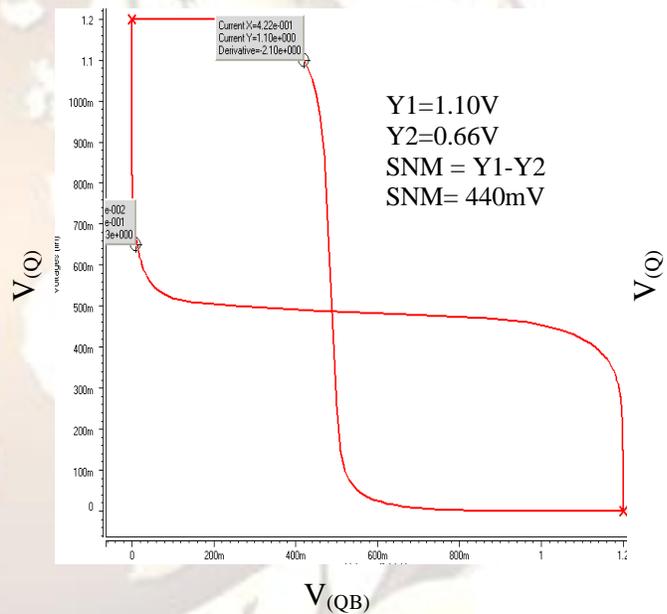


Figure 6: Simulation of HOLD SNM of 6T SRAM cell

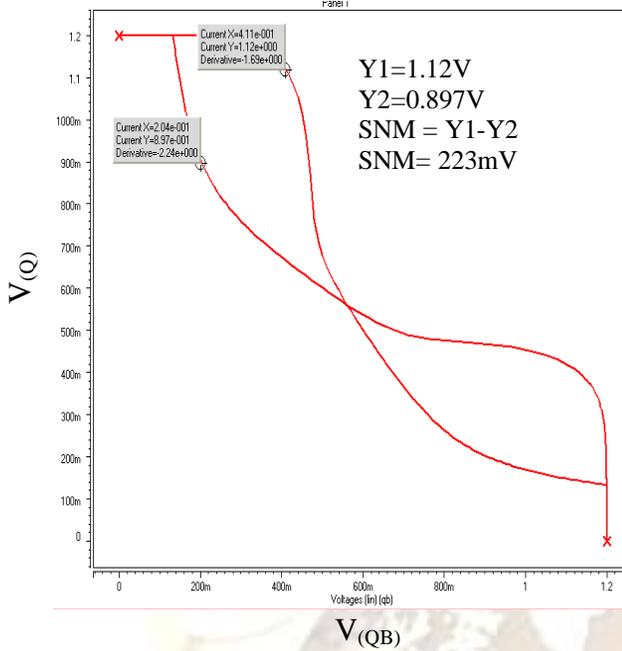


Figure 7: Simulation of RNM of 6T SRAM cell

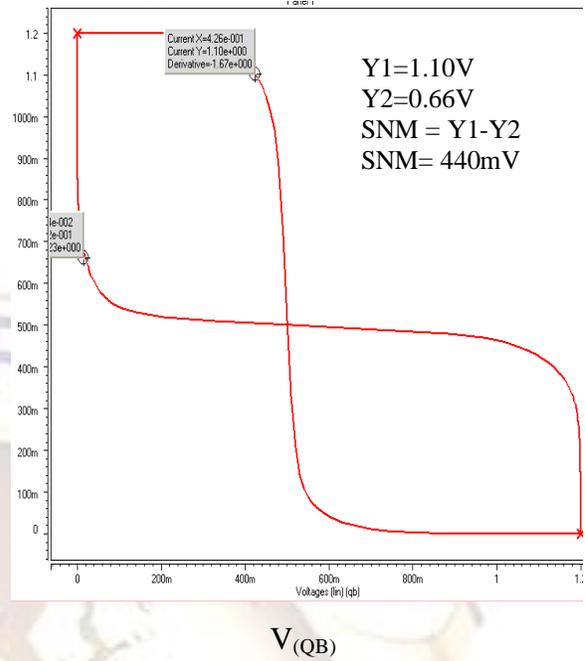


Figure 9: Simulation of RNM of 8T SRAM cell

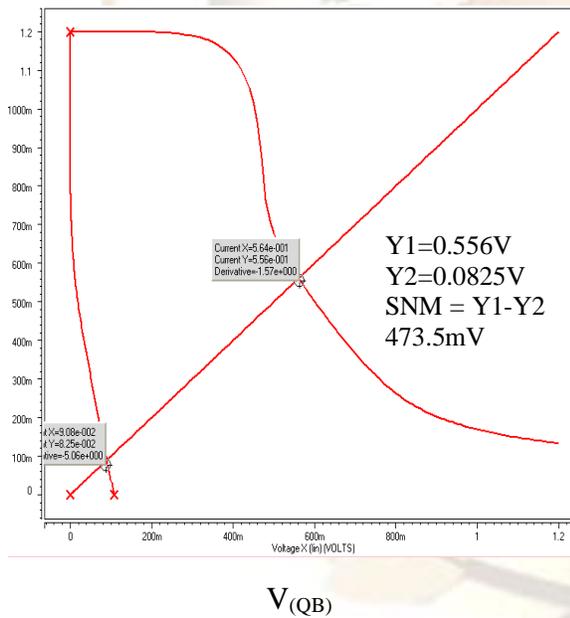


Figure 8: Simulation of WNM of 6T SRAM cell

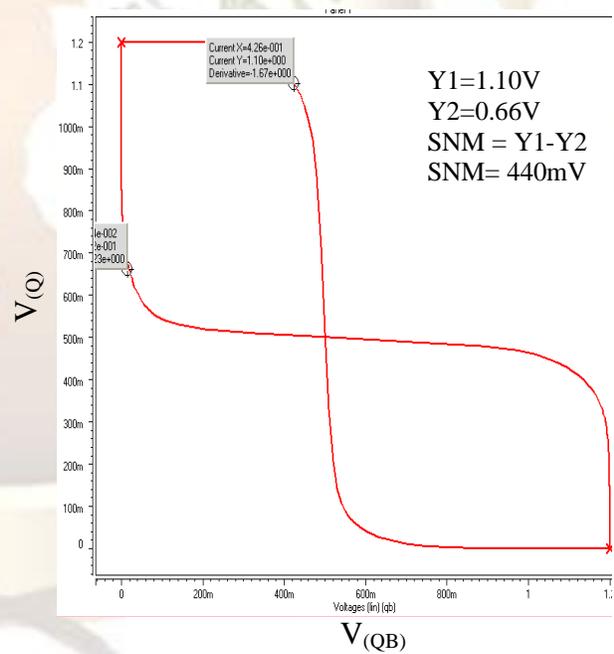


Figure 10: Simulation of RNM of 9T SRAM cell

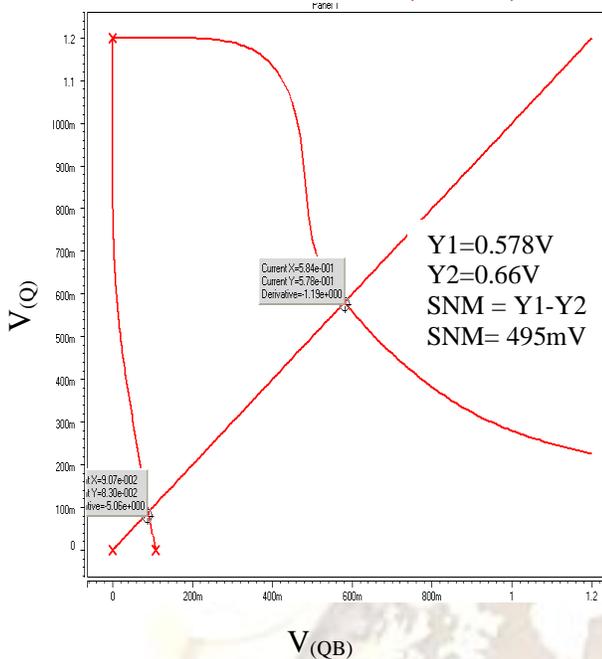


Figure 11: Simulation of WNM of 9T SRAM cell

Table 1: SNM for 6T, 8T and 9T SRAM cell

SRAM CELL	HOLD SNM (mV)	READ SNM (mV)	WRITE SNM (mV)
6T	440	223	473.5
8T	440	440	473.5
9T	440	440	495

6. CONCLUSION

The stability performances of three SRAM cell topologies have been presented. As process technologies continue to advance, the speed of SRAMs will increase, but devices will be more susceptible to mismatches, which worsen the static-noise margin of SRAM cells.

The 6T SRAM provide very less RNM. To obtain higher RNM in 6T SRAM cell width of the pull down transistor has to be increased but this increases area of the SRAM which in turn increases the leakage currents.

The 8T SRAM cell provide higher read noise margin. Due to asymmetric cell structure 8T SRAM cell may prone to failure during write operation. On the other hand 9T SRAM cell has higher RNM as well as WNM thus showing better stability performance as compare to 6T and 8T SRAM cell.

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REFERENCES

- [1] Jiajing Wang, Satyanand Nalam, and Benton H. Calhoun, *Analyzing Static and Dynamic Write Margin for Nanometer SRAMs*, Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, VA 22904, USA.
- [2] Kanak Agarwal, Sani Nassif, *Statistical Analysis of SRAM Cell Stability*, IBM Research, Austin, TX.
- [3] Mo Maggie Zhang, *Performance Comparison of SRAM Cells Implemented in 6, 7 and 8-Transistor Cell Topologies*, Electrical and Computer Engineering, University of California, Davis.
- [4] B. Alorda, G. Torrens, S. Bota and J. Segura, *Static-Noise Margin Analysis during Read Operation of 6T SRAM Cells*, Univ. de les Illes Balears, Dept. Fisica, Cra. Valldemossa, 07071 Palma de Mallorca, Spain.
- [5] Debasis Mukherjee¹, Hemanta Kr. Mondal² and B.V.R. Reddy³, *Static Noise Margin Analysis of SRAM Cell for High Speed Application*, *IJCSI International Journal of Computer Science Issues*, Vol. 7, Issue 5, September 2010.
- [6] Evelyn Grossar, Michele Stucchi, Karen Maex, *Read Stability and Write-Ability Analysis of SRAM Cells for Nanometer Technologies*, *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, VOL. 41, NO. 11, NOVEMBER 2006, pp.2577-2588.
- [7] Jiajing Wang, Satyanand Nalam, and Benton H. Calhoun, *Analyzing Static and Dynamic Write Margin for Nanometer SRAMs*, Department of Electrical and Computer Engineering, University of Virginia.
- [8] Andrei S. Pavlov, *Design and Test of Embedded SRAMs*, doctoral diss., University of Waterloo, Ontario, Canada, 2005.