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# A Speed Control Of Pmbldcm Drive Using Single Stage Pfc Half Bridge Converter

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#### **Abstract**

In this paper, a buck half-bridge DC-DC converter is used as a single-stage power factor correction (PFC) converter for feeding a voltage source inverter (VSI) based permanent magnet brushless DC (PMBLDCM) drive. The front end of this PFC converter is a diode bridge rectifier (DBR) fed from single-phase AC mains. PMBLDCM is used to drive a compressor load of an air conditioner through a threephase VSI fed from a controlled DC link voltage. The speed of the compressor is controlled to achieve energy conservation using a concept of the voltage control at DC link to the desired speed of the proportional PMBLDCM. Therefore the VSI is operated only as an electronic commutator of the PMBLDCM. The stator current of PMBLDCM during step change of reference speed is controlled by a rate limiter for the reference voltage at DC link. The proposed PMBLDCM drive with voltage control based PFC converter is designed, modeled and its performance is simulated Matlabin Simulink environment for an air conditioner compressor driven through a 1.5 1500 rpm PMBLDC motor. The evaluation results of the proposed speed control scheme presented are demonstrate an improved efficiency of the proposed drive system with PFC feature in wide range of the speed and an input AC voltage.

IndexTerms— PFC, PMBLDCM, Air conditioner, Buck Half- bridge converter, Voltage control, VSI.

#### 1. Introduction

**PERMANENT** magnet brushless dc motors (PMBLDCM) are preferred motors for a compressor of an air-conditioning (Air con) system due to its features like high efficiency, wide speed range and low maintenance requirements [1-4]. The operation of the compressor with the speed control results in an improved efficiency of the system while maintaining the temperature in the air-conditioned zone at the set reference consistently. Whereas, the existing air

conditioners mostly have a single-phase induction motor to drive the compressor in 'on/off' control mode. This results in increased losses due to frequent 'on/off' operation with increased mechanical and electrical stresses on the motor, thereby poor efficiency and reduced life of the motor. Moreover, the temperature of the air conditioned zone is regulated in a hysteresis band. Therefore, improved efficiency of the Air-Con system will certainly reduce the cost of living and energy demand to cope-up with ever increasing power crisis.

A PMBLDCM which is a kind of threephase synchronous motor with permanent magnets (PMs) on the rotor and trapezoidal back EMF waveform, operates on electronic commutation accomplished by solid switches. It is powered through a three-phase voltage source inverter (VSI) which is fed from single-phase AC supply using a diode bridge rectifier (DBR) followed by smoothening DC link capacitor. The compressor exerts constant torque (i.e. rated torque) on the PMBLDCM and is operated in speed control mode to improve the efficiency of the Air-Con system.

Since, the back-emf of the PMBLDCM is proportional to the motor speed and the developed torque is proportional to its phase current [1-4], therefore, a constant torque is maintained by a constant current in the stator winding of the PMBLDCM whereas the speed can be controlled by varying the terminal voltage of the motor. Based on this logic, a speed control scheme is proposed in this paper which uses a reference voltage at DC link proportional to the desired speed of the PMBLDC motor. However, the control VSI is only for electronic of which is based on the rotor commutation position signals of the PMBLDC motor.

The PMBLDCM drive, fed from a single-phase AC mains through a diode bridge rectifier (DBR) followed by a DC link capacitor, suffers from power quality (PQ) disturbances such as poor power factor (PF), increased total harmonic distortion (THD) of current at input AC mains and its high crest factor (CF). It is mainly due to uncontrolled charging of the DC link capacitor

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which results in a pulsed current waveform having a peak value higher than the amplitude of the fundamental input current at AC mains. Moreover, the PQ standards for low power equipments such as IEC 61000-3-2 [5], emphasize on low harmonic contents and near unity power factor current to be drawn from AC mains by these motors. Therefore, use of a power factor correction (PFC) topology amongst various available topologies [6-14] is almost inevitable for a PMBLDCM drive.

Most of the existing systems use a boost converter for PFC as the front-end converter and an isolated DC-DC converter to produce desired output voltage constituting a two-stage PFC drive [7-8]. The DC-DC converter used in the second stage is usually a flyback or converter for low power applications and a higher for converter full-bridge applications. However, these two stage PFC converters have high cost and complexity in implementing two separate switch-mode converters, therefore a single stage converter combining the PFC and voltage regulation at DC link is more in demand. The single-stage PFC converters operate with only one controller to regulate the DC link voltage along with the power factor correction. The absence of a second controller has a greater impact on the performance of single-stage PFC converters and requires a design to operate over a much wider range of operating conditions.

For the proposed voltage controlled drive, a half-bridge buck DC-DC converter is selected because of its high power handling capacity as compared to the single switch converters. Moreover, it has switching losses comparable to the single switch converters as only one switch is in operation at any instant of time. It can be operated as a single-stage power factor corrected (PFC) converter when connected between the VSI and the DBR fed from singlephase AC mains, besides controlling the voltage at DC link for the desired speed of the Air-Con compressor. A detailed modeling, design and performance evaluation of the proposed drive are presented for an air conditioner compressor driven by a PMBLDC motor of 1.5 kW, 1500 rpm rating.

## 2. PROPOSED SPEED CONTROL SCHEME OF PMBLDC MOTOR FOR AIR CONDITIONER

The proposed speed control scheme (as shown in Fig. 1) controls reference voltage at DC link as an equivalent reference speed, thereby replaces the conventional control of the motor speed and a stator current involving various

sensors for voltage and current signals. Moreover, the rotor position signals are used to generate the switching quence for the VSI as an electronic commutator of the PMBLDC motor. Therefore, rotor-position information is required only at the commutation points, e.g., every 60°electrical in the three-phase [1-4]. The rotor position of PMBLDCM is sensed using Hall effect position sensors and used to generate switching sequence for the VSI as shown in Table-I.

The DC link voltage is controlled by a half-bridge buck DC-DC converter based on the duty ratio (D) of the converter. For a fast and effective control with reduced size of magnetics and filters, a high switching frequency is used; however, the switching frequency (f<sub>S</sub>) is limited by the switching device used, operating power level and switching losses of the device. Metal oxide field effect transistors (MOSFETs) are used as the switching device for high switching frequency in the proposed PFC converter. However, insulated gate bipolar transistors (IGBTs) are used in VSI bridge feeding PMBLDCM, to reduce the switching stress, as it operates at lower frequency compared to PFC switches.

The PFC control scheme uses a current control loop inside the speed control loop with current multiplier approach which operates in continuous conduction mode (CCM) with average current control. The control loop begins with the comparison of sensed DC link voltage with a voltage equivalent to the reference speed. The resultant voltage error is passed through a proportional-integral (PI) controller to give the modulating current signal. This signal is multiplied with a unit template of input AC voltage and compared with DC current sensed after the DBR. The resultant current error is amplified and compared with saw-tooth carrier wave of fixed frequency (f<sub>S</sub>) in unipolar scheme (as shown in Fig.2) to generate the PWM pulses for the halfbridge converter. For the current control of the PMBLDCM during step change of the reference voltage due to the change in the reference speed. a voltage gradient less than 800 V/s introduced for the change of DC link voltage, ensures the stator current of the PMBLDCM within the specified limits (i.e. double the rated current).

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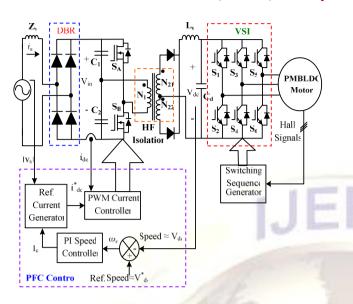


Figure 1. Control schematic of Proposed Bridgebuck PFC converter fed PMBLDCM drive

## 3. DESIGN OF PFC BUCK HALF-BRIDGE CONVERTER BASED PMBLDCM DRIVE

The proposed PFC buck half-bridge converter is designed for a PMBLDCM drive with main considerations on PQ constraints at AC mains and allowable ripple in DC link voltage. The DC link voltage of the PFC converter is given as,

V<sub>dc</sub> = 2 (N<sub>2</sub>/N<sub>1</sub>) V<sub>in</sub> D and N<sub>2</sub>= N<sub>21</sub>=N<sub>22</sub> where N<sub>1</sub>, N<sub>21</sub>, N<sub>22</sub> are number of turns in primary, secondary upper and lower windings of the high frequency (HF) isolation transformer, respectively.

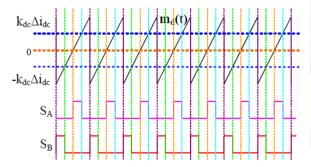


Figure 2. PWM control of the buck half-bridge converter

 $V_{in}$  is the average output of the DBR for a given AC input voltage ( $V_{S}$ ) related as,

$$V_{in} = 2\sqrt{2}V_s/\pi$$

A ripple filter is designed to reduce the ripples introduced in the output voltage due to high switching frequency for constant of the

buck half-bridge converter. The inductance ( $L_O$ ) of the ripple filter restricts the inductor peak to peak ripple current ( $\Delta I_{LO}$ ) within specified value for the given switching frequency ( $f_S$ ), whereas, the capacitance ( $C_d$ ) is calculated for a specified ripple in the output voltage ( $\Delta V_{Cd}$ ) [7-8]. The output filter inductor and capacitor are given as,

$$L_{O}= (0.5-D)V_{dC}/\{f_{S}(\Delta I_{LO})\}$$

$$C_{d}=I_{O}/(2\omega\Delta V_{Cd})$$
(4)

The PFC converter is designed for a base DC link voltage of  $V_{dc} = 400 \text{ V}$  at  $V_{in} = 198 \text{ V}$  from  $V_{s} = 220 \text{ Vrms}$ . The turns ratio of the high frequency transformer (N2/N1) is taken as 6:1 to maintain the desired DC link voltage at low input AC voltages typically at 170V. Other design data are  $f_{s} = 40 \text{ kHz}$ ,  $I_{o} = 4 \text{ A}$ ,  $\Delta V_{Cd} = 4 \text{ V}$  (1% of  $V_{dc}$ ),  $\Delta I_{Lo} = 0.8 \text{ A}$  (20% of  $I_{o}$ ). The design parameters are calculated as  $I_{o} = 2.0 \text{ mH}$ ,  $C_{d} = 1600 \text{ \muF}$ .

TABLE I. VSI SWITCHING SEQUENCE BASED ON THE HALL EFFECT SENSOR SIGNALS

|       | Ha    | Hb                | Hc               | Ea          | Eb   | Ec   | <b>S</b> 1 | <b>S2</b> | <b>S3</b> | <b>S4</b>    | <b>S</b> 5 | <b>S6</b> |          |
|-------|-------|-------------------|------------------|-------------|------|------|------------|-----------|-----------|--------------|------------|-----------|----------|
| 0     | 0     | 0                 | 0                | 0           | 0    | 0    | 0          | 0         | 0         | 0            | 0          | 0         |          |
| 7     | 0     | 0                 | 1                | 0           | -1   | +1   | 0          | 0         | 0         | 1            | 1          | 0         |          |
|       | 0     | 1                 | 0                | -1          | +1   | 0    | 0          | 1         | 1         | 0            | 0          | 0         |          |
| 7     | 0     | 1                 | 1                | -1          | 0    | +1   | 0          | 1         | 0         | 0            | 1          | 0         |          |
|       | 1     | 0                 | 0                | +1          | 0    | -1   | 1          | 0         | 0         | 0            | 0          | 1         |          |
|       | 1     | 0                 | 1                | ±1          | -1   | 0 .  | 1          | 0         | 0.        | 1.           | 0          | 0         | _        |
| (1) v | yhere | 1 <sup>N</sup> 1, | <del>ტ</del> 21, | <b>№</b> 22 | +are | nµmt | er of      | Oturi     | ış ın     | <b>B</b> rim | gry,       | seco      | ndary up |
|       | 1     | 1                 | 1                | 0           | 0    | 0    | 0          | 0         | 0         | 0            | 0          | 0         |          |

# 4.MODELING OF THE PROPOSED PMBLDCM DRIVE

The main components of the proposed PMBLDCM drive are the PFC converter and PMBLDCM drive, which are modeled by mathematical equations and the complete drive is represented as a combination of these models.

## A. PFC Converter

The modeling of the PFC converter consists of the modeling of a speed controller, a reference current generator and a PWM controller as given below.

1) Speed Controller: The speed controller, the prime component of this control scheme, is a proportional-integral (PI) controller which closely tracks the reference speed as an equivalent (29 ference voltage. If at  $k^{th}$  instant of time,  $V^*_{dc}(k)$  is reference DC link voltage,  $V_{dc}(k)$  is sensed DC link voltage then the voltage error

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Ve(k) is calculated as,

 $V_{e}(k) = V^*_{dc}(k) - V_{dc}(k)$ 

The PI controller gives desired control signal after processing this voltage error. The output of the controller  $I_{\text{C}}(k)$  at  $k^{\text{th}}$  instant is given as.

$$\begin{array}{lll} I_C & (k) = I_C & (k\text{-}1) \ + \ K_p\{V_e(k) \ - \ V_e(k\text{-}1)\} \ + \\ K_iV_e(k) & \end{array}$$

where  $K_p$  and  $K_i$  are the proportional and integral gains of the PI controller.

2) Reference Current Generator: The reference input current of the PFC converter is denoted by idc\* and given as,

$$i^*_{dc} = I_c$$
 (k)  $uV_s$  (7) where  $uV_s$  is the unit template of the voltage at input AC mains, calculated as,

 $uV_S=v_d/V_{sm}; v_d=|v_S|; v_S=V_{sm} \sin \omega t$  (8) where  $V_{sm}$  is the amplitude of the voltage and  $\omega$  is frequency in rad/sec at AC mains.

3) PWM Controller: The reference input current of the buck half-bridge converter ( $idc^*$ ) is compared with its sensed current (idc) to generate the current error  $\Delta idc = (idc^* - idc)$ . This current error is amplified by gain kdc and compared with fixed frequency ( $f_s$ ) saw-tooth carrier waveform md(t) (as shown in Fig.2) in unipolar switching mode [7] to get the switching signals for the MOSFETs of the PFC buck half-bridge converter as,

If  $k_{dc}$   $\Delta i_{dc}$  >  $m_d$  (t) then  $S_A = 1$  else  $S_A = 0$ 

If  $-k_{dc} \Delta i_{dc} > m_d$  (t) then  $S_B = 1$  else  $S_B = 0$  (10) where  $S_A$ ,  $S_B$  are upper and lower switches of the half-bridge converter as shown in Fig. 1 and their values '1' and '0' represent 'on' and 'off' position of the respective MOSFET of the PFC converter.

#### **B. PMBLDCM Drive**

The PMBLDCM drive consists of an electronic commutator, a VSI and a PMBLDC motor.

1) Electronic Commutator: The electronic commutator uses signals from Hall effect position sensors to generate the switching sequence for the voltage source inverter based on the logic given in Table I.

2) Voltage Source Inverter: Fig. 3 shows an equivalent circuit of a VSI fed PMBLDCM. The output of VSI to be fed to phase 'a' of the PMBLDC motor is given

$$v_{ao} = (V_{dc}/2)$$
 for  $S_1 = 1$  (11)

$$v_{ao} = (-V_{dc}/2)$$
 for  $S_2 = 1$  (12)

$$v_{ao} = 0$$
 for  $S_1 = 0$ , and  $S_2 = 0$  (13)

$$v_{an} = v_{ao} - v_{no} \tag{14}$$

where  $v_{ao}$ ,  $v_{bo}$ ,  $v_{co}$ , and  $v_{no}$  are voltages of the three-phases and neutral point (n) with respect to virtual mid-point of the DC link voltage shown as 'o' in Fig. 3. The voltages  $v_{an}$ ,  $v_{bn}$ ,  $v_{cn}$  are voltages of three-phases with respect to neutral point (n) and  $V_{dc}$  is the DC link voltage. S=1 and 0 represent 'on' and

'off' position of respective IGBTs of the VSI and considered in a similar way for other IGBTs of the VSI i.e. S3-S6.

Using similar logic v<sub>bo</sub>, v<sub>co</sub>, v<sub>bn</sub>, v<sub>cn</sub> are generated for other two phases of the VSI feeding PMBLDC motor.

3) PMBLDC Motor: The PMBLDCM is represented in the form of a set of differential equations [3] given as,

$$v_{an} = Ri_a + p\lambda_a + e_{an}$$
 (15)

$$v_{bn} = Rib + p\lambda b + ebn$$
 (16)

$$v_{cn} = Ri_c + p\lambda_c + e_{cn}$$
 (17)

where p is a differential operator (d/dt),  $i_a$ ,  $i_b$ ,  $i_c$  are three-phase

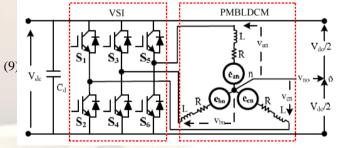


Figure 3.Equivalent Circuit of a VSI fed PMBLDCM Drive

The flux linkages are represented as,

$$\lambda_a = \text{Li}_a - M (i_b + i_c) \tag{18}$$

$$\lambda_b = \text{Li}_b - M (i_a + i_c) \tag{19}$$

$$\lambda_{C} = \text{Li}_{C} - M (i_{b} + i_{a}) \tag{20}$$

where L is self-inductance/phase, M is mutual inductance of motor winding/phase. Since the PMBLDCM has no neutral connection, therefore,

$$i_a + i_b + i_c = 0$$
 (21)  
From Eqs. (14.21) the voltage between neutron

From Eqs. (14-21) the voltage between neutral terminal (n) and mid-point of the DC link (o) is given as,

$$v_{no} = \{v_{ao} + v_{bo} + v_{co} - (e_{an} + e_{bn} + e_{cn})\}/3$$
 (22)  
From Eqs. (18-21), the flux linkages are given as,

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$$\begin{array}{lll} \lambda_{a} &= (L+M) \ i_{a}, & \lambda_{b} &= (L+M) \ i_{b}, \\ \lambda_{c} &= (L+M) \ i_{c}, & \end{array} \eqno(23)$$

From Eqs. (15-17 and 23), the current derivatives in generalized state space form is given as,

$$pi_X = (v_{Xn} - i_X R - e_{Xn})/(L+M)$$
 where x represents phase a, b or c. (24)

The developed electromagnetic torque,  $T_e$  in the PMBLDCM is given as,

$$T_e = (e_{an} i_a + e_{bn} i_b + e_{cn} i_c)/\omega$$
 (25) where  $\omega$  is motor speed in rad/sec,

The back emfs may be expressed as a function of rotor position  $(\theta)$  as,

$$e_{xn} = K_b f_x(\theta) \omega$$

(26) where x can be phase a, b or c and accordingly  $f_X(\theta)$  represents function of rotor position with a maximum value  $\pm 1$ , identical to trapezoidal induced emf given as,

$$f_a(\theta) = 1$$

for 
$$0 < \theta < 2\pi/3$$
 (27)  
 $f_a(\theta) = \{ (6/\pi)(\pi - \theta) \} - 1$ 

for 
$$2\pi/3 < \theta < \pi$$
 (28)

$$f_a(\theta) = -1 \qquad \text{for } \pi < \theta < 5\pi/3 \tag{29}$$

 $f_a(\theta) = \{(6/\pi)(\theta - 2\pi)\} + 1$  for  $5\pi/3 < \theta < 2\pi$  phase difference of 120° and 240° respectively. Therefore, the electromagnetic torque is expressed as

$$T_e = K_b\{f_a(\theta) i_a + f_b(\theta) i_b + f_c(\theta) i_c\}$$
 (31)  
The mechanical equation of motion in speed derivative form is given as,

$$p\omega = (P/2) (T_e-T_L-B\omega)/(J)$$
 (32)

The derivative of the rotor position angle is given as,  $p\theta = \omega$  (33) where P is no. poles, TL is load torque in Nm, J is moment of inertia in kg-m<sup>2</sup> and B is friction coefficient in Nms/Rad.

These equations (15-33) represent the dynamic model of the PMBLDC motor.

# 5.PERFORMANCE EVALUATION OF PROPOSED PFC DRIVE

The proposed PMBLDCM drive is modeled in Matlab- Simulink environment and evaluated for an air conditioning compressor load. The compressor load is considered as a constant torque load equal to rated torque with the speed control required by air conditioning system. A 1.5 kW rating PMBLDCM is used to drive the air conditioner compressor, speed of which is controlled effectively by controlling the

DC link voltage. The detailed data of the motor simulation parameters are given Appendix. The performance of the proposed PFC drive is evaluated on the basis of various parameters such as total harmonic distortion (THDi) and the crest factor (CF) of the current at input AC mains, displacement power factor (DPF), power factor (PF) and efficiency of the drive system (ndrive) at different speeds of the motor. Moreover, these parameters are also evaluated for variable input AC voltage at DC link voltage of 416 V which is equivalent to the rated speed (1500 rpm) of the PMBLDCM. The results are shown in Figs. 4-9 and Tables II- III to demonstrate effectiveness of the proposed PMBLDCM drive in a wide range of speed and input AC voltage.

## A. Performance during Starting

The performance of the proposed PMBLDCM drive fed from 220 V AC mains during starting at rated torque and 900 rpm speed is shown in Fig. 4a. A rate limiter of 800 V/s is introduced in the reference voltage to limit the starting current of the motor as well as the charging current of the DC link capacitor. The PI controller closely tracks the reference speed so that the motor attains reference speed smoothly within 0.35 sec while keeping the stator current within

(30) the desired dissipates and the extra transfer of the extra t

## **B.** Performance under Speed Control

Figs. 4-6 show the performance of the proposed PMBLDCM drive under the speed control

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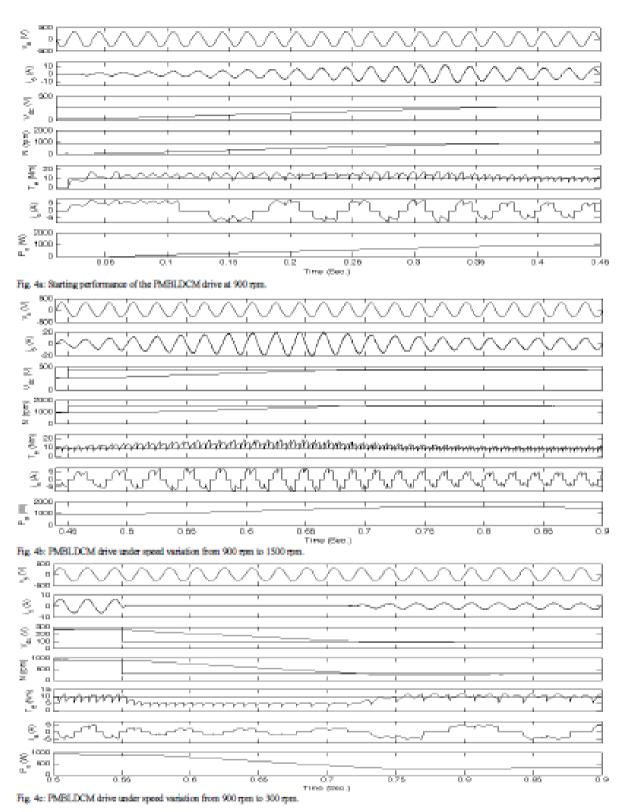


Figure 4. Performance of the Proposed PMBLDCM drive under speed variation at 220 VAC input.

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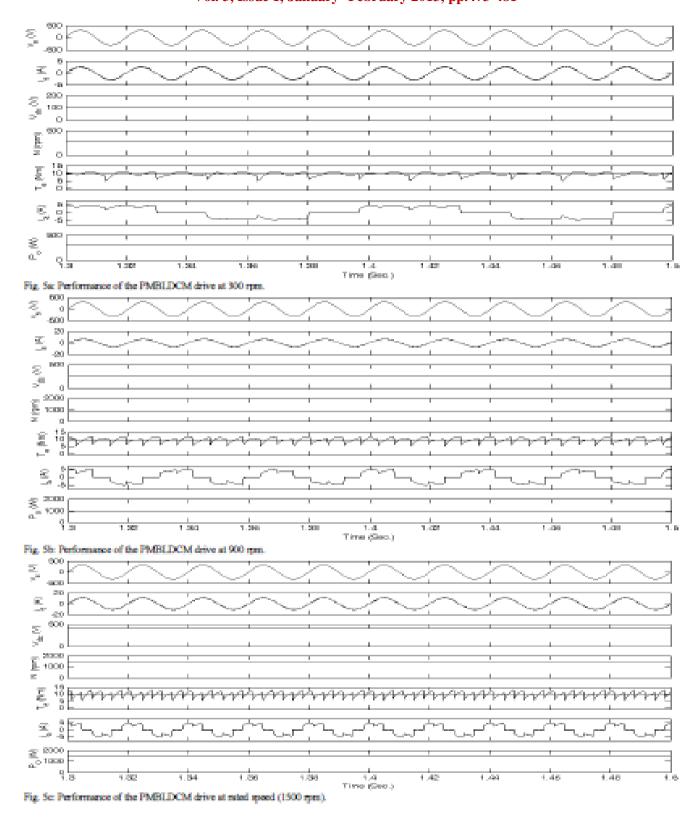


Figure 5. Performance of the PMBLDCM drive under steady state condition at 220 VAC input.

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at constant rated torque (9.55 Nm) and 220 V AC mains supply voltage. These results are categorized as performance during transient and steady state conditions.

- 1) Transient Condition: Figs. 4b-c show the performance of the drive during the speed control of the compressor. The reference speed is changed from 900 rpm to 1500 rpm for the rated load performance of the compressor; from 900 rpm to
- 300 rpm for performance of the compressor at light load. It is observed that the speed control is fast and smooth in either direction i.e. acceleration or retardation with power factor maintained at nearly unity value. Moreover, the stator current of PMBLDCM is within the allowed limit (twice the rated current) due to the introduction of a rate limiter in the reference voltage.
- 2) Steady State Condition: The speed control of the PMBLDCM driven compressor under steady state condition is carried out for different speeds and the results are shown in Figs. 5-6 and Table-II to demonstrate the effectiveness of the proposed drive in wide speed range. Figs.5a-c show voltage (v<sub>s</sub>) and current (i<sub>s</sub>) waveforms at AC mains, DC link voltage (V<sub>dc</sub>), of the motor (N), developed electromagnetic torque of the motor (Te), the stator current of the PMBLDC motor for phase 'a' (I<sub>a</sub>), and shaft power output (P<sub>0</sub>) at 300 rpm, 900 rpm and 1500 rpm speeds. Fig. 6a shows linear relation between motor speed and DC link voltage. Since the reference speed is decided by the reference voltage at DC link, it is observed that the control of the reference DC link voltage controls the speed of the motor instantaneously. Fig.

6b shows the improved efficiency of the drive system ( $\eta$ drive)

in wide range of the motor speed.

### C. Power Quality Performance

The performance of the proposed PMBLDCM drive in terms of various PQ parameters such as THD<sub>i</sub>, CF, DPF, PF is summarized in Table-II and shown in Figs. 7-8. Nearly unity power factor (PF) and reduced THD of AC mains current are observed in wide speed range of the PMBLDCM as shown in Figs. 7a-b. The THD of AC mains current remains less than 5% along with nearly unity PF in wide range of speed as well as load as shown in Table-II and Figs. 8a-c.

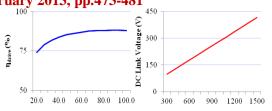


Fig. 6a. DC link voltage with speed Fig.6b. Efficiency with load

Figure 6. Performance of the proposed PFC drive under speed control at rated torque and 220 VAC

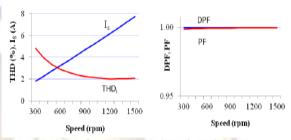


Fig. 7a. THD of current at AC mains Fig. 7b. DPF and PF

Figure 7. PQ parameters of PMBLDCM drive under speed control at rated torque and 220 VAC input

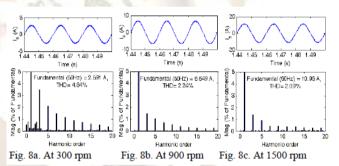


Figure 8. Current waveform at AC mains and its harmonic spectra of the PMBLDCM drive under steady state condition at rated torque and 220 VAC

TABLE III. VARIATION OF PQ PARAMETERS WITH INPUT AC VOLTAGE (VS) AT 1500 RPM (416 VDC)

| VAC        | THDi | DPF    | PF     | CF   | $I_S$ | ηdrive       |
|------------|------|--------|--------|------|-------|--------------|
| <b>(V)</b> | (%)  |        |        |      | (A)   | ( <b>%</b> ) |
| 170        | 2.88 | 0.9999 | 0.9995 | 1.41 | 10.4  | 84.9         |
| 180        | 2.59 | 0.9999 | 0.9996 | 1.41 | 9.7   | 85.8         |
| 190        | 2.40 | 0.9999 | 0.9996 | 1.41 | 9.2   | 86.3         |
| 200        | 2.26 | 0.9999 | 0.9996 | 1.41 | 8.6   | 87.2         |
| 210        | 2.14 | 0.9999 | 0.9997 | 1.41 | 8.2   | 87.6         |
| 220        | 2.09 | 0.9999 | 0.9997 | 1.41 | 7.7   | 88.1         |
| 230        | 2.07 | 0.9999 | 0.9997 | 1.41 | 7.4   | 88.2         |
| 240        | 2.02 | 1.0000 | 0.9998 | 1.41 | 7.1   | 88.4         |
| 250        | 1.99 | 1.0000 | 0.9998 | 1.41 | 6.8   | 88.7         |
| 260        | 2.01 | 1.0000 | 0.9998 | 1.41 | 6.5   | 88.7         |
| 270        | 2.01 | 1.0000 | 0.9998 | 1.41 | 6.2   | 89.0         |

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### 6.CONCLUSION

A new speed control strategy of a PMBLDCM drive is validated for a compressor load of an air conditioner which uses the reference speed as an equivalent reference voltage at DC link. The speed control is directly proportional to the voltage control at DC link. The rate limiter introduced in the reference voltage at DC link effectively limits the motor current within the desired value during the transient condition (starting and speed control). The additional PFC feature to the proposed drive ensures nearly unity PF in wide range of speed and input AC voltage. Moreover, power quality parameters of the proposed PMBLDCM drive are in conformity to an International standard IEC [5]. 61000-3-2 The proposed drive has demonstrated good speed control with energy efficient operation of the drive system in the wide range of speed and input AC voltage. The proposed drive has been found as a promising candidate for a PMBLDCM driving Air-Con load in 1-2 kW power range.

## **APPENDIX**

Rated Power: 1.5 kW, rated speed: 1500 rpm, rated current: 4.0 A, rated torque: 9.55 Nm, number of poles: 4, stator resistance (R): 2.8  $\Omega$ /ph., inductance (L+M): 5.21mH/ph., back EMF constant (Kb): 0.615 Vsec/rad, inertia (J): 0.013 Kg- m<sup>2</sup>. Source impedance (Z<sub>S</sub>): 0.03 pu, switching frequency of PFC switch (f<sub>S</sub>) = 40 kHz, capacitors (C<sub>1</sub>= C<sub>2</sub>): 15nF, PI speed controller gains (K<sub>p</sub>): 0.145, (K<sub>i</sub>): 1.45.

#### REFERENCES

- [1] T. Kenjo and S. Nagamori, *Permanent Magnet Brushless DC Motors*, Clarendon Press, oxford, 1985.
- [2] T. J. Sokira and W. Jaffe, Brushless DC Motors: Electronic Commutation and Control, Tab Books USA, 1989.
- [3] J. R. Hendershort and T. J. E. Miller, Design of Brushless Permanent- Magnet Motors, Clarendon Press, Oxford, 1994.
- [4] J. F. Gieras and M. Wing, *Permanent Magnet Motor Technology Design and Application*, Marcel Dekker Inc., New York, 2002.
- [5] Limits for Harmonic Current Emissions (Equipment input current ≤16 A per phase), International Standard IEC 61000-3-2, 2000.
- [6] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters,"

- *IEEE Trans. Industrial Electron.*, vol. 50, no. 5, pp. 962 981, oct. 2003.
- [7] N. Mohan, T. M. Undeland and W. P. Robbins, "Power Electronics: Converters, Applications and Design," John Wiley, USA, 1995.
- [8] A. I. Pressman, Switching Power Supply Design, McGraw Hill, New Yor k. 1998.
- [9] P.J. Wolfs, "A current-sourced DC-DC converter derived via the duality principle from the half-bridge converter," *IEEE Trans. Ind. Electron.*, vol. 40, no. 1, pp. 139 144, Feb. 1993.
- [10] J.Y. Lee, G.W. Moon and M.J. Youn, "Design of a power-factor- correction converter based on half-bridge topology," *IEEE Trans. Ind. Electron.*, vol. 46, no. 4, pp.710 723, Aug 1999.
- [11] J. Sebastian, A. Fernandez, P.J. Villegas, M.M. Hernando and J.M. Lopera, "Improved active input current shapers for converters with symmetrically driven transformer," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 592 600, March-April 2001.
- [12] A. Fernandez, J. Sebastian, M.M. Hernando and P. Villegas, "Small signal modelling of a half bridge converter with an active input current shaper," in *Proc. IEEE PESC*, 2002, vol.1, pp.159 164.
- [13] S.K. Han, H.K. Yoon, G.W. Moon, M.J. Youn, Y.H. Kim and K.H. Lee, "A new active clamping zero-voltage switching PWM current-fed half-bridge converter," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1271 1279, Nov. 2005.
- [14] R.T.Bascope, L.D.Bezerra, G.V.T.Bascope, D.S. Oliveira, C.G.C. Branco, and L.H.C. Barreto, "High frequency isolation on-line UPS system for low power applications," in *Proc. IEEE APEC'08*, 2008, pp.1296 1302.