

## Design and implementation of MAC Transmitter for the transmission of UDP packet using FSM and verilog coding techniques

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### Abstract

The purpose of this paper is to design and develop a MAC Transmitter on Field Programmable Gate Arrays (FPGA) that converts 32 bit data in to 4 bit DATA for transmitter. The data which is used for transmission is UDP Packet. The entire UDP packet will go as data for MAC frame. In this paper we design the Ethernet (IEEE 802.3) connection oriented LAN Medium Access Control Transmitter (MAC). It starts by describing the behavior of MAC circuit using Verilog. A synthesized Verilog model of the chip is developed and implemented on target technology. This paper will concentrate on the testability features that increase product reliability. It focuses on the design of a MAC Transmitter chip with embedded Built-In-Self-Test (BIST) architecture using FPGA technology.

**Keywords**—UDP,MAC, IEEE 802.3

### 1.INTRODUCTION :

User Datagram Protocol (UDP) is a transport layer protocol that supports Network Application. It layered on just below the 'Session' and sits above the IP(Internet Protocol) in open system interconnection model (OSI). This protocol is similar to TCP (transmission control protocol) that is used in client/ server programs like video conference systems expect UDP is connection less.Unlike TCP, UDP doesn't establish a connection before sending data, it just sends. Because of this, UDP is called "Connectionless". UDP packets are often called "Datagrams. It's a transport layer protocol. This section will cover the UDP protocol, its header structure & the way with which it establishes the network connection.

UDP is a connectionless and unreliable transport protocol. The two ports serve to identify the end points within the source and destination machines. User Datagram Protocol is used, in place of TCP, when a reliable delivery is not required. However, UDP is never used to send important data such as web-pages, database information, etc. Streaming media such as video ,audio and others use UDP because it offers speed.

The reason UDP is faster than TCP is because there is no form of flow control. No error checking, error

correction, or acknowledgment is done by UDP.UDP is only concerned with speed. So when, the data sent over the Internet is affected by collisions, and errors will be present. UDP packet's called as user datagrams with 8 bytes header. A format of user datagrams is shown in figure below. In the user datagrams first 8 bytes contains header information and the remaining bytes contains data.

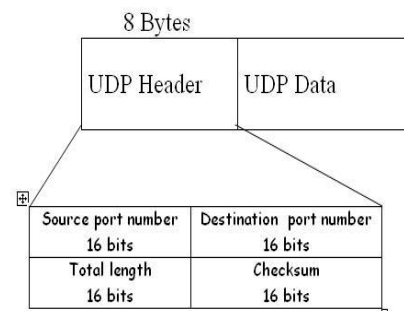
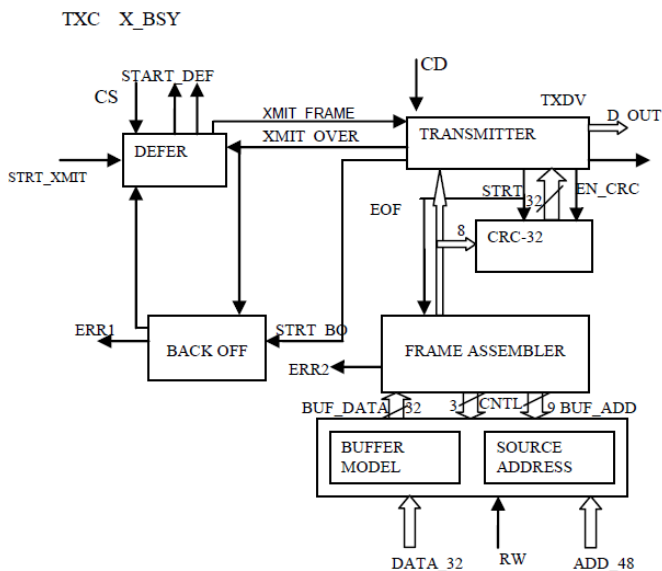


Figure: UDP Frame Format

The Media Access Control (MAC) data communication protocol sub-layer, also known as the Medium Access Control, is a part of the data link layer specified in the seven-layer of OSI model (layer 2). It provides addressing and channel access control mechanisms that make it possible for several terminals or network nodes to communicate within a multipoint network, typically with a local area network (LAN) or metropolitan area network (MAN). A MAC protocol is not required in full-duplex point-to-point communication. In single channel point-to-point communications full-duplex can be emulated. This emulation can be considered a MAC layer. The MAC sublayer acts as an interface between the Logical Link Control sub layer and the network's physical layer. The MAC layer provides an addressing mechanism called physical address or MAC address. This is a unique serial number assigned to each network adapter, making it possible to deliver data packets to a destination within a sub network, i.e. a physical network without routers, for example an Ethernet network. FPGA area and speed optimization to implement computer network protocol is subject of research mainly due to its importance to network performance. The objective

of resource utilization of field programming gate array (FPGA) is to allocate contending to embed maximum intricate functions. This approach makes design cost effective and maximizing IEEE 802.3 MAC performance. Binary exponential back off algorithm. Verilog coding to implemented synchronous counter and FSM coding style influence performance of MAC transmitter[1][3].However effective VHDL coding style optimizes FPGA resource allocation for area and speed performance of IEEE 802.3 MAC transmitter can be optimized using linear feedback shift register, one hot finite machine (FSM) state encoding style.

## 2.MAC TRANSMITTER:



### Block diagram of MAC Transmitter

On receiving „STRT\_XMIT. from the upper layer (LLC) this Block makes the X\_BUSY. signal active and starts the process of monitoring the channel for CARRIER SENSE.. This process is called DEFER. The signal CARRIER SENSE. is provide the physical layer. It monitor the channel for inter-frame gap period, which.s 96 bit period. The period is split up into two different slot 60 bit period and 36-bit period[1].During the 60-bit period if it receives CARRIER SENSE. as active then the timer is restarted. After 60 bit time period is elapsed, the transmitter does not monitor CARRIER SENSE. for next 36 bit period[1] and gives the signal XMIT\_FRAME.. Once the transmission is started it waits for XMIT\_OVER. or START\_DEF to be asserted and goes to start of defer when either is asserted.

## 3.OPTIMIZATION IMPLEMENTATION OF BACK OFF:

When a transmission attempt has been terminated due to collision, it is retired by the transmitter until it is successful or a maximum

number of sixteen attempts have been made. The scheduling of the retransmission is determined by a controlled randomization process known as “Truncated Binary Exponential Back Off”[1][4]. After the end of enforcing a Collision (jamming), the transmitter delay before attempting to retransmit the frame delay is an integer multiple of slot times to delay before the retransmission attempt is chosen as a uniformly distributed random integer  $r$  in the range.

$$0 \leq r \leq 2^k$$

Where

$$K = \min(n, 10)$$

If all attempt limit fails. This event is reported as an error

## 4. IMPLEMENTATION OF BACK OFF WITH FINITE STATE MACHINE BASED APPROACH:

The function of a frame assembler is to contain the information of the different components of the frame viz .destination address, source address and data, and supply this to the transmitter as well as the CRC block. Hence, the frame Assembler assembles all the fields over which FCS is determined [8]. The Frame Assembler block is controlled by the transmitter block through the STRT signal. This signal is low when the transmitter is idle. The STRT signal function as an enable for the Frame Assembler assembles block. The buffer width is 32 bits. Since the entire frame data is assumed to be present inside the MAC, the Buffer has to accommodate at least 1500 bytes, which is the maximum data size in an 802.3 frame. Here, it is assumed that the entire data contents of a frame reside with the MAC before transmission. In order to address a 32 wide buffer of 1500 bytes a 9 bit address is required. The CNTRL (2) is connected to RD pin of the buffer while CNTRL (1) and CNTRL(0) controls data to be read from either buffer location of the source address register(1).

Table 1. CNTRL data

CNTRL[2:0]	BUF DATA
011	Source Address (47 to 16)
001	Source Address(15 to 0) on the higher 16 bits
101	Buffer Data

The function of a frame assembler is to construct the 802.3 frame from the following

1. Destination address stored in first 6 bytes of buffer.
2. Source address that is hardwired onto the MAC
3. Length stored in the lower word of the second location of buffer
4. Data bytes stored in the subsequent buffer location

5. Pad bytes if length is less than 46 bytes to make up a total of 46 bytes of data and pad

Hence the frame Assembler is tested as follows :-

1. The buffer is filled with some destination address and a length. A source address is also stored in its register.
2. The subsequent buffer location are filled with randomly generated data vectors
3. The frame assembler is activated by the STRT signal.
4. The byte output of the frame assembler is stored into an output file through textio
5. The frame generated is analyzed to isolate its individual components viz. destination Address,Source Address, Length data + Pad. Each field is verified for correct operation. The total length of the data must match the length specified in the length field for length between 46 and 1500,where as it should be 46 bytes including data and padding for length field or less than 46. if the length specified is greater than 1500 the frame Assembler should generate an error condition and exit. The Frame Assembler is tested for the following length

Conditions

Length=0, Length<46, Length=46, Length>46,and <1500

Length =1500, Length <1500

### 5. OPTIMIZATION IMPLEMENTATION OF TRANSMITTER:

On receiving „STRT\_XMIT active from DEFER block this starts transmitting 4 bits at a time. At the same time it gives signal Transmit Valid (TXDV) to the physical layer. First it transmit 7-byte of Preamble then 1 byte of Start Frame Delimiter(SFD) is transmitted and it also gives STRT signal to Frame Assembler until it receive END of Frame(EOF) signal from the Frame Assembler. Then it transmits 32 bit of CRC and give the signal„Transmit Over (XMIT\_OVER) to DEFER block and de-assert the signal TXDV and STRT. Since CRC block works on bytes. Frame Assembler gives 8-bit of data at the output. Where as ,Transmitter give nibble at the output so it reads from Frame Assembler. After 2 clock cycles(Frame Assembler) Block also give output on every 2 clock cycles. This block also monitor the signal collision Detector(CD) provided by the physical layer. If it detects CD during transmitting Preamble then it completes transmitting Preamble and then it transmits 4 bytes of JAM sequence. It also asserts the signal Start Back Off (STRT\_BO) and de-assert signal STRT.If collision is detected anywhere else then Preamble then„Transmitter stops transmitting and sends JAM sequence.It also asserts the signal Start Back Off(STRT\_BO) and dessert signal STRT.

### 6.CRC Generator:

A Cyclic Redundancy Check [CRC] is used by the transmit

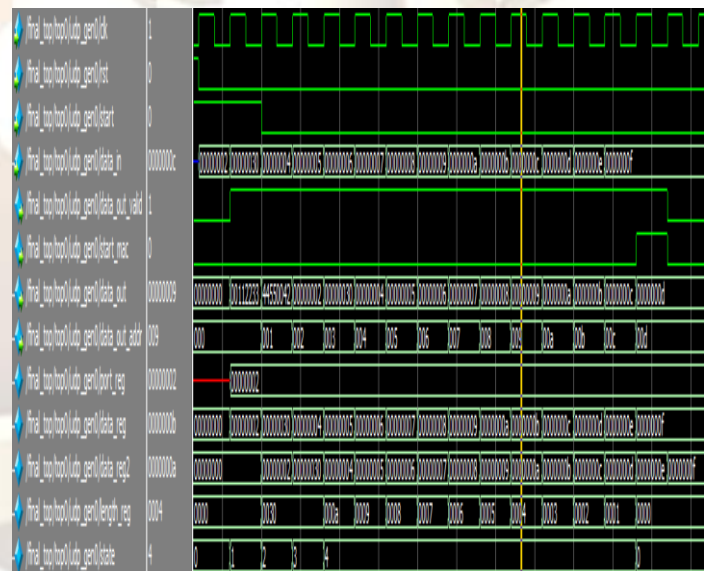
and receive algorithms to generate a CRC value for the FCS field, The frame check sequence [FCS] field contains a 4-octet CRC value, This value is computed as a function of the contents of the Source Address, Destination Address , Length, LLC data and pad. The encoding is defined by the following generating polynomial:

$$X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+ X^4+X^2+X^1+1 [4]$$

Mathematically, the CRC value corresponding to a given frame is defined by the following procedure[4].

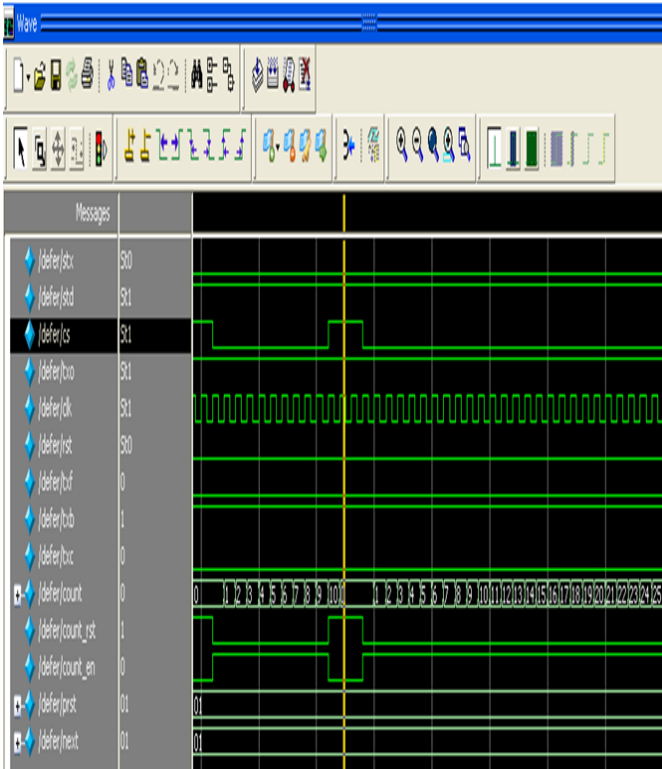
1. The first 32 bits of the farm are complemented.
2. The n bits of the frame are then considered to be thecoefficient of a polynomial M[x] of degree [n-1]. (The first bit of the destination Address field corresponds to the X (n-1). term and last bit of data field corresponds to the X term)
3. M (x) is multiplied by X<sup>32</sup> and divided by G (x) , producing a remainder R(x) of degree < 31 .
4. The coefficients of R (x)are considered to be a32-bit sequence.
5. The bit sequence is completed and the results the CRC

### 7. SIMULATION RESULTS

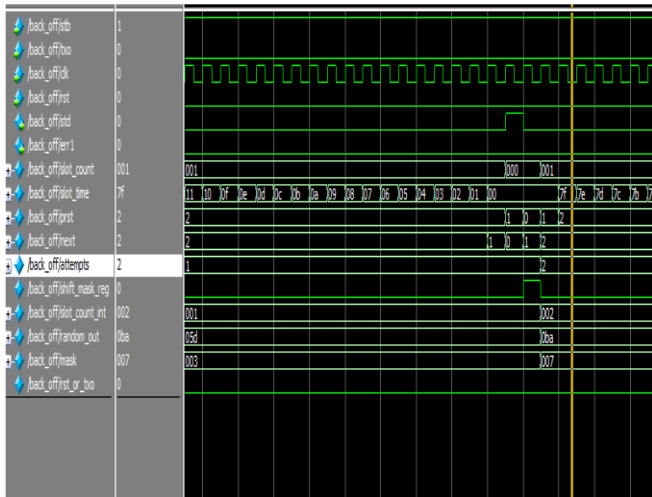


### UDP SIMULATION RESULTS

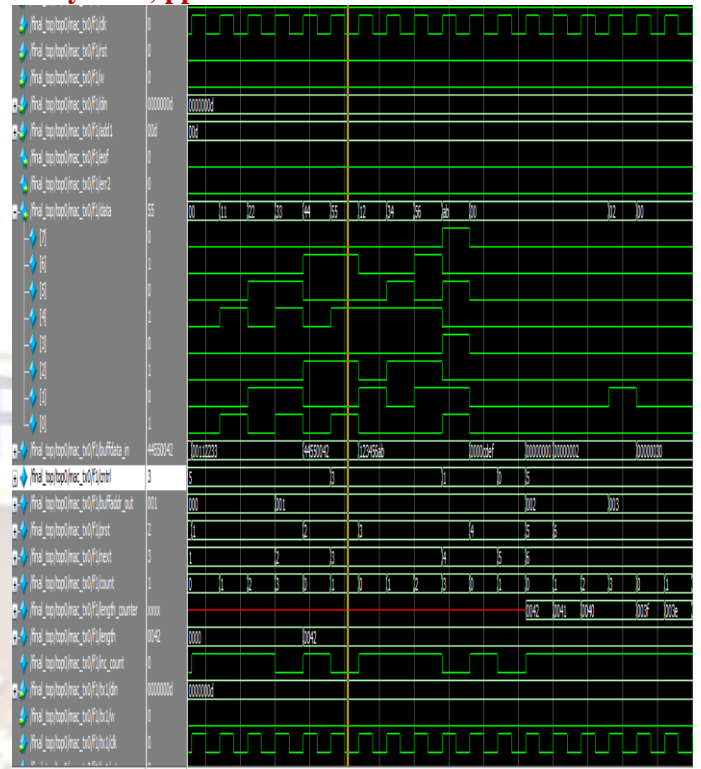




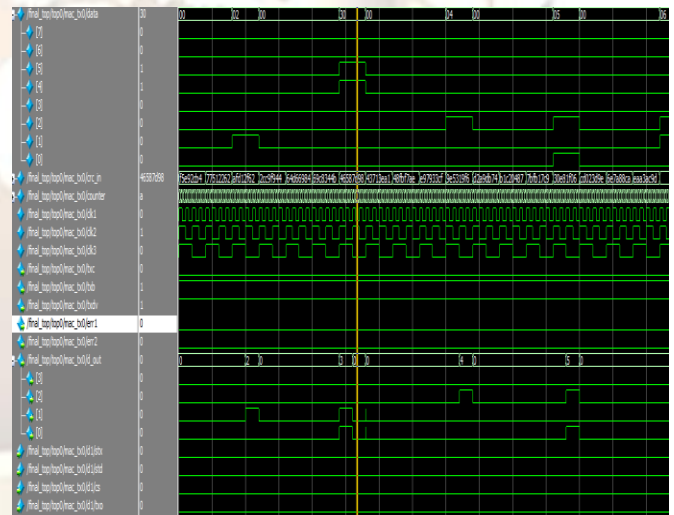
**DEFER SIMULATION RESULTS**



**BACK OFF SIMULATION RESULTS**



**FRAME ASSEMBLER SIMULATION RESULTS**



**TRANSMITTER SIMULATION RESULTS**

**8. CONCLUSIONS:**

The data which is sent through UDP packet is transmitted by the transmitter. The Verilog Implementation of MAC gives the improved digital design process, especially for FPGA design. A hardware description language allows a digital system to be designed and debugged at a higher level before conversion to the gate and flip-flop level. One of the most popular hardware description languages is Verilog .It is used to describe and simulate the operation of variety IEEE 802.3

systems. This paper has covered and discussed a software design, and implementation of a basic IEEE 802.3 (MAC Transmitter) system. The speed of data transmission is very high & it gives proper CRC bit for receiving correct data. The simulated waveforms give the reliability of the Verilog implementation to describe the characteristics and the architecture of the designed MAC with embedded BIST. The simulated waveforms also have shown the observer how long the test result can be achieved by using the Built- In-Self-Test technique (BIST) is completed at 39.2ms using 25 MHz clock speed transmitting at 100 Mbps. Even though it seems not to be as fast as it should be when BIST is implemented (the receiver needs to wait the signal from the transmitter), the MAC Transmitter module still takes advantage of the 100% fault coverage. This is the most important thing that should not be left out by any designer to ensure the reliability of their design. The next target for this research is to verify the RTL, implement and download it on Xilinx's FPGA chip.

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