

## Optimal Design Of CMOS Op- Amp Using Geometric Programming

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### ABSTRACT

The problem of CMOS op-amp circuit sizing is addressed here. Given a circuit and its performance specifications, the goal is to automatically determine the device sizes in order to meet the given performance specifications while minimizing a cost function, such as a weighted sum of the active area and power dissipation. The approach is based on the observation that the first order behavior of a MOS transistor in the saturation region is such that the cost and the constraint functions for this optimization problem can be modeled as posynomial in the design variables. The problem is then solved efficiently as a convex optimization problem. Second order effects are then handled by formulating the problem as one of solving a sequence of convex programs. Numerical experiments show that the solutions to the sequence of convex programs converge to the same design point for widely varying initial guesses. This strongly suggests that the approach is capable of determining the globally optimal solution to the problem. Accuracy of performance prediction in the sizing program (implemented in MATLAB) is maintained by using a newly proposed MOS transistor model and verified against detailed SPICE simulation.

### INTRODUCTION

The current trend in microelectronics is to integrate a complete system that previously occupied one or more boards on one or a few chips. Although most of the functionality in an integrated system is implemented in digital circuitry, analog circuits are needed to interface between the core digital system and the real world. Analog interface circuits have, thus, become vital and indispensable parts of most digital circuits. They provide the necessary signal conditioning and modification so that they can be processed digitally. Interface circuits span a wide variety of functions and applications such as data acquisition systems, A/D and D/A converters, particle and radiation detection circuits, automotive electronics, biomedical instrumentation and control circuits, robot sensing, industrial process monitoring, implantable biomedical instruments, preamplifiers, compressors, power drivers, etc. Therefore, to realize an

integrated system on a single chip, the digital and analog circuits are combined together. This integration of analog and digital circuits results in so called mixed-signal integrated circuits. Though in an integrated system, the analog circuitry occupies a small physical area compared to the digital counterpart and becomes the bottleneck in design time reduction. The main reason for this is that the number of performance functions in an analog circuit is much larger than that in a digital circuit. Further, analog performances are very sensitive to the design variables and variation in the performance across the design space is quite high. Increase of design complexity and, at the same time, demand of design cycle time reduction due to highly competitive market can be managed only by the use of computer aided design. CAD tools specifically made to analog integrated circuit design promise to improve the design process in a variety of ways:--

- 1) By shortening design times:
- 2) By simplifying the design process:
- 3) By improving the likelihood of error-free designs from the first fabrication run:
- 4) By reducing design and production cost:
- 5) By improving manufacturing yield:
- 6) By allowing easier tracking of fabrication processes

### Design Formulation for Two-Stage CMOS OP-AMP Sizing

Two stage refers to the number of gain stages. First gain stage is a differential input single ended output stage. The second gain stage is normally a common source gain stage that has an active load. Capacitor  $C_c$  is included to ensure stability when the op-amp is used with feedback. Because  $C_c$  is between the input and the output of the high gain second stage, it is often called Miller capacitance. Since its effective capacitive load on the first stage is larger than its physical value In the class of two-stage op-amps, there is a basic structural similarity, namely the hierarchical structure of different configurations is the same. It is only the sub circuits, which are the leaf cells of the hierarchy that are different across the various topologies. A two-stage op-amp consists of an input stage, a second stage, and a compensating circuit. The input stage has three parts:--

1. Current Source,
2. Differential Pair
3. Current Mirror.

The second stage has two parts:--

1. Transconductance Amplifier
2. Active Load.

Each one of the four sub circuits, namely differential pair, current mirror, transconductance amplifier, and active load, can be either simple or cascoded. For a cascoded current mirror, a level shifter is required between the input stage and the second stage. The compensating circuit consists of a capacitor and a resistor. The transistors in the differential pair can either be n-type or p-type. The choice of polarity of the transistors in the differential pair also determines the polarity of the transistors in the other subcircuits.

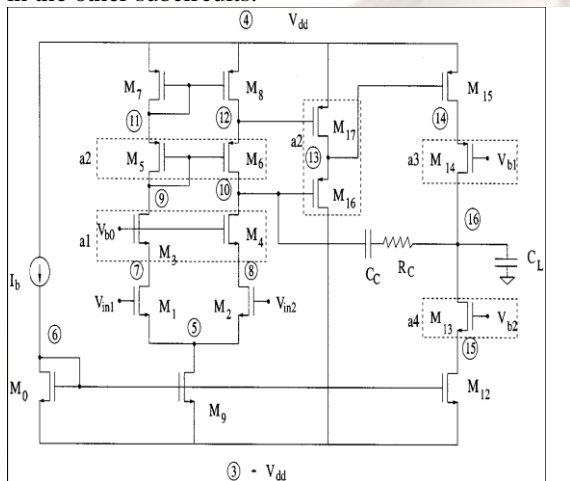


Fig .Two Stage CMOS Op-Amp

### Basic geometric programming

#### Monomial and posynomial functions

Let  $x_1, \dots, x_n$  denote  $n$  real positive variables and  $x = (x_1, \dots, x_n)$  a vector with components  $x_i$ . A real valued function  $f$  of  $x$ , with the form

$$f(x) = cx_1^{a_1} \dots x_n^{a_n} \quad (1)$$

where  $c > 0$  and  $a_i \in \mathbb{R}$ , is called a monomial function, or more informally, a monomial (of the variables  $x_1, \dots, x_n$ ). Constant  $c$  is referred as the coefficient of the monomial, the constants  $(a_1, \dots, a_n)$  are referred as the exponents of the monomial. Any positive constant is a monomial, as is any variable. Monomials are closed under multiplication and division i.e. if  $f$  and  $g$  are both monomials then so are  $f^*g$  and  $f/g$ . (This includes scaling by any positive constant.) A monomial raised to any power is also a monomial:-

$$f(x)^{\gamma} = (cx_1^{a_1} \dots x_n^{a_n})^{\gamma}$$

The term 'monomial', which is used here (in the context of geometric programming) is similar to, but differs from the standard definition of 'monomial' used in algebra. In algebra, a monomial has the form (1), but the exponents  $a_i$  must be nonnegative integers, and the coefficient  $c$  is one.

A sum of one or more monomials, i.e., a function of the form

$$\sum_{k=1}^K f(x) = \sum_{k=1}^K c_k x_1^{a_{1k}} \dots x_n^{a_{nk}} \quad (2)$$

where  $c_k > 0$ , is called a posynomial function or, a posynomial (with  $K$  terms, in the variables  $x_1, \dots, x_n$ ). The term 'posynomial' is meant to suggest a combination of 'positive' and 'polynomial'. Any monomial is also a posynomial. Posynomials are closed under addition, multiplication, and positive scaling. Posynomials can be divided by monomials (with the result also a posynomial) i.e. if  $f$  is a posynomial and  $g$  is a monomial, then  $f/g$  is a posynomial. If  $\gamma$  is a nonnegative integer and  $f$  is a posynomial, then  $f^{\gamma}$  is a posynomial (since it is the product of  $\gamma$  posynomials).

#### Standard form geometric program

A geometric program (GP) is an optimization problem of the form

$$\begin{aligned} &\text{minimize } f_0(x) \\ &\text{subject to } f_i(x) \leq 1; i = 1, \dots, m; \\ &g_i(x) = 1; i = 1, \dots, p; \end{aligned} \quad (3)$$

where  $f_i$  are posynomial functions,  $g_i$  is monomials, and  $x_i$  is the optimization variables. (There is an implicit constraint that the variables are positive, i.e.,  $x_i > 0$ .) We refer to the problem (3) as a geometric program in standard form. In a standard form GP, the objective must be posynomial (and it must be minimized) the equality constraints can only have the form of a monomial equal to one, and the inequality constraints can only have the form of a posynomial less than or equal to one. We can switch the sign of any of the exponents in any monomial term in the objective or constraint functions, and still have a GP. But if we change the sign of any of the coefficients, or change any of the additions to subtractions, the resulting problem is not a GP.

### RESULTS

The CMOS op-amp sizing technique described has been implemented in MATLAB for two stage CMOS op-amp. In the implementation, convex programming problem is solved by using the sequential quadratic programming method which is available in optimization toolbox. Experimental results are given below. Table 1 consists of spice

simulation results using optimal design point variables against various given specifications.

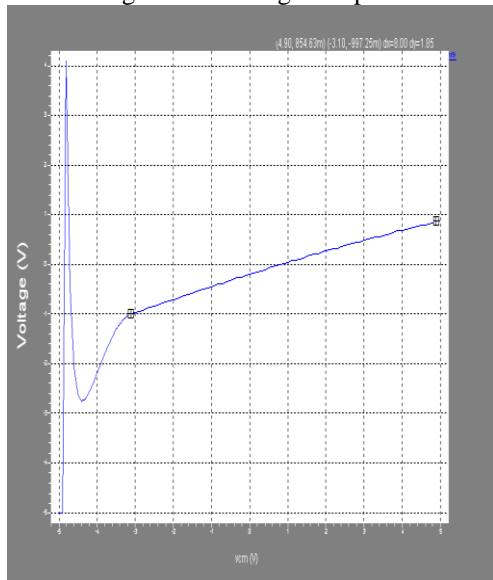


Figure5 : Common Mode Range

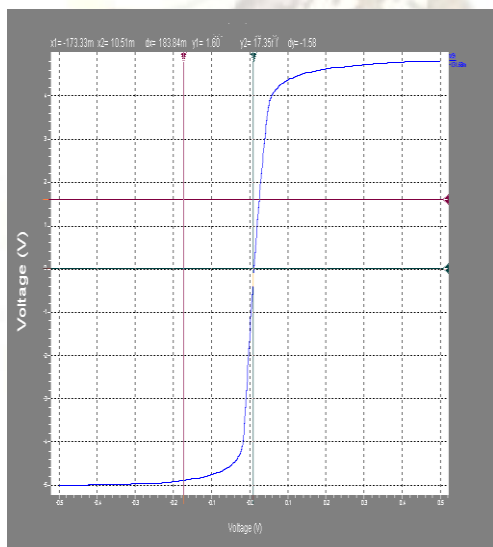


Figure6 : Input Offset Voltage

## CONCLUSION

An efficient technique for sizing CMOS op-amps is used. The main concept in this approach is that the CMOS op-amp sizing problem can be formulated as a sequence of (convex)geometric programs. Such a formulation has two major advantages as enumerated below:--

- 1) Since the convex programming problem is very well understood, it is very straight forward to solve it in a robust and computationally efficient manner.
- 2) The sequence of solutions generated is a sequence of global optimal of convex programming sub problems. It suggests that the point to which this sequence converges is the globally optimal solution of the original problem. This is supported by experimental results, where it is shown that the

method converges to the same final design point for widely varying initial design points. This is achieved by modeling  $V_{GT}$ ,  $g_m$ , and  $g_d$  as a PoP function of the transistor sizes and the bias current at a “relaxed” estimate of the dc operating point. Because of this iterative formulation, as the iterant proceed and approach convergence, the coefficient and powers of the first-order PoP model are made accurate via the use of second order model functions. Restricting the devices to operate in the saturation region is done because in standard CMOS op-amp design, the mosfets that are used as loads or amplification devices are biased in the saturation region for, among other reasons, the low  $g_d$  that is achievable in this region. There are specific exceptions to this rule, e.g., when a parallel connection of an NMOS and PMOS device is used to build a resistor, or the common mode feedback transistor in a fully differential two-stage op-amp. SCP (Sequential Convex Programming) approach can be applied to MOS circuits without concerning about the region of operation of the individual devices, or even for bipolar circuits if the iterative model-optimize approach is applied appropriately. For this it is required that the derived device parameters, e.g.,  $g_m$  and  $g_d$ , be modeled as PoP functions of the independent design variables and that these PoP models become accurate approximations of the original device models as the iterants converge. There are certain performance metrics like settling time, which cannot be modeled as a suitable analytic function. While it is possible to meet a given settling time specification by suitably constraining slew rate, unity gain frequency, and phase margin (which are modeled as posynomials). Effort required to derive analytic expressions of performance metrics (for a new op-amp) is a hindrance to the widespread use of techniques such as described here but this hurdle should be crossed in order to bring the major advantages of convex optimization into a truly automated circuit-sizing tool.

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