

## Study And Analysis Of Low Power Low Voltage Pipeline Architecture Of ADC Using 0.18 $\mu\text{m}$ Technology

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### ABSTRACT

This paper is concerned with improving the efficiency of analog to digital converters (ADCs). the fast advancement of CMOS fabrication technology, more and more signal-processing functions are implemented for a lower cost, lower power consumption, and higher yield. The design of analog-to-digital converters is one of the most critical and challenging aspects in the development of new and more powerful electronic systems, In this thesis design of 3 bit Pipeline ADC using 0.18 micrometer CMOS technology and The schematic of the various circuits drawn in Tanner SEdit and the simulation waveforms obtained using Tanner WEdit have been included.

### I. INTRODUCTION

Reduction of the power dissipation associated with high speed sampling and quantization is a major problem in many applications, including portable video devices such as camcorders, personal communication devices such as wireless LAN transceivers, in the read channels of magnetic storage devices using digital data detection, and many others . In the past, high-speed A/D converters required for these applications in the sampling rate range above 5 Msample/sec (MS/s) with 8 to 12 bit of resolutions have consumed large power ranging typically from 100 mW to 500 mW. For battery-powered portable applications this level of power consumption may not be suitable and further power reduction is essential for power-optimized A/D interfaces.

Low voltage operation is another important key factor in these portable A/D interface environments. With the trend that A/D interfaces are incorporated as a cell in complex mixed-signal ICs containing mostly digital blocks for DSP and control, the use of the same supply voltage for both analog and digital circuits can give advantages in reducing the overall system cost by eliminating the need of generating multiple supply voltages with DC-DC converters. Therefore, in order to be compatible with low-voltage systems, a new generation of A/D converters that can operate at supply voltage below 5 V is desired.

With recent improvements on higher speed and higher integration capability of the scaled technologies, a CMOS technology is becoming

increasingly attractive as a cost effective solution for many applications once reserved for bipolar or other fast technologies. This trend is expected to continue with scaled sub-micron CMOS technologies.

Among many types of CMOS A/D converter architectures, a pipeline architecture can achieve good high input frequency dynamic performances and as a high throughput as the flash ADC due to a S/H circuit in each stage of the pipeline for concurrent processing . In this dissertation, both fundamental and practical limitations to the power dissipation in CMOS A/D converters are examined, and techniques to allow low power and low voltage operation of the pipeline architecture are described. To verify the effectiveness of the techniques, a 3 bit pipeline A/D converter is designed using 0.18  $\mu\text{m}$  CMOS technology.

### II. PIPELINE ARCHITECTURE:

Pipeline ADC is a popular architecture for data conversion schemes which require a compromise between speed and accuracy. Although the pipeline architecture is inherently not as fast as a flash scheme, its serial nature results in a linear scaling of power and area with resolution apposed to the exponential scaling which occurs in a flash, resulting in the pipeline architecture being a more attractive solution around and above the 9 bit level. Similarly, for very high resolution schemes sigma delta architectures are generally used, however the over-sampling nature of such schemes limits the maximum speed to a fraction of the fastest possible sampling rate. However the concurrent nature of a pipeline removes the over-sampling required, in effect converting the over-sampling speed limit into a latency problem. The pipeline converter architecture consists of high speed, low resolution cascaded stages to obtain a final conversion. Only a brief overview of the pipeline converter is discussed here, for a more detailed description. Figure 2.4 shows a block diagram of a general pipeline with k stages. The output of each stage is digitally corrected to obtain an accurate digital output. The advantages of breaking down the conversion into many stages are:

1. Key advantage is high conversion rate. There is one complete conversion per clock cycle.

2. Overall chip size is reduced because the sample rate is not governed by the number of pipeline stages.

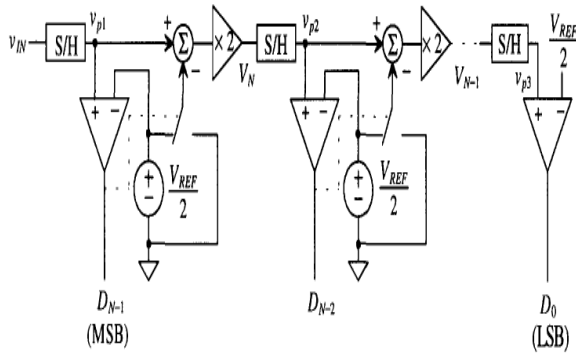


Figure 2.4 Block diagram of pipeline ADC

3. If chip space is available additional stages can be added for increased resolution.
4. The major disadvantage of Pipeline architecture is an inherent sampling latency.
5. By combining the merits of the successive approximation and flash ADCs this type is fast, has a high resolution, and only requires die size.

#### Disadvantage

The disadvantage of adding the gain blocks is that they tend to be the dominant source of power dissipation in the ADC. Therefore, pipelined ADCs tend to dissipate more power than sub ranging ADCs. However, like the other sub ranging ADCs, pipelined ADCs can achieve high resolutions with relatively little hardware. Furthermore, mismatches can easily be eliminated as a limitation to resolution by self-calibration techniques.

### III. EQUATIONS

#### CALCULATION OF $V_{IL}$

$$V_{IL} = 2V_Y + V_{T.O.P} - V_{DD} + \frac{K_R \cdot V_{T.O.n}}{1 + K_{RC}} V_{IH}$$

#### ALCULATION OF $V_{IH}$

$$V_{IH} = V_{DD} + V_{T.O.P} + \frac{K_R(2V_Y + V_{T.O.n})}{1 + K_R}$$

#### CALCULATION OF $V_{TH}$

$$V_{TH} = V_{T.O.n} + \frac{(V_{DD} + V_{T.O.P})}{\sqrt{K_R(1 + \sqrt{1/K_R})}}$$

### IV. RESULTS

The simulations results of sine wave in 3 bit pipeline architecture of ADC with operating voltage 3V and sampling rate is 80 MHz and input frequency is 1MHz.

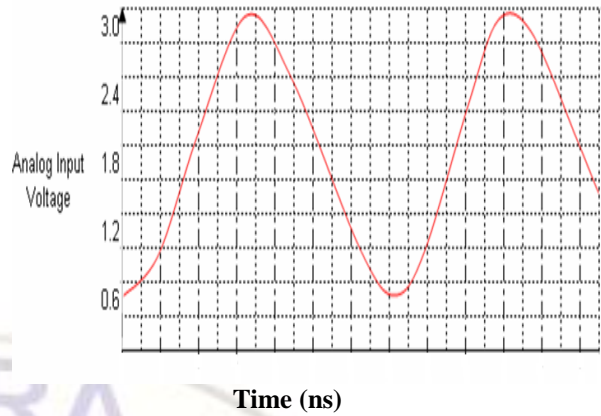


Fig : Input voltage signal of 3 bit pipeline ADC.

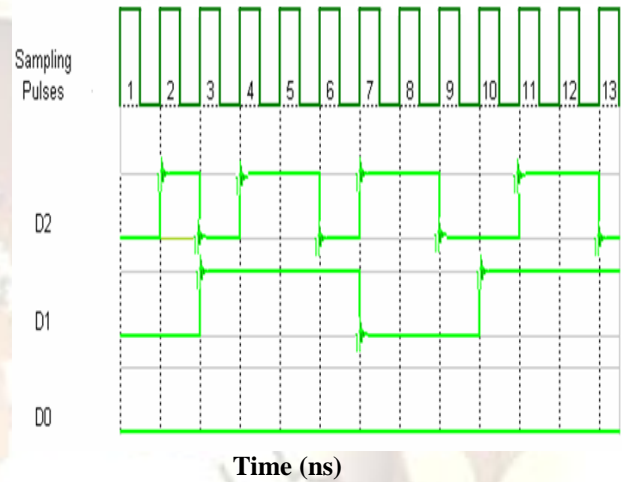


Fig : Output voltage signal of 3 bit pipeline ADC.  
 Fig: Waveform obtained after the transient analysis of 3 bit pipeline ADC.

The Figure shows the transient analysis of 3 bit pipeline ADC. Sine wave is the input pulse signal applied with amplitude 3V and the output taken is D0, D1, D2 as shown in Figure 4.5. when input is applied to the circuit then it sampled by sampling pulses where we want to out put. Then output is find across D0, D1, D2. First bit of the signal is find across D0, and second from D1, and third across D2 in a continue manner. For example if sampling pulses sample the signal at 2V then out from D0 is 0 and output from D1 is 1 and output from D2 is 0. Error in the wave form due to nonideal characteristics is the offset of the comparator. When the comparator computes the difference of between the two input signals, an internal offset voltage is added to this difference. Thus, when the two inputs are close together, the comparator may make a wrong decision. And due to KT/C noise in sample and hold circuit.

### V. CONCLUSION

This thesis presents a detailed study of design analysis of the pipeline architecture of ADC with 3 bit of resolution and 80MS/s nominal conversion rate using 0.18μm CMOS technology.

Initially our work describes the study of design of low voltage low power pipeline architecture of ADC using individual blocks of latch comparator, sample and hold circuit, two stage op amp, clock circuitry.

The two stage Opamp was designed for a gain of 80 dB and phase margin and unity gain bandwidth of 400MHz at a load capacitance 1pF. The sample and hold circuit designed using this Opamp gave a maximum settling time of about 120ns. Noise analysis should be performed to get the required capacitor values so that the SFDR requirements could be met. The design of the latched comparator with high sampling frequency and analog bandwidth. And it doesn't require high gains but works on the principle of positive feedback the values of  $V_{ref+}=2v$  and  $V_{ref-}=-2V$ .

Considerable improvement in the parameters is observed when it is compared with the other architecture of ADC. A comparison among the pipeline ADC is done using the simulated results. The simulation waveforms of all the above mention circuits is done using tanner simulation tool WEdit. Table II lists the performance of some high speed ADC appeared in the literature. In comparison with reported ADC, the pipelining ADC achieves high sampling frequency with relatively low power consumption. This thesis provides a considerable insight into the overall operation and advantages of pipeline architecture of ADC.

In this project the prototype ADC was built using two stage amplifiers in order to simultaneously achieve high gain and high swing. Using this two stage amplifier architecture is a big penalty in terms of speed and power dissipation. It would be desirable to use a telescopic cascade amplifier to improve the speed and save power. Furthermore, the telescopic cascode amplifier

would have less output swing than the two stage amplifier.

#### REFERENCES

- 1 P.E. Allen and D.R Holberg," CMOS Analog Circuit Design", Second Edition, Oxford University Press, 2002.
- 2 JohnA. McNeill, *Member, IEEE*, Christopher David, *StudentMember, IEEE*, Michael Coln, *Member, IEEE*, and Rosa Croughwell, *Member, IEEE*, "Split ADC" Calibration for All-Digital Correction of Time-Interleaved ADC Errors", *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS*, VOL. 56, NO. 5, MAY 2009.
- 3 Junhua Shen and Peter R. Kinget, *Senior Member, IEEE*, "A 0.5-V 8-bit 10-Ms/s Pipelined ADC in 90-nm CMOS", *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, VOL. 43, NO. 4, APRIL 2008.
- 4 Lukas Dörrer, Franz Kuttner, Patrizia Greco, Patrick Torta, and Thomas Hartig, "A 3-mW 74-dB SNR 2-MHz Continuous-Time Delta-Sigma ADC with a Tracking ADC Quantizer in 0.13- $\mu$ m CMOS", *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, VOL. 40, NO. 12, DECEMBER 2005.
- 5 Chun-Ying Chen, Michael Q. Le, *Member, IEEE*, and Kwang Young Kim, "A Low Power 6-bit Flash ADC With Reference Voltage and Common-Mode Calibration", *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, VOL. 44, NO. 4, APRIL 2009.