Design and Computation of Energy Factor Parameters for an Interleaved Boost Converter

[1]Radha Sree.K, [2]Dr.R.Seyezhai
[1]Student, Department of EEE, [2] Associate Professor, Department of EEE
SSN College of Engineering, Kalavakkam, Chennai - 603110

Abstract

Energy factor and the sub-sequential parameters best describe the characteristics of the DC-DC converter and they are mainly used in stability studies as well as controller design. In this paper, the computation of these parameters for a 3-phase interleaved boost converter (IBC) has been described in detail. Also, the design of IBC has been given importance. The values of the parameters computed have been tabulated. The simulation of the 3-phase IBC has been carried out using MATLAB/SIMULINK.

Keywords – IBC, ripple, energy factor, transfer function.

I. INTRODUCTION

In order to overcome the drawback associated with the conventional converters such as low voltage gain, some new topologies were proposed as mentioned in [1]-[4]. One such topology is the IBC, in which the input current is shared among the phases. This feature in turn results in high reliability and high efficiency. Besides characteristics such as efficiency and reliability the other system characteristics such as maintenance, repair, fault tolerance [5] etc also improved. By virtue of IBC, the voltage stresses on the switches are alleviated with subsequent reduction in the input current ripple.

IBC are employed in wide range of applications such as power factor correction circuits, fuel cell systems, photovoltaic arrays etc [6]-[8]. In this paper, the design methodology of IBC has been elucidated. The computation of the inductance and the filter capacitance of the IBC have been done. The design of IBC has been carried out with the ultimate objective of reducing the ripple in the output voltage and the input current.

The analysis of DC-DC converters was confusing because of the non-availability of the parameters to best describe the characteristics of the converters. Study of energy storage in the converters has gained a lot of attention in the recent years. To make the analysis simpler and to describe the converters characteristics, a new concept called the energy factor was introduced. With the introduction of energy factor and other sib-sequential parameters, the modeling of the converter has become simpler.

These parameters are entirely different from the conventional ones such as total harmonic distortion (THD), ripple factor etc. They give a clear picture of system stability, reference response and interference recovery. They aid in converter characteristics foreseeing and also in system design.

In this paper, energy factor and the other sub-sequential factors have been defined along with their significance. The parameters have been computed for a 3-phase IBC and the values obtained are tabulated. From, these parameters the Transfer function of the converter can be devised, which is useful for studying the response of the system.

II. INTERLEAVED BOOST CONVERTER

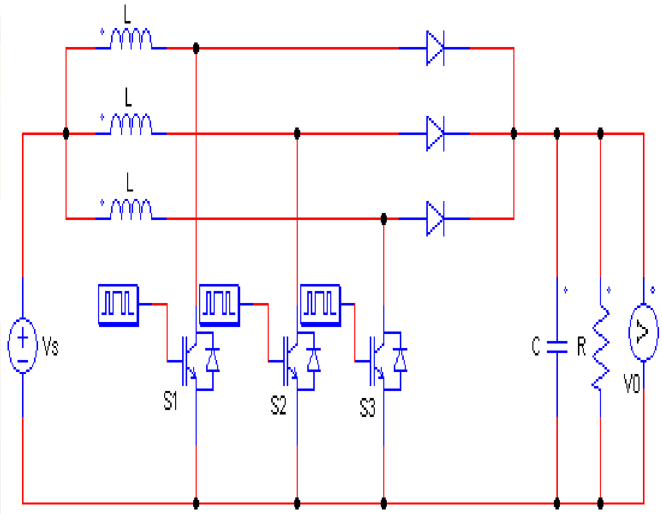

Fig.1. Circuit of IBC

The circuit of the interleaved boost converter is shown in Fig.1.The interleaved boost converter is popular as the configuration, minimizes the current ripple thereby reducing the size of the input filter. The input current also gets divided in the n-parallel paths and this leads to reduction in stresses also. Higher efficiency is also realized. Moreover, the interleaving technique facilitates the reduction in the size of the inductors employed.

The gating pattern of the IBC is shown in Fig.2. The IBC is made up of N-parallel boost converters [9]. The operation of IBC is similar to that of the conventional boost converter. The number of inductors and diodes is same as the number of phases. The switching frequency of the 3-phase IBC is identical but the gating pattern of each phase is shifted by an angle 360/N, n denotes the number of phases [10]. In case of 3-phase IBC, the angle is 120º. 3-phase IBC is mostly preferred as the current ripple can be reduced considerably. Interleaving technique reduces the Electromagnetic interference (EMI); therefore, the size of the EMI filter also gets reduced [11].

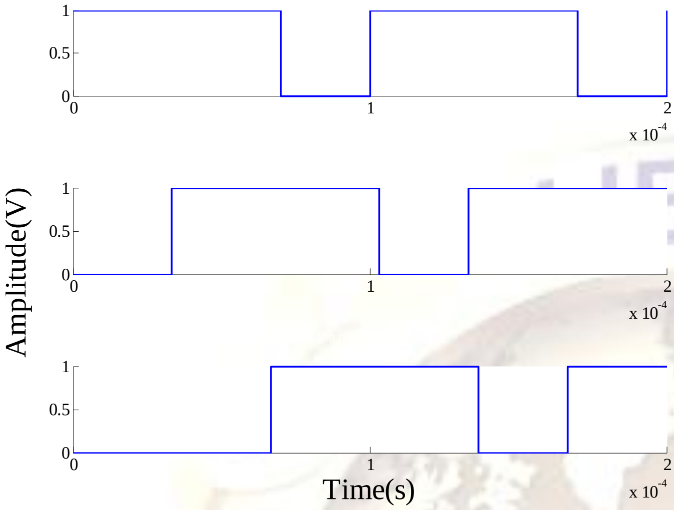

Fig.2. Gating pattern of IBC.

III. DESIGN ASPECTS

The design of IBC generally involves the selecting the number of phases, duty ratio, inductors, power switches etc [12]-[13]. This requires a good knowledge of the peak currents. The inductors and the diodes in all channels should be kept identical. Designing the components in the power path is similar to that of the single boost converter with which operates at 1/n times the power.

A. Selection of number of phases

It has been observed that the ripple in the input current decreases with increase in the number of phases. On the other hand, the cost and complexity of the circuit also increases. So, a compromise had to be made between them. In this paper, the number of phases was chosen to be three to reduce the ripple content without increasing the cost drastically.

B. Selection of duty ratio

Duty ratio also aids in ripple reduction and hence it has to be selected carefully. From the plot of the input current ripple versus the duty ratio, it can be found that for an N-phase IBC, the ripple can be zero at particular values of duty ratio [14]-[16]. For a 3-phase converter, the ideal duty ratio at which the ripple is zero is 0.7.

C. Selection of inductance and Capacitance

The value of the filter capacitor [17]-[18] to be employed can be computed using the equation (1),

$$C = \frac{V_s DF}{R\Delta V_o} \qquad (1)$$

where, V_s and V_o represent the input and the output voltage respectively, D is the duty ratio, F is the switching frequency, R is the load resistance employed and ΔV_o is the ripple in the output voltage. Similarly, the inductance can be computed using equation (2),

$$L = \frac{V_s DF}{\Delta I_l} \qquad (2)$$

Where, ΔI_l represents the ripple in the inductor current.

D. Selection of power device

IGBT was used as the power device. IGBT combines the gate-drive characteristics of MOSFET and also the high current low saturation voltage capability of bipolar transistors. Their high pulse ratings and affordability makes them very popular. The conduction losses associated with the device is less when compared to MOSFET. In general, they are used in high voltage, high current and low switching frequency applications.

IV. ENERGY FACTOR AND SUB-SEQUENTIAL PARAMETERS FOR IBC

The energy factor and the sub-sequential parameters are elucidated in detail in this section. For the computation of these parameters the instantaneous input voltage and the current and the average values are assumed to be $v_1(t)$, $i_1(t)$, V_1, I_1. Similarly the instantaneous output voltage and current and the average values are taken to be $v_2(t)$, $i_2(t)$, V_2, I_2. The various parameters are given by equations (3) to (14) [19].

A. Pumping Energy, PE

In IBC, the transfer of energy from the source to energy storage elements like inductor and capacitor takes place with the help of the pumping circuit. Pumping energy is used to count the input energy in a switching period T.

$$\begin{aligned} PE &= \int_0^T P_{in}(t)dt \qquad (3) \\ &= \int_0^T V_1 i_1(t)dt \\ &= V_1 I_1 T \end{aligned}$$

B. Stored energy, SE

The energy stored in the inductor and capacitor is given by (4) and (5) respectively as:

$$W_L = 0.5 * L\, I_L^2 \qquad (4)$$

$$W_c = 0.5 * C\, V_C^2 \qquad (5)$$

The total stored energy if there are n_L inductors and n_C capacitors is depicted in (6)

$$SE = \sum_{j=1}^{n_L} W_{L_j} + \sum_{j=1}^{n_C} W_{C_j} \quad (6)$$

C. Capacitor – inductor stored energy ratio, CIR

The DC-DC converters are composed of inductors and capacitors. Therefore, CIR can be defined as:

$$CIR = \frac{\sum_{j=1}^{n_C} W_{C_j}}{\sum_{j=1}^{n_L} W_{L_j}} \quad (7)$$

D. Stored energy variation on inductors and capacitors, VE

Considering the ripple in the inductor current, the variation of stored energy on the inductor is given by,

$$\Delta W_L = LI_L \Delta i_L \quad (8)$$

Where, Δi_L is the ripple in the inductor current. As the voltage across the capacitor has variation (ripple) Δv_C, the variation of the stored energy across the capacitor is:

$$\Delta W_C = CV_C \Delta v_C \quad (9)$$

Hence the total variation in the stored energy is:

$$VE = \sum_{j=1}^{n_L} \Delta W_{L_j} + \sum_{j=1}^{n_C} \Delta W_{C_j} \quad (10)$$

E. Energy factor, EF

Energy factor can be defined as the ratio of stored energy (SE) over pumping energy (PE). Being the most important factor of the converter, it is independent of k and is inversely proportional to the switching frequency, f.

$$EF = \frac{SE}{PE} = \frac{\sum_{j=1}^{n_L} W_{L_j} + \sum_{j=1}^{n_C} W_{C_j}}{V_1 I_1 T} \quad (11)$$

F. Variation energy factor, EF_V

Energy factor and the variation energy factors are mainly used to analyze the characteristics of the converter. The variation energy factor can be defined as the ratio of variation of stored energy over the pumping energy.

$$EF_V = \frac{VE}{PE} = \frac{\sum_{j=1}^{n_L} \Delta W_{L_j} + \sum_{j=1}^{n_C} \Delta W_{C_j}}{V_1 I_1 T} \quad (12)$$

G. Time constant, τ

The transient process of the converter can be described using the time constant. It is given as:

$$\tau = \frac{2T * EF}{1 + CIR} \left(1 + CIR * \frac{(1-\eta)}{\eta}\right) \quad (13)$$

If there is no power loss in the converter, the efficiency, ŋ can be taken as one.

H. Damping time constant, τ_d

The damping time constant also describes the transient process of the DC-DC converter. The oscillation response for unit step or impulse interference can be estimated using this parameter. It is given as:

$$\tau_d = \frac{2T * EF}{1 + CIR} * \frac{CIR}{\eta + CIR(1-\eta)} \quad (14)$$

Ŋ=1 if there are no power losses in the converter.

I. Time constant ratio, ξ

Also, used to analyze the transient process of the converter and is given as:

$$\xi = \frac{\tau_d}{\tau} = \frac{CIR}{\eta\left(1 + CIR \frac{1-\eta}{\eta}\right)^2} \quad (15)$$

CIR>1 and hence, when the power loss is higher, the time constant ratio gets smaller.

V. SIMULATION RESULTS

The simulation of the three phase interleaved boost converter was carried out using MATLAB/SIMULINK. The parameters of the circuit are shown in table I.

TABLE-I
Parameters of the Interleaved boost converter

Parameters	Values
Inductance, L	1mH
Capacitance, C	1000uF
Load Resistance, R	5 Ohms
Switching Frequency, f	10kHz
Duty Ratio, k	0.7
Input Voltage, V_s	30V
Output Voltage, V_o	99.13V
Voltage transfer gain, M	3.33
Inductor current, I_L	21.11A
Input Current, I_1	66.35A
Load Current, I_2	19.83A

The output voltage of the three phase IBC is shown in Fig.3. Voltage of magnitude 99.18V was obtained with k=0.7. The ripple in the output voltage was 0.111%

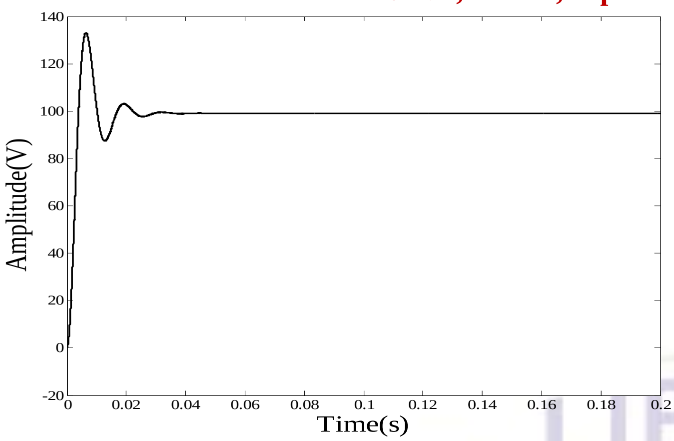

Fig.3. Output voltage of IBC

The ripple in the input current has been analyzed for k>0.5 and k<0.5. The ripple in the input current for k<0.5 is shown in Fig.4. The input current ripple for duty cycle of 0.4 was computed to be 0.9472%.

In order to minimize the ripple in the input current, k was chosen to be 0.7 for the three phase IBC. The percentage of ripple was computed to be 0.2714. The input current ripple for k>0.5 is shown in Fig.5.

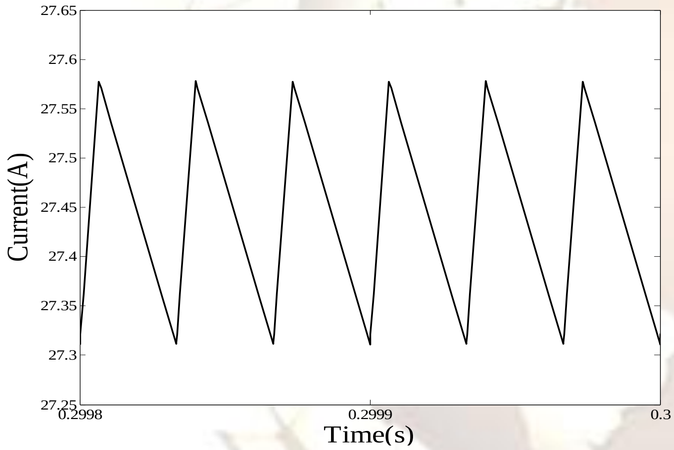

Fig.4. Ripple in the input current for k<0.5

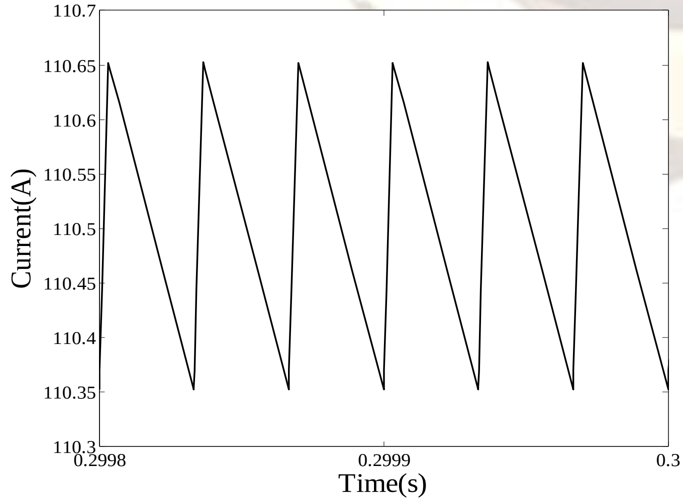

Fig.5. Input current ripple for k>0.5

The energy factor and the sub-sequential parameters were computed for the proposed three phase IBC and the values obtained are shown in Table – II

TABLE-II
Energy factor and sub-sequential parameters

Parameters	Values
Pumping Energy, PE	0.19905J
Stored energy in the inductor	668.4mJ
Stored energy in the capacitor	5J
Total stored energy, SE	5.6684J
Capacitor-Inductor stored energy ratio, CIR	7.481
Time constant	733.6us
Damping time constant	4.65ms
Time constant ratio	6.3386
Variation in stored energy in the inductor	0.1203J
Variation in stored energy in the capacitor	`0.0110J
Total variation in stored energy, VE	0.37191J
Energy factor, EF	28.477
Variation energy factor, EF_V	1.868

VI. CONCLUSION

In this paper, a 3-phase interleaved boost converter was designed with the aim of reducing the input current ripple. The results obtained revealed that the current ripple was almost zero when IBC was operated with a duty ratio of 0.7. The energy parameters were also computed for the 3-phase IBC. The transfer function of the converter can be obtained using the computed values and further the response of the converter for a step input can also be studied.

REFERENCES

[1] Yungtaek Jang and Milan M. Jovanovic, "A New Two-Inductor Boost Converter with Auxiliary Transformer", *IEEE Transactions on Power Electronics*, vol.19, no.1, pp. 169-175, January 2004.

[2] P. J. Wolfs, "A Current Sourced DC-DC Converter derived via the Duality Principle from the Half-bridge Converter", *IEEE Transactions Industrial Electronics*, vol. 40, no. 1, pp. 139-144, February 1993.

[3] Roger Gules, L. Lopes Pfitscher and L. Claudio Franco, "An Interleaved DC-DC Boost Converter with Large Conversion Ratio", *IEEE International Symposium on Power Electronics*, 2003, ISIE'03, vol. 1, pp.411-416, June 2003.

[4] K. C. Tseng, T. J. Liang, "Novel high Efficiency Step-up Converter", *IEEE Proc.*

Electr. Power Appl., vol. 151, no. 2, pp. 182-190, March 2004.

[5] S. Kamtip, K. Bhumkittipich, "Design and Analysis of Interleaved Boost Converter for Renewable Energy Applications", 9th *Eco-Energy and Material Science Engineering Symposium*, May 2011.

[6] A. Newton, T.C. Green and D. Andrew, "AC/DC Power Factor Correction using Interleaving Boost and Cuk Converters", *IEEE Power Electr. And Variable Speed Drives Conf*, pp. 293-298, 2000.

[7] M. Veerachary, T. Senjyu and K. Uezato, "Maximum Power Point Tracking of Coupled Inductor Interleaved Boost converter Supplied PV System", *IEEE Pro. Electr Power Appl.*, vol. 150, no.1, pp. 71-80, 2003.

[8] B. A. Miwa, D. M. Otten and M. F. Schlecht, "High Efficiency Power Factor Correction using Interleaving Techniques", *IEEE Proc. APEC'92*, Boston, USA, vol. 1, pp. 567-578, 1992.

[9] M. T. Zhang, M. M. Jovanovic nad F. C. Lee, "Analysis and Evaluation of Interleaving Techniques in Forward Converters", *IEEE Transactions on Power Electronics*, vol. 13, no. 4, pp. 690-698, July 1998.

[10] Gyu-Yeong Choe, Hyun Soo Kang, Byoung-Kuk Lee, "Design Considerations of Interleaved Converters for Fuel-cell Applications", *Proc. of international Conference on Electrical Machines and Systems*, pp.238-243, 2007.

[11] Chris Bridge and Laszlo Balogh, "Understanding Interleaved Boundary Condition Mode PFC Converters", *Fairchild Semiconductor Power Seminar*, pp. 1- 14, 2008-2009.

[12] H.Xu, E.Qiao, X.Guo, X.Wen and L.Kong , "Analysis and Design of High Power Interleaved Boost Converters for Fuel Cell Distributed Generation System", *Int. Conf. IEEE Power Electronics Specialists Conference (PESC)*, pp. 140 – 145, 2005

[13] H.Kosai, S.McNeal, Austin Page, Brett Jordan, Jim Scofield and B.Ray, "Characterizing the effects of inductor coupling on the performance of an interleaved boost converter", *Proc. CARTS USA*, pp. 237–251, 2009.

[14] R.J.Wai and R.Y.Duan, "High step-up converter with coupled-inductor", *IEEE Transactions on Power Electronics*, Vol. 20, No.5, pp. 1025-1035, 2005.

[15] Laszlo Huber, T.Brian Irving and M.Milan Jovanović, "Closed-Loop Control Methods for Interleaved DCM/CCM Boundary Boost PFC Converters", *Int. Conf. IEEE Applied Power Electronics, Washington*, pp. 991-997, 2009.

[16] R. Seyezhai, "Design Considerations of interleaved Boost Converter for Fuel-cell Systems", *International Journal of Advanced Engineering Sciences and Technologies*, vol. 7, no. 2, pp. 323-329, 2011.

[17] P.Thounthong, P.Sethakul, S.Rael and B.Davat , "Design and implementation of 2-phase interleaved boost converter for fuel cell power source", *Int. Conf. Power Electronics, Machines, and Drives ,PEM* , pp. 91–95, 2008.

[18] M.Veerachary, T.Senjyu and K.Uezato, "Modeling and analysis of interleaved dual boost converter", *IEEE International Symposium on Industrial Electronics*, Vol. 2, pp 718 – 722, 2001.

[19] Fang Lin Luo, Hong Ye, Muhammad Rashid, "Digital Power Electronics and Applications", pp. 34-43.