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A Novel Approach to Design of 6T (8 X 8) SRAM Cell Low Power Dissipation Using MCML Technique on 45 Nm

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ABSTRACT

The most research on the power consumption of 6T SRAM has been focused on the static power dissipation and the power dissipated by the leakage current. On the other hand, as the current VLSI technology scaled down, the sub-threshold current increases which further increases the power consumption. In this paper we have proposed 6T (8 X 8) SRAM cells using MCML technology which will reduce the leakage power in SRAM cell and will control the sub-threshold current. The results of 6T (8 X 8) SRAM cell array using MCML technology in 45 nm library on Cadence Virtuoso Tool, represents that there is a significant reduction in power dissipation and leakage current using MCML technology.

Keywords: Cadence virtuoso tool, Low power dissipation, Leakage current, MOS current mode logic, SRAM cell

I. INTRODUCTION

As the technology scales down, the increase in leakage current is an important factor of CMOS device. As the number of transistors increases, the leakage power increases. Significant thought has been rewarded to the design of minimum power and high-performance SRAM as they are significant components in together handheld devices and high performance processors [1].

Dynamic power has been a main source of power dissipation. The static power dissipation is flattering a large part of the total power dissipation. In any design the static power is power dissipated which the switch is form on to off and vice versa. The static power dissipation is the product of supply power voltage and leakage current [3] [4].

The objective of this paper is to design a low power 6T (8 X 8) SRAM cell array using MCML technology. Simulation results shows that the proposed design power savings measured up to the conventional SRAM cell array based on the 6 transistors configuration. In this paper we have designed 6T (8 X 8) SRAM with and without using MCML technique. Fig. 1 shows that design of 6T SRAM without MCML technology. A basic 6T SRAM cell has been 6 transistors (two p-type transistor and four n-type transistor).Transistors M1, M2, M3 and M4 implemented as a pair of cross-coupled CMOS inverters that apply positive feedback to store significance. Transistors M5 and M6 are two pass transistors that allow access to that storage nodes for reading and writing. To write information into SRAM cell, the new value of the information and its complement are driven on the bit lines, and then word line is increasing. The new value will overwrite old value, since the bit lines are actively driven by write circuitry [5]. To read a value from and SRAM cell, the bit lines are precharged high and then word line is increased turning on the pass transistors. Since one of the internal storage nodes is low down, one of the bit lines starts discharging. A sense amplifier which is connected to the bit lines sense which of the bit lines is discharging and reads the stored value. The sizing of the transistors in SRAM cell should be done carefully for proper operation of SRAM [6].

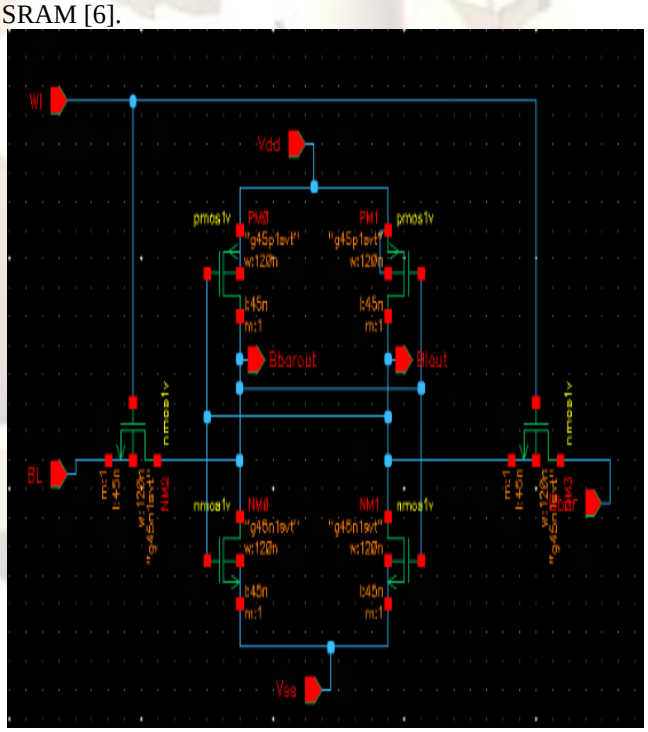

Figure 1: 6T SRAM cell

The leakage currents in SRAM vary within a clock cycle depending on the time of the operation being performed, since many types of the transistors would be in off state during dissimilar operations. The SRAM cells have tendencies to be unstable and the very less power supply operation becomes hard to get.

II. SIMULATION OF 6T SRAM USING MCML

2.1 SRAM CELL

The 6T SRAM with MCML circuit designed with the help of 9 transistors (4 PMOS, 5 NMOS transistors) is shown in figure 2. MCML gates behaving like differential and steer current between the two criticize resistances. Fig. 2 shows that PMOS transistor (M1, M2) works as resistors when supply voltage is zero. The NMOS transistor (M9) behaves like a current supply. The current source is an NMOS transistor with fixed ref2 (gate) working in saturation state. The load resistor behaves like PMOS devices with fixed gate voltage (ref1) and is created to be operator in the linear region in order to model resistors.

The goal of NMOS differential pair is to switch the current provided by the current source from one side to the other. The current source for MCML circuits is designed with a single NMOS transistor.

Table 1: Design parameter of 6T SRAM cell using MCML

Device	No. of transistors	Threshold voltage	Length/Width
PMOS	4	400 mV	45 nm/120 nm
NMOS	5	400 mV	45 nm/120 nm
Input pins	7 pins	Name: V_{DD}, V_{SS}, ref1,ref2 B, Bbar, WL	

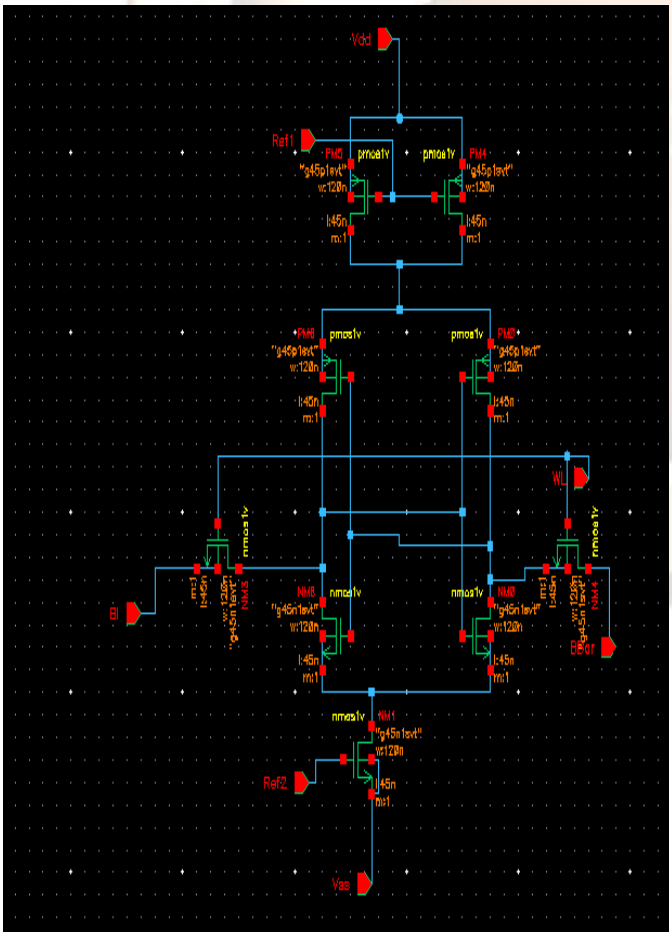

Figure 2: SRAM cell using MCML

2.2 SENSE AMPLIFIER

The sense amplifiers have to increase the input signal (data) which is present on the bit lines (bit line and bit bar line) during the read action. The memory cells are weak according their small size, and hence cannot the discharge the bit lines quick as much. Also, the bit lines carry on slew turn over a large difference of voltage is formed between bit line and bit bar line. This causes large power dissipation since the bit lines have large capacitances. Thus the limiting the word line pulse width, we can organized the amount of charge pulled down by the bit lines and hence limit power dissipation. It consists of two cross paired gain stages which are allowed by the sense clock signal, sense clock signal is enabled. The cross paired stage make curtains a full strengthening of the input signal. This type of amplifier uses less amount of power, however they can possibility be slower as some timing margin is required for the generation of the sense clock signal. If the sense amplifiers enabled before sufficient difference of the voltage is formed, it could direct to a wrong output. Accordingly, the timing of the sense clock signal needs to be such that the sense amplifier can activate over various process corners and temperature ranges.

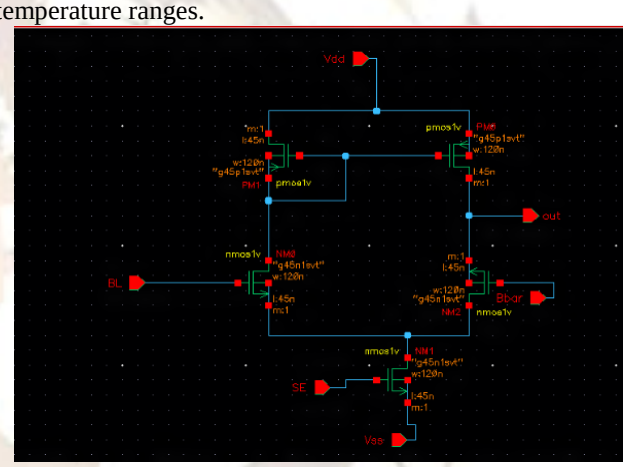

Figure 3: Sense Amplifier

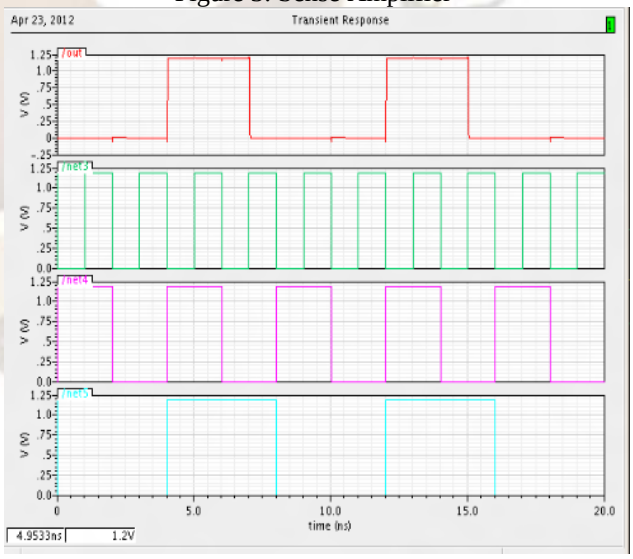

Figure 4: Transient response of Sense Amplifier

2.3 ROW/ COLUMN DECODER

3 to 8 decoder is made using 3 inputs AND GATE. Row decoder selects the word lines and column decoder selects the bit lines. Both decoders select the SRAM cell. A cell is accessed for reading or writing by choosing its row and

column. Every cell can store 0 or 1. The row and column (or group of columns) decoder will select the particular cell of SRAM cell array. Fig. 5 represents the schematic of 3 to 8 decoder.

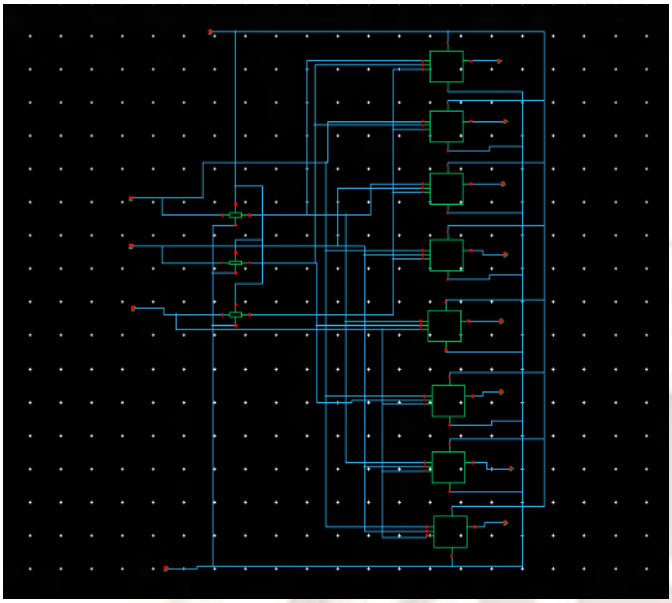

Figure 5: 3 to 8 decoder

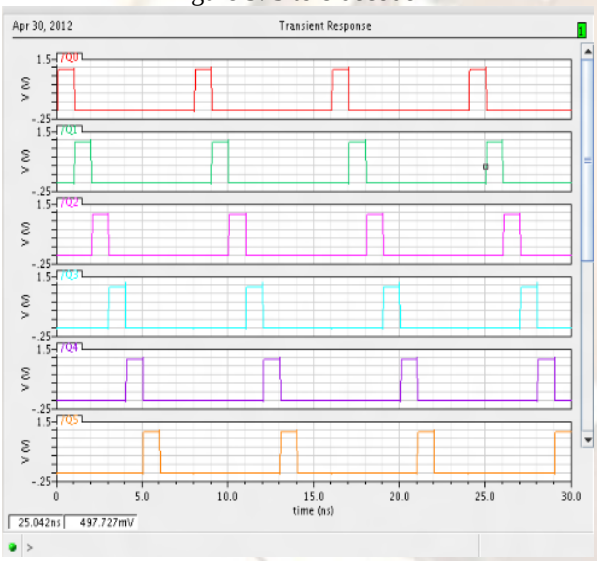

Figure 6: Transient response of 3 to 8 decoder

III SIMULATION OF (8 X 8) 6T SRAM CELL ARRAY

Fig. 7 shows (8 X 8) SRAM cell array. This is made by using 3 to 8 decoder, precharge circuit, sense amplifier, multiplexer and SRAM cell. 3 to 8 decoder is used to select the row (Word lines) of SRAM cell and column decoder is used to select the column of SRAM cell array which are connected the bit lines. Precharge circuit is used to store the previous value. It stores the voltage $V_{DD}/2$. Precharge circuit connects with the bit line and bit bar line. When precharge signal is high, it will reset the old value. SRAM cell is designed by using two cross coupled inverters. Inverter using by PMOS and NMOS transistors. SRAM cell has two pass transistors which are used to select the bit lines. RAM cell is used to store the one bit. When row and column decoder selects the one SRAM cell then precharge circuit gives the difference voltage of bit lines, it store the one bit in SRAM cell. Sense amplifier uses for amplify the voltage. Sense amplifier is connected the bit lines. Bit line will as act one input of sense amplifier and bit bar lines will act as another input of sense amplifier. Sense amplifier gives the difference of both inputs which is connected to the bit lines. When sense enable signal is high, sense amplifier will work otherwise its store previous values. Output of sense amplifier is the output signal of SRAM cell. Fig. 8 represents the transient response of (8 X 8) SRAM cell array.

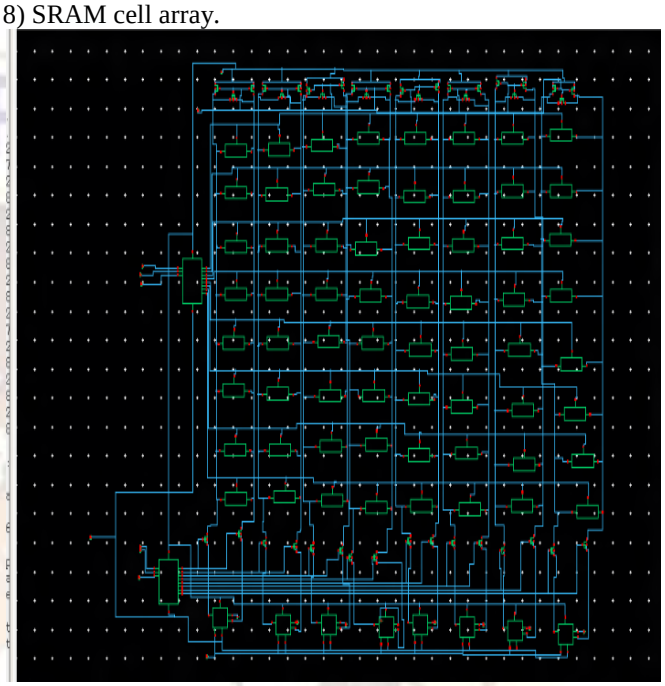

Figure 8: (8 X 8) SRAM cell array

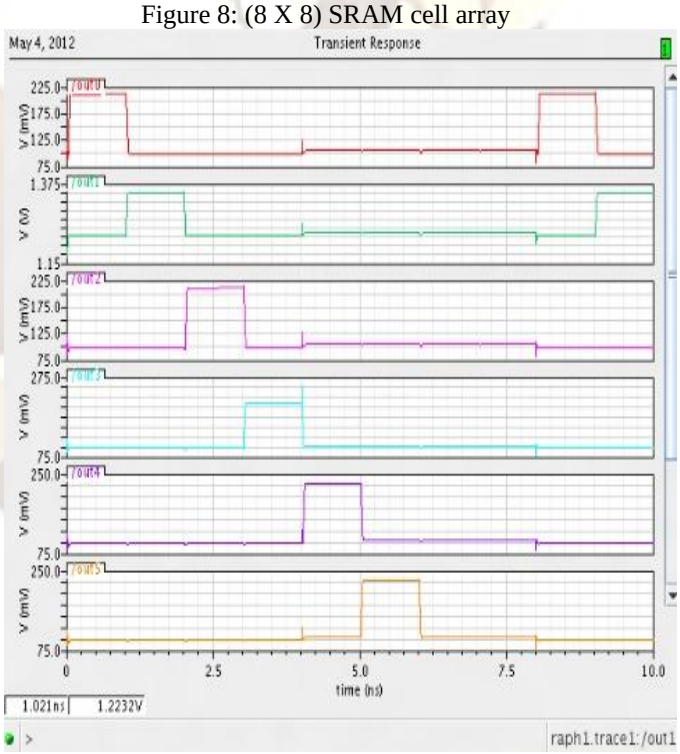

Figure 8: Transient response of 8 X 8 SRAM cell array

3.1 (8 X 8) SRAM ARRAY USING MCML

Fig. 9 shows (8 X 8) SRAM cell array using MCML. This is made by using 3 to 8 decoder, precharge circuit, sense

amplifier, multiplexer and SRAM cell using MCML. MCML circuit is connected the SRAM cell. In MCML, two PMOS transistors are connected between V_{DD} and the PMOS transistor of inverter which works as a thin resistor, One NMOS transistor is connected between ground and NMOS transistor of inverter which works as current source. When row and column decoder selects the one SRAM cell and precharge circuit gives the difference voltage of bit lines, it store the one bit in SRAM cell**.** Output of Sense amplifier is the output signal of SRAM cell which store the SRAM cell using MCML technology.

MCML technology gives the low power because PMOS transistor of MCML technology increases the subthreshold voltage which further decreases the threshold voltage and decreases the leakage current. So leakage power is reduce. Fig. 10 represents the transient response of (8 X 8) SRAM cell array using MCML technology.

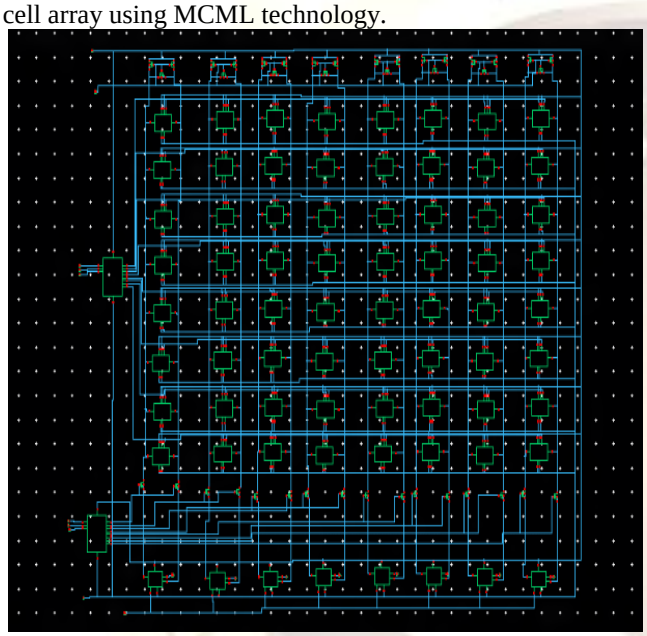

Figure 9: (8 X 8) SRAM cell array using MCML technology

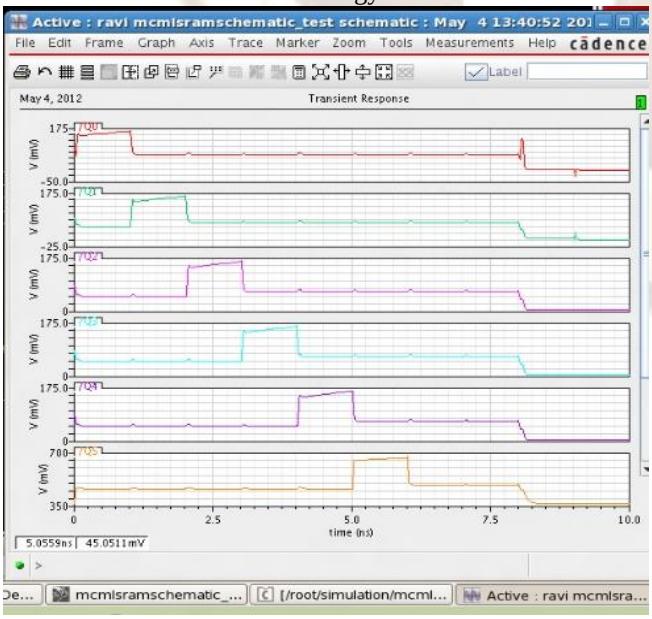

Figure 10: Transient response of (8 X 8) SRAM cell array

IV. SIMULATION RESULTS:

4.1 POWER DISSIPATION

Table 2 compares the power dissipation of (8 X 8) SRAM cell array and (8 X 8) SRAM cell array with MOS Current Mode Logic (MCML) on 45 nm. At a supply voltage of 1.2 V (8 X 8) SRAM cell array gives 480.3 µW of power dissipation which further reduces to 128.6 µW using MCML technology. Results show that as the supply voltage decrease the power dissipation also decreases. At 1.1 V the power dissipation is 239.56 µW which further reduces to 16.1 µW as we decrease the supply voltage from 1.1 to 0.7 V. For MCML it further to 6.78 µW at 0.7 V. So from the results it is concluded that there is a significant reduction in the power dissipation using MCML technology.

Table 2: Power dissipation and vs. supply voltage

Supply Voltage (Volts)	Power dissipation of (8 X 8) SRAM cell array	Power dissipation (8 X 8) SRAM cell array using MCML
1.2 V	480.3 µW	128.6 µW
1.1 V	239.56 µW	78.91 µW
1.0 V	120.22 µW	46.44 µW
0.9 V	62.85 µW	25.37 µW
0.8 V	31.4 µW	12.2 µW
0.7 V	16.1 µW	6.78 µW

4.2 LEAKAGE CURRENT

Table 3: Leakage current and technology

Technology	Leakage current(µA)
8 X 8 SRAM cell array	49.28
8 X 8 SRAM cell array using MCML	41.95

Table 3 represents the leakage current of (8 X 8) SRAM cell array. We can see that there is a good reduction in leakage current using MCML technology. For (8 X 8) SRAM cell array the measured leakage current is 49.28 µA which further reduces to 41.95 µA .using MCML technologies. These values are measured for supply voltage of 1.2 V.

4.3 STATIC POWER DISSIPATION

Table 3: Technology and static power dissipation

Technology	Static power dissipation(µW)
8 X 8 SRAM cell array	59.11
8 X 8 SRAM cell array using MCML	49.95

The table 3 represents the static power dissipation for (8 X 8) SRAM cell array. Using MCML technology the static power dissipation reduces to 49.95 µW from 59.11 µW.

4.4 POWER –DELAY AND ENERGY DELAY PRODUCT

Power –delay and energy delay product are represented in table 4. The minimum power delay product is 9.83 e^{-12} using MCML technology which is 34.05e^{-12} without using

MCML. The energy delay product for MCML is 78. $68e^{-12}$ which was $9.83e^{-12}$ without MCML technology.

Table 4: Technology, Power –delay and energy -delay product

Technology	Power –Delay product	Energy –Delay product
8 X 8 SRAM cell array	34.05E-12	272.04E-12
8 X 8 SRAM cell array using MCML	9.83E-12	78.68E-12

V CONCLUSION

After simulation it is observed that the MCML technology is the best technology because it reduces the power dissipation. It has concluded that (8 X 8) SRAM cell array using MCML gives the lower power dissipation of 128.6 µW; leakage current of 41.95 µA at power supply is 1.2 V. this technology also reduces the static power dissipation i.e. 49.65 µW using MCML technology. It also gives the lower power delay product of $9.8e^{-12}$ and energy delay product of $78.68e^{-12}$.

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