Performing Reliability Simulation For SRAM Circuit Using SPICE

Radha Madhuri.Rajulapati*, Naseema.Sheik**
** (Department of Electronics and Communication Engineering, K.L.University, Vijayawada,A.P)
** (Department of Electronics and Communication Engineering, K.L.University, Vijayawada,A.P)

ABSTRACT

Based on some new accelerated lifetime models and failure equivalent circuit modeling techniques for the common semiconductor wear out mechanisms, simulation program with integrated circuit emphasis (SPICE) can be used to characterize CMOS VLSI circuit failure behaviors and perform reliability simulation. This paper used a simple SRAM circuit as an example to demonstrate how to apply SPICE to circuit reliability modeling, simulation, analysis, and design. The SRAM circuit, implemented with a commercial 0.25-μm technology, consists of functional blocks of 1-bit six-transistor cell, precharge, read/write control, and sense amplifier. The SRAM operation sequence of "write 0, read 0, write 1, read 1" was first simulated in SPICE to obtain the terminal voltage and current stress profiles of each transistor.

Keywords –sram, read operation, write operation, simulations.

I. INTRODUCTION

Starting from the design specification to the generation of mask layout, layout design of an integrated circuit has several processing steps which have to be carefully exercised. These steps include design of transistor level schematic, SPICE simulation of the circuit according to the designed W/L ratios of the individual transistors, drawing of the layout using a layout editor, design rule check, parasitic extraction and final simulation and verification. These all processing methods are inevitable for the error free operation of chip and similar methodology is followed for the design of 1 K-Byte SRAM IC. Basic building block of the SRAM is SRAM cell which stores one bit data. Using common bit lines data can be read and written to the SRAM cell. SPICE, being an industry standard tool for circuit simulation and analysis, is used for the simulation and analysis of SRAM cell and subsequently for the whole design. Precharge circuit, sense amplifier and read-write circuits completes the one SRAM memory. The memory is arranged in row-column matrix which facilitates easy addressing of memory bits and also provides design flexibility. Once the functionality of one memory cell array is proved it can be duplicated several times with minor design change in the I/O control circuitry.

II. PLAN OF THE CHIP

Block diagram of the complete chip is shown in Figure(1.1).Six transistor SRAM cells are organized into 8 blocks. The capacity of the SRAM cell is 1 Kbyte. To address all these locations total 10 address lines from A0 to A9 are used. Out of these, A0 to A2 are used as column address decoding lines while A3 to A9 are used for decoding the rows. Each row consists total 8 memory cells and constitute to form one byte. Thus address lines address each byte not the each bit.

Each block is comprised of 128 rows and 8 columns. Thus the total number of transistors required for memory cells are 6 transistors x 128 rows x 8 columns x 8 blocks = 49,152. Rows of the each block are decoded using NOR based 7 x128 decoder. Total 1024 transistors are required for this circuit. Row decoder outputs are connected to the each row of the each block. Similarly each block is selected by the 3 x 8 column decoder. This requires total 32 transistors.

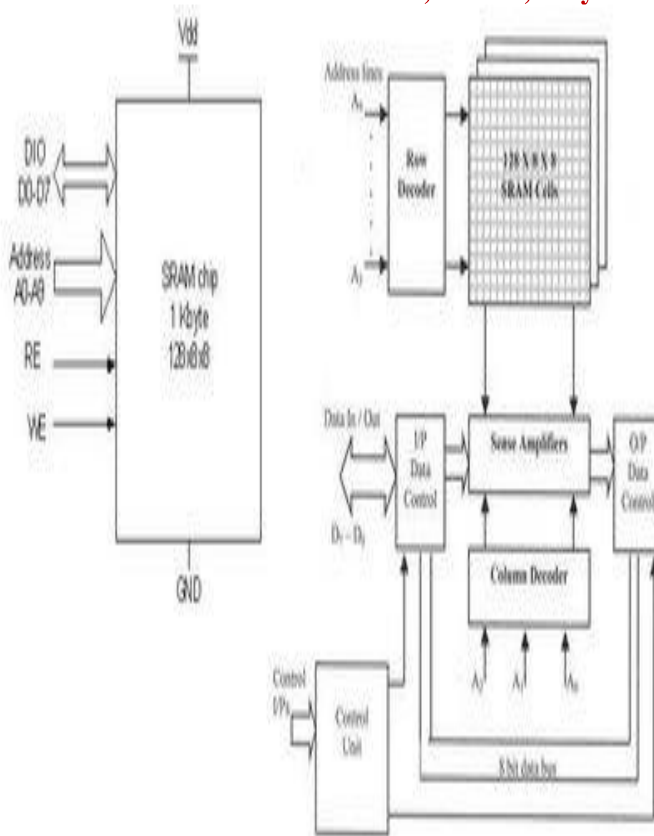


Figure (1.1) SRAM block diagram [4]

Sense amplifier is used to sense the data present in the memory cell. Input and output data control block consists of read and write circuitry and related driver circuits. 8 bits of the data D0 to D7 is read or written parelell. Read enable (RE) and write enable (WE) are the two control lines available for the chip. As the name indicate, before data read operation is performed RE is activated for read operations. Similarly for write operations WE signal has to be enabled.

Table(1.1) transistors required for different blocks.

Table (1.1) summarises the total number of transistors required for each individual block of the SRAM memory. 1.8V is assumed for the chip power supply internally as well as externally.

III. SRAM CELL: SCHEMATIC AND WORKING

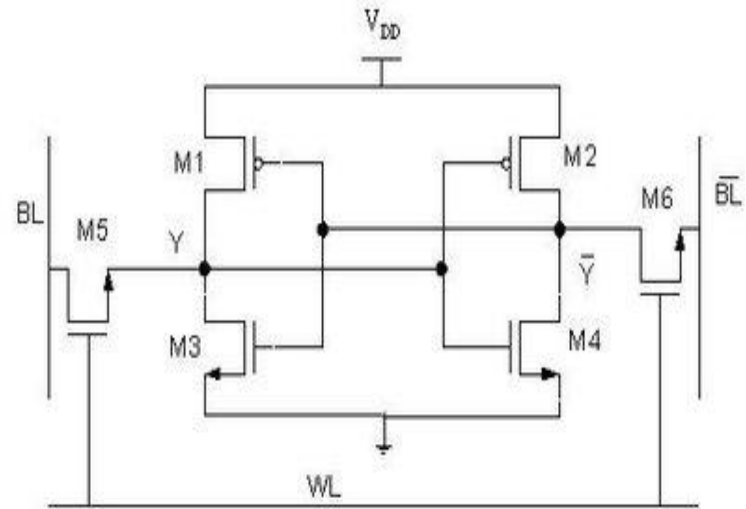


Figure (1.2) Schematic of SRAM cell

Single bit SRAM memory cell is shown in Figure (1.2). Static latches are used in the SRAM cell. SRAM cell is made up of flip flop comprising of two cross coupled inverters. Two access transistors are used to access the stored data in the cell. These transistors are turned ON/OFF by the control line called word line(WL). Generally this word line is connected to the output of row decoder circuits. When $WL=V_{DD}$ the SRAM cell is connected to bit line(BL) and complement of bit line (BLbar) allowing both read and write operations. Read-write operation is carried out by the help of access transistors.

Read operation:

Consider node Y as reference node of the SRAM cell. Cell is said to be storing 1 if node Y is high at V_{DD} and node Y-bar is at 0V. For the reverse voltage conditions cell is said to be storing zero. Let us assume that cell is storing 1.Before the read operation starts BL and BLbar lines are pre-charged to $V_{DD}/2$. When the WL is activated the current flows through M5 and M6. Now current from V_{DD} will flow through M1 and M5 charging the bit line capacitance, say C_{BL}. The existing capacitance on the line BLbar, say C_{BLbar} discharges through the transistors M6 and M4. This process develops a voltage difference between node Y and node Ybar which is sensed by the sense amplifier to detect it as 1. Similarly a 0 in the cell is also detected by the sense amplifier.

Write operation:

Let us consider the write operation of zero to the cell which is storing a value of 1. For this, sense amplifiers and precharge circuits are disabled. The cell is selected by activating the corresponding WL signal. To write zero to the cell, BL line held low and BLbar line is raised to V_{DD} by the write circuit. Thus the node Ybar is pulled up towards the $V_{DD}/2$ while node Y is pulled down to $V_{DD}/2$. When the voltage crosses this level on two nodes feedback action starts. Parasitic capacitances developed by M3, M5 and M4, M6 are charged and discharged respectively. Ultimately node Y stabilises at the value 1. Since these parasitic capacitances offered by transistors are comparatively much lesser than the bit line capacitances, write operation is faster than read operation.

Transistor sizing:

The W/L ratio of the transistor is selected to provide the gate with current driving capability in both the directions equal to that of the basic inverter. From the basic inverter design $(W/L)_n$ is usually 1.5 to 2 and for a matched design, $(W/L)_p=(\mu_n/\mu_p)(W/L)_n$. The SRAM cell must be designed such a way that, during read operation, the changes in Y and Ybar are small enough to prevent the cell from changing its state. Generally two back to back coupled inverters of the SRAM cell is designed so that Kn and Kp are matched. This design places the inverter threshold at $V_{DD}/2$. The size of the access transistors are usually made 2 to 3 times wider than Kn of the inverters.

To achieve optimum operation of the cell following (W/L) ratio is choosed for different transistors. A minimum ratio of 2 is required for NMOS transistors of inverters and 4 is necessary for PMOS transistors. Access transistors must be made double wider or more by providing a W/L ratio of more than 4. But these set of ratios does not match with the design rule of Cadence Virtuoso layout editor for 0.18 micron technology. For 0.18 μ technology minimum width for an NMOS transistor comes out to be 0.6 μ. Thus (W/L) ratio is 3.33. For PMOS transistor the ratio becomes 6.66. This implies a width of 1.2 μ. Based on the SPICE simulation results and its analysis, W/L ratio for access transistor is kept at 9.99. This refers to a gate width of 1.8 μ.

IV. SIMULATION

Mainly two types of simulation analysis is reported here. The first one focusses on normal operation of SRAM cell with approapriate W/L ratio. The second simulation studies the affect of variation of W/L ratio of access transistor on the working of SRAM cell.

Simulation 1:

Figure (1.3) shows the SPICE simulation waveform of the SRAM cell. For 0.18 μ technology, the gate width choosed for NMOS transistors are 0.6 μ; for PMOS it is 1.2 V and for access transistors gate width is 1.8 μ. When WL is disabled(i.e. low) SRAM cell is disconnected from the BL and BLbar lines. Hence voltage at node Y and Ybar is complement to each other and remains in a stable state. The stable state value is dependant on the previous value present at BL and BLbar lines.

BL signal is forced with pulse waveform of period 8ns and pulse width of 4ns. Upon activation of WL signal SRAM cell gets connected with BL and BLbar signal.

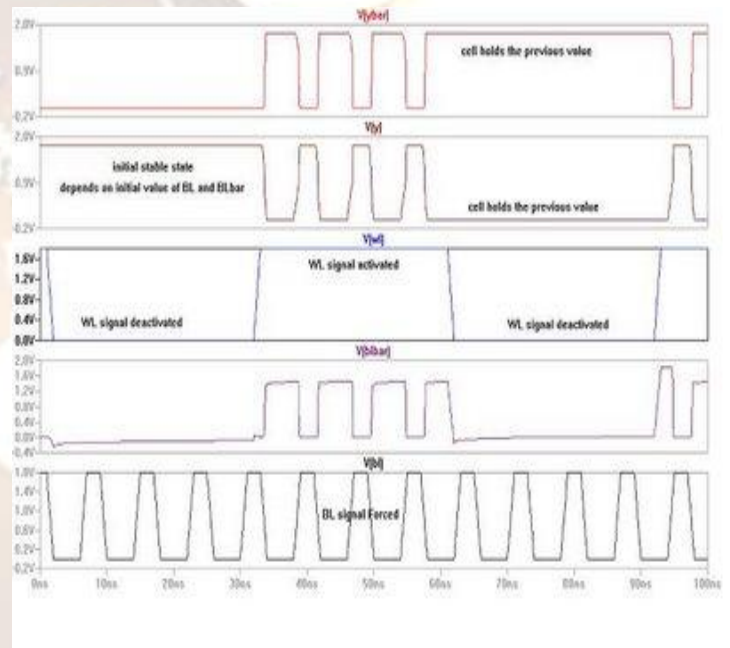


Figure (1.3) SRAM cell SPICE simulation waveform 1

Now the expected waveform at the BLbar is the inverted signal of BL. The same result can be seen in simulation waveform 1. Voltage at node Y follow the pulse voltage of BL; and node Ybar and BLbar are same and complement to pulse signal at BL.Removal of WL again disconnects the SRAM cell from the BL and BLbar line. SRAM cell holds the value whatever it had while removing the WL signal.

Simulation 2:
If W/L ratio of access transistors is reduced to the ratio of PMOS transistors then the cell fails to operate as expected due to the inefficient current driving capability of access transistor. Related waveform is shown in Figure (1.4). Here for access transistors W/L ratio is set same as that of PMOS transistor i.e. 6.66 which implies a gate width of 1.2 µ. Observe the waveform shape at area marked by circles. The waveform at BLbar should be complement to waveform at BL. But it is remaining at high state.

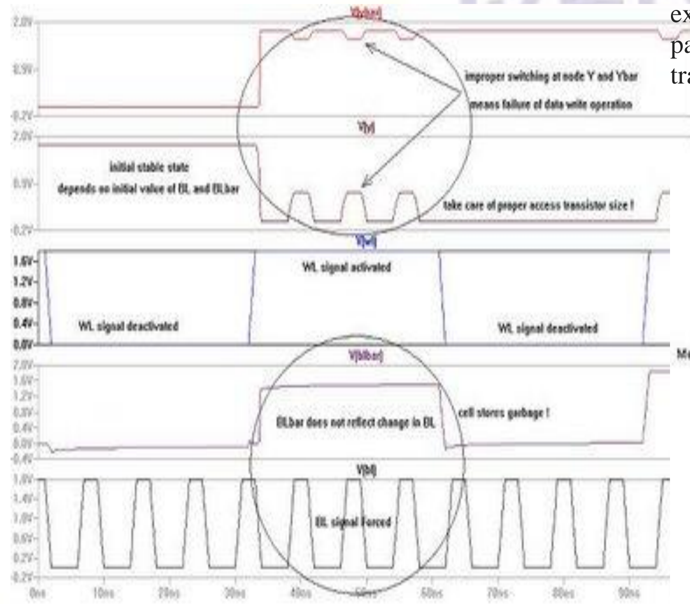


Figure (1.4) SRAM cell SPICE simulation waveform 2

This is due to the poor switching of access transistor. Similar waveforms can be observed at node Y and Ybar. (Outputs of cross coupled inverters).

1.5 Layout of the SRAM cell

Layout is a physical representation of a schematic. A set of geometric constraints or rules for a particular manufacturing process has to be followed for the physical mask layout generation. Geometries are determined by the electrical properties of the devices and design rules pertaining to the associated manufacturing process.

The mask layout design of CMOS logic gate or cell starts with the functionality and performance specification of the cell to be designed and ends in the layout. The specifications include circuit topology and initial size of the transistor. The designed transistor level schematic is simulated by the help of SPICE simulation tools. If simulation does not satisfy the required specification architecture and schematic design is revised. Optimum ordering of the transistors is determined by the Euler path method. Stick diagram representation is drawn which shows the location of the transistors, local intersections between transistors and location of the contacts. Mask layers are formed using a layout editor tool. After several iterations of editing and design rule check (DRC) and layout versus schematic (LVS) check the layout is subjected to extraction procedure. Extraction procedure extracts parasitic capacitance values and actual sizes of the transistors.

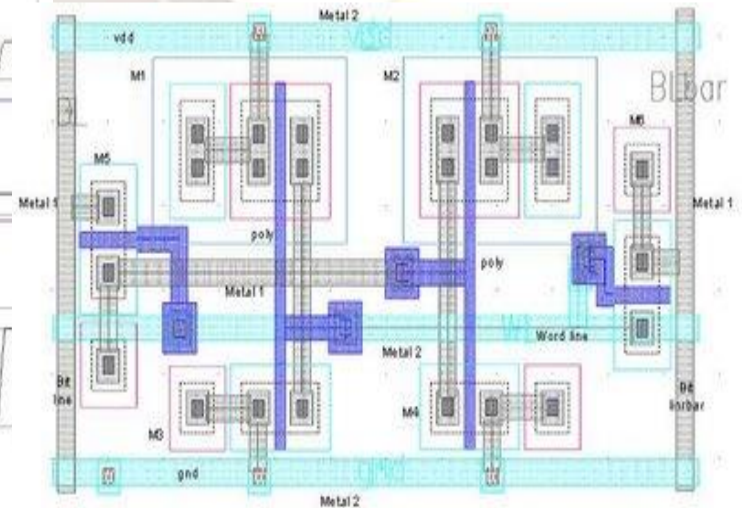


Figure (1.5) SRAM cell layout

(This is not a optimized layout...or rather not even followed basic rules !!! It just demonstrates how to draw a layout!!)

SPICE file is automatically generated consisting of all these parasitic capacitance values and other device parameters. This net list is simulated using a SPICE simulator and verified for the designed specification. If this doesn't match the whole process is repeated from the scratch.

Design rules include geometric constraints and line width constraints. The later defines constraints like metal and poly-silicon interconnection, diffusion area, minimum feature dimensions and allowable separations between two different features. Mainly there are two ways of design rules. They are known as micron rules and lambda rules. In micron rule all layout constraints are defined in micrometers

while in lambda rule it is defined in terms of a single parameter lambda (λ). For the present assignment micron rules are used.

Design specifications of the SRAM cell and its corresponding SPICE simulation results have been studied in the previous sections. For the SRAM cell layout shown in the Figure (1.5) first we need to design the individual transistors according to the design rules. PMOS transistors are placed in an n-well region whereas NMOS transistors are placed directly above the substrate. Transistors M1 to M6 are placed. Polysilicon gate of both NMOS and PMOS transistors of cross coupled inverters (i.e. latch) are aligned so that polysilicon length is minimized to reduce parasitic resistance and capacitance. Metal 1 and metal 2 layer is used for the interconnections between transistors. Metal 1 is used for direct interconnections and wherever the connections crisscross metal 2 layer is used. Bit line (BL) and bit linebar(BLbar) are vertically drawn with metal 1 layer while word line(WL), vdd and gnd are drawn horizontally with metal 2 layer. This layout method helps to extend SRAM memory by adding more SRAM cells.

From the layout Figure (1.5) it can be noted that total area of the SRAM cell can be further reduced by using optimization methods (like Euler method). Since basic motto of this SRAM cell design is to understand the layout methodology no optimization effort is put.

1.6 SRAM cell array: schematic and working

Figure (1.6) shows a cell array SRAM which comprises of total eight cells organized into one row and 8 columns. Number of cells in each column can be extended to 128 or more than that depending on the specification of the SRAM. In addition to SRAM cells, supporting circuits like sense amplifiers and precharge and equalization circuits are connected to BL and BLbar lines of columns. To test working of 3x8 decoder along with memory cells, instead of addressing whole 8 bits by one address, each column is addressed by each output of decoder.

BL and BLbar signals are connected to internal data lines. Read driver circuit has these DL and DLbar lines as its input and output is connected to chip data I/O pin. For the write circuitry chip I/O becomes input and DL and DLbar lines become output.

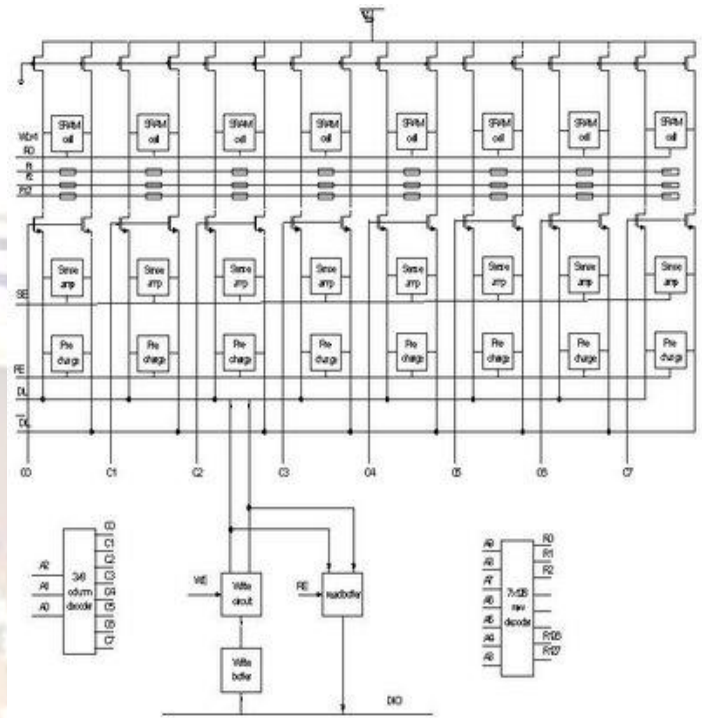


Figure (1.6) SRAM cell array

The same circuit can be extended to 128x8 block memory. This can be accomplished by adding additional SRAM cells in each column. Total 128 SRAM cells can be added in a column. These cells are addressed by a 7x128 row decoder. The outputs of row decoder from R0 to R127 are connected to word lines of individual row SRAM cells. All WL of each row SRAM cells are tied together. Thus with the help of total 10 address bits we can address whole 128x8 block of 2^{10}=1024 bits. To make simulation process and analysis simple, only one row and 8 columns (i.e. total 8 SRAM cells) is constructed. Once it is proved that this cell array works as expected then the same concept can be extended for higher size of SRAM.

The precharge transistors used above SRAM cells in Figure (1.6) can be omitted if precharge block is used and vice versa. Precharge circuit speeds up the read operation. Sense amplifier is used to sense the data available in the SRAM cell. The working and simulation analysis of sense amplifier, precharge circuit and address decoder are discussed in detail in Chapter 2.

Read operation:

At startup both decoders are inactive. As soon as decoders are enabled either by separate address enable signal or chip enable signal, they are precharged first. This process makes all output high for a small amount of time. This address is invalid. Then address settles down according to the input of the decoder and one particular SRAM cell is activated.

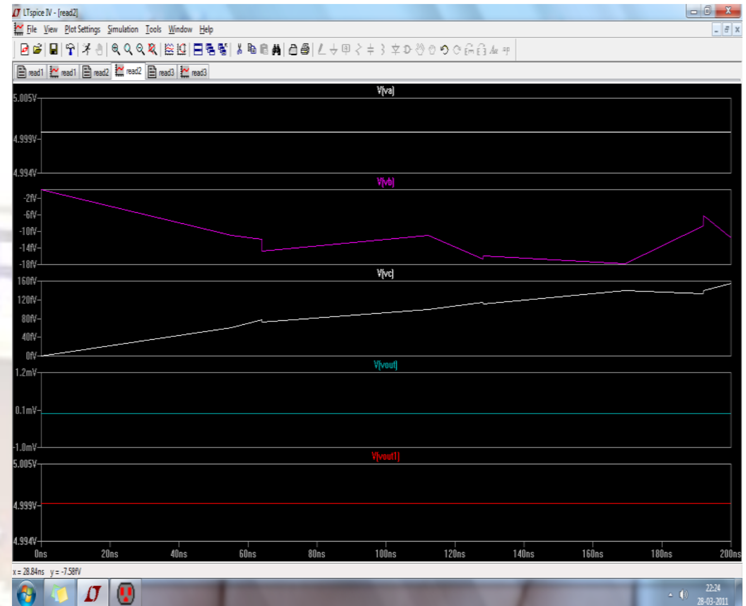
To begin the read operation, precharge circuit is enabled by activating PE for a small amount of time and then disabled. This process precharges BL and BLbar lines to either V_{DD} or $V_{DD}/2$ depending on the precharge circuit used. To sense the voltage difference established at BL and BLbar, sense amplifier is enabled. Sense amplifier reinforces the state of the BL and BLbar lines. Activation of read enable (RE) signal enables the read buffer. Since BL and BLbar lines are commonly connected DL and DLbar lines and these two signals are input to read buffer. The read SRAM cell data traverses towards read buffer. The read buffer reads both DL and DLbar lines and outputs the data available in DL line.

Thus the data bit is read from memory cell. To continue the read operation address bits are changed to address the next memory cell. Precharge is activated and then deactivated. Since sense amplifier and read buffer is already activated read data is immediately available at the output of the buffer. For simulation PE, SE and RE are separately forced. But in practical cases taking all these enable signals to chip I/O may not be efficient design strategy. A single read enable signal is provided for the chip. One more circuitry has to be added which provides sufficient delay between PE, SE and RE so that all circuits are enabled one by one.

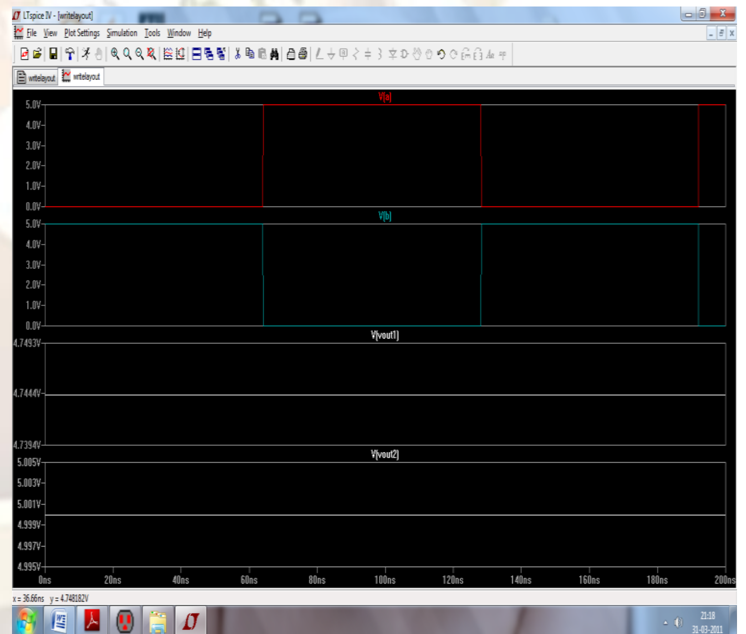
Write operation:

For the write operation PE, SE and RE signal is disabled which disables all read related circuits from interacting with SRAM cell. The address is selected and data is given to write circuit as input. Upon the activation of write enable (WE) signal, write buffer output change according to the input. The outputs are connected to DL and DLbar lines and hence BL and BLbar lines, both signals are forced to change to a new value. The feedback action in SRAM cell then stabilizes the data of the memory. WE signal is then disabled for safe write operation and to avoid further writing of spurious data. To continue the write operation to other cells address bits are changed and same procedure is repeated.

V. RESULTS



Sram read simulation results



Sram write simulation results

VI. CONCLUSION

Single bit SRAM cell is designed and simulated. From the simulation and related analysis it is found that access transistor size plays vital role in the memory bit design. The latch transistors should be matched and access transistors must be twice of the PMOS transistor size. Layout is drawn and area required is approximately 1µ x 0.7 µ. Applying optimization methods will reduce the area required for the cell. Further study and analysis of extracted parasitic values and its affect on circuit functionality will prove beneficial to include the cell in a standard cell library.

REFERENCES

1. M. Fukuma, H. Furuta, and M. Takada, "Memory LSI reliability," *Proc.IEEE*, vol. 81, no. 5, pp. 768–775, May 1993.
2. R. Rodriguez, R. V. Joshi, J. H. Stathis, and C. T. Chuang, "Oxide breakdown model and its impact on SRAM cell functionality," in *Proc. IEEE SISPAD*, Sep. 2003, pp. 283–286.
3. X. Li, J. D. Walter, and J. B. Bernstein, "Simulating and improving microelectronic device reliability by scaling voltage and temperature," in *Proc. IEEE 6th ISQED*, Mar. 2005, pp. 496–502.
4. W. J. Hsu, B. J. Sheu, S. M. Gowda, and C. G. Hwang, "Advanced integrated-circuit reliability simulation including dynamic stress effects,"*IEEE J. Solid State Circuits*, vol. 27, no. 3, pp. 247–257, Mar. 1992..