

Offset Reduction in the Double tailed latch-type Voltage Sense Amplifier

Jagdish Jolia

Electronics and Communication Dept.
Vishwakarma Govt. Engineering College,
Gandhinagar, India

Abstract—This paper presents an improved double tailed latch-type voltage Sense Amplifier using a latch load in the first stage. A latch load at the first stage provides the second stage with large input difference voltage. Thus completely removes the offset voltage due to mismatch in transistor pairs in the second stage of Sense Amplifier. The Performance of the Sense Amplifier was Simulated using LtSpice with threshold mismatch of 10% between transistor pairs of the second stage, where it achieved offset removal at 3GHz clock rate with $V_{DD}=1.2V$ in 90nm CMOS technology. Since the input transistors of the first stage are in parallel with transistor pair of the latch, it does not affect the delay.

Keywords-latch load; delay; offset reduction.

I. INTRODUCTION

Comparators are used for many application such as analog to digital converters(ADCs), memory sense amplifier and data receivers[1]. Fast speed and low power consumption are the two most important parameter of the comparator which are to be used in high speed ADCs. The technology scaling of MOS transistors enables high-speed and low-power operation but the offset voltage of the comparator is increased due to the transistor mismatch[2]. Different architectures like preamplifier based comparator and the latch based comparators have developed but the prove to be inefficient in one or the other way. A fully dyanamic latch based architecture with two stage prove efficient for the high speed, low power consumption and low offset. While these comparators can reduce the offset voltage than the previous comparators but they are not able to fully remove the offset voltage in the second stage thus giving a total offset voltage (offset voltage of first stage + offset voltage of the second stage).A new technique which uses the latch as load in the first stage is used to fully remove the offset voltage in the second stage[4].

A Double tail latch-type voltage Sense Amplifier shown in fig.1 is a fully dynamic comparator with high-speed, low-offset, low power consumption [3]. However these design reduce the effect of the offset voltage due to mismatch in the second stage (M6 and M7, M8 and M9, M10 and M11), it can not remove it completely because of the lower differential voltage at the second stage as shown in fig.2.

In this paper a double tail latch-type Sense Amplifier with the latched load are proposed. In these proposed Sense Amplifiers as shown in fig.3 and fig.4, a latch is used as a load in the first stage for large differential voltage for the second stage input to remove the offset completely. As shown in fig.6 and fig.7, the differential voltage is wide enough to overcome wide range Offset voltage in the input of the second stage.

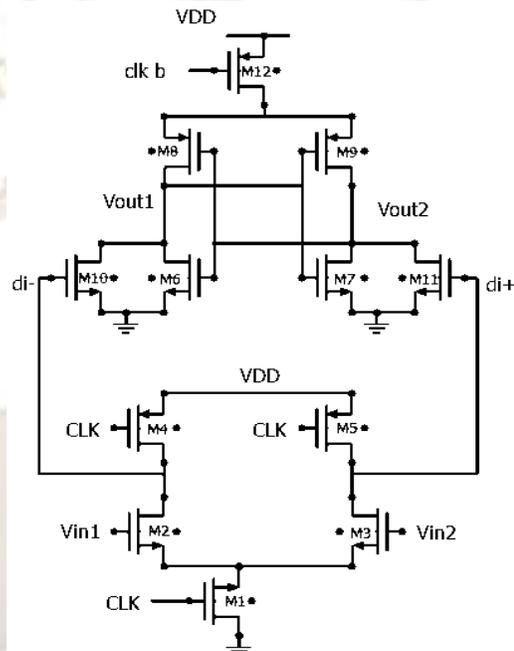


Figure 1. Double tail latch-type Voltage Sense Amplifier.

II. CIRCUIT DESIGN

A. LATCHED LOAD

A latched load for the large voltage difference for second stage input is shown in fig.3. In this structure a cascode-connected dynamic latch is used as the load of the first stage to increase the voltage difference [4]. However due to cascode connection the delay is increased. In fig.4 modified connection of the latch is used, here input transistors are in parallel with a pair of transistors in latch and thus delay is reduced. However in this structure

accurate timing of the CLKB is required as shown in fig.5.

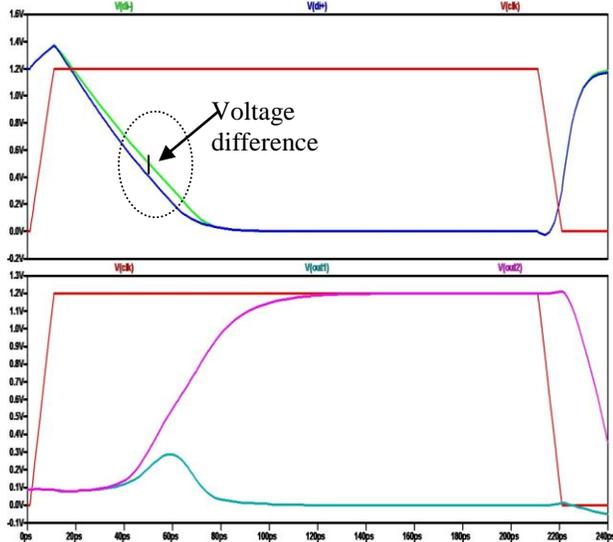


Figure 2. Waveform of Double tail latch-type Voltage Sense Amplifier: (a) Differential voltage $Di+$ and $Di-$. (b) Output $Out1$ and $Out2$.

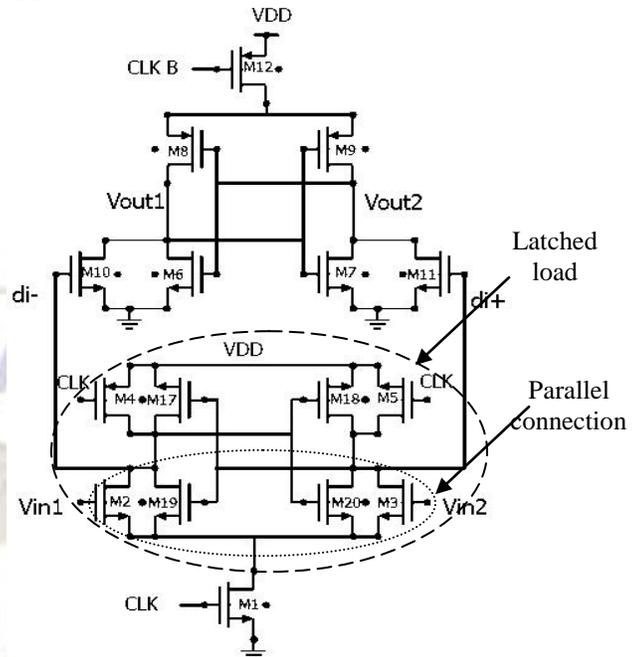


Figure 4. Double tail latch-type Voltage Sense Amplifier with latched load (parallel connection).

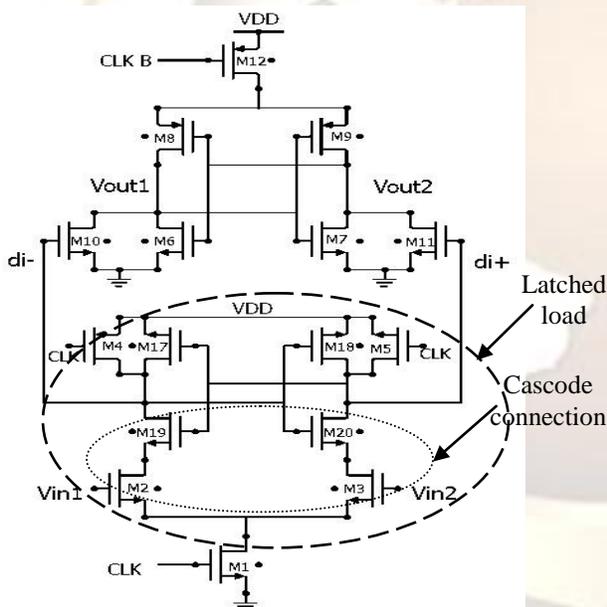


Figure 3. Double tail latch-type Voltage Sense Amplifier with latched load (cascode connection).

OPERATION

Both of these structures operate in a similar way. During the reset phase ($CLK=0V$ and $CLKB=V_{DD}$), transistors $M4$ and $M5$ precharge the Di nodes to V_{DD} , which causes $M10$ and $M11$ to discharge the output nodes to ground. After the reset phase, in the evaluation phase ($CLK=V_{DD}$ and $CLKB=0V$), the tail transistor $M1$ and $M12$ turns ON and the latch of the first stage start regenerating depending on the input differential voltage ($Vin1 - Vin2$), Producing a large difference voltage. This difference voltage is sense at the second stage input and the second stage latch regenerate output voltage $Out1$ and $Out2$ as shown in the fig.6 and fig.7.

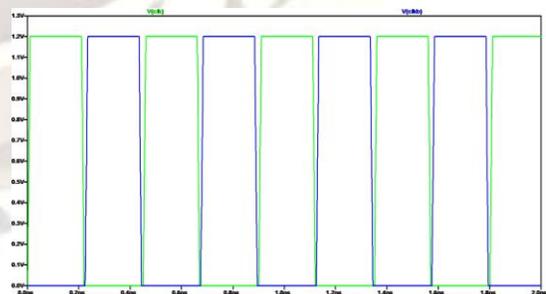


Figure 5. Accurate Waveform of CLK and $CLKB$ for zero offset in SA with parallel connected latch load.

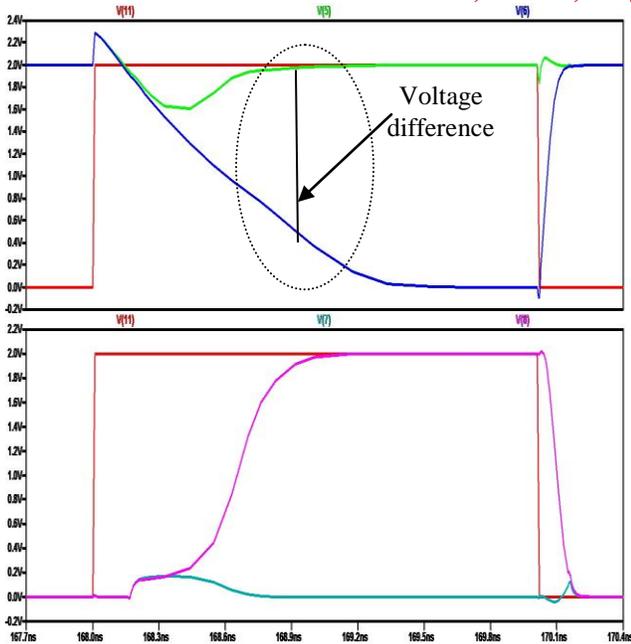


Figure 6. Waveform of Double tail latch-type Voltage Sense Amplifier with cascode connection: (a) Differential voltage Di+ and Di-. (b)Output voltage Out1 and Out2.

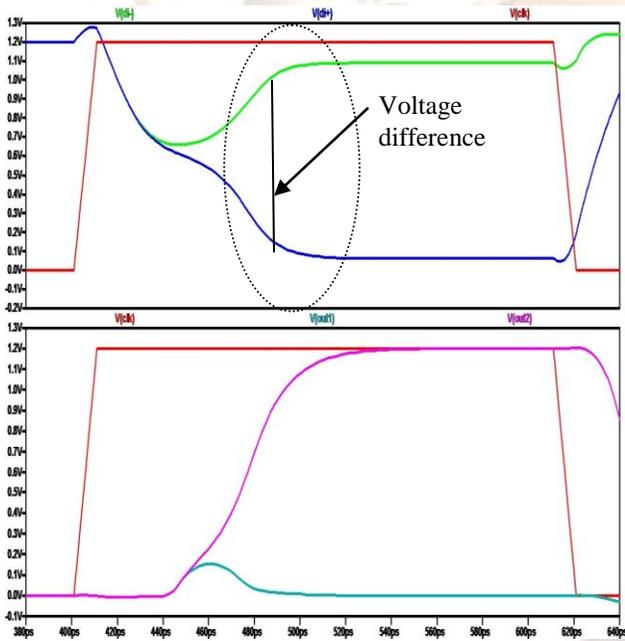


Figure 7. Waveform of Double tail latch-type Voltage Sense Amplifier with parallel connection: (a) Differential voltage Di+ and Di-. (b)Output Out1 and Out2.

III. SIMULATION RESULTS

To compare both these Sense Amplifiers (SAs), both circuits are simulated in LtSpice Simulator with same transistor dimensions (here it is assumed that first stage of

both SAs are completely matched). The operating conditions are $V_{DD}=1.2V$ and $f_{clk} = 3GHz$ and the input has common voltage $V_{CM} = 0.6V$. The proposed Sense Amplifier shows zero offset for any transistor pair mismatch in the second stage. Offset voltage for the mismatch in transistor pairs of the second stage is shown in table 1. For the mismatch of transistor pair M1 and M2 all the three Sense Amplifiers have the same offset voltage.

TABLE I.

SAs	Offset in mV due to mismatch in transistor pair		
	M6 & M7	M8 & M9	M10 & M11
Conventional SA	4	2	3
SA with cascode connected latch load	0	0	0
SA with parallel connected latch load.	0	0	0

CONCLUSION

A low-power and low-offset Sense Amplifier using a latched load is proposed. The latch load effectively removes the offset voltage in second stage. Thus the overall offset voltage (when offset in the first is considered) of Sense Amplifier can be reduced using latched load. However for the Sense Amplifier with cascode-connected latch the delay is increased where as for the Sense Amplifier with parallel connected latch the delay remains the same but it needs accurate timing of the CLKB. Results obtained from simulation confirm the advantages of the proposed Sense Amplifiers.

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