

## **Three Phase AC-AC Converter Using Nine Switch (IGBTS) Converter Topology**

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### **ABSTRACT**

**This project proposes a novel three phase nine switch AC/AC converter topology. This converter features sinusoidal inputs and outputs, unity power factor, and more importantly, low manufacturing cost. The Operating principle of the Converter is elaborated, its modulation schemes are also discussed, and experimental results from a 5kVA prototype system are provided.**

*Keywords:* AC-AC converter, IGBT.

### **I. INTRODUCTION**

Three-phase AC/DC/AC and AC/AC converters with variable frequency (VF) and variable voltage operation have found wide applications in the industry. The most popular configuration uses voltage source inverter (VSI) with a diode rectifier as the front end for adjustable speed drives (ASDs), uninterruptible power supplies (UPS), and other industrial applications. This configuration features low cost and reliable operation due to the use of a diode rectifier, but it generates highly distorted input line currents and does not have regenerative or dynamic braking capability [6]. These problems can be mitigated by using a back-to back two-level voltage source converter (B2B 2L-VSC), shown in Fig. 2, where a pulse width modulation (PWM) voltage source rectifier is used to replace the diode rectifier. The B2B 2L-VSC requires a relatively high number (12) of active switches such as insulated gate bipolar transistors (IGBTs). It also needs a dc-link capacitor that is responsible for a limited lifespan and increased cost.

To reduce the device count and minimize/eliminate the dc-capacitor filter, various converter topologies have been proposed in the literature. The first approach reported in previous papers puts two dc capacitors in cascade and takes their midpoint as one of the input-output terminals, whereby an entire phase leg for the rectifier and/or inverter can be saved. It is also possible to reduce the total number of switches, as the second approach suggests by sharing one of the three phase legs between the rectifier and inverter with proper control. In addition, combined use of dc midpoint connection and phase leg sharing has been proposed in previous papers, where only four legs are needed to perform three-phase ac to ac conversion with bidirectional power flow and power factor control [5]. Although all the earlier references achieve the goal of reducing the number of switches and thus reducing the

cost, they unexceptionally have limits or involve complex control due to their unbalanced topological structure.

With the recent progress in power semiconductor device technology followed by advancements in power electronic control methods, variable frequency inverter-fed ac drives are being adopted for a wide variety of applications [6]. Recently there has been growing interest in low cost ac drives to meet the needs for reducing cost. Improvements in power semiconductor switch technology have significantly reduced the cost and size of such drives and improved waveform quality. Little change, however, has been made to the basic structure of the conventional ac-ac converter, while significant advances have been made in soft switching techniques and control strategies such as field-oriented drives, sensor-less controls, and adaptive controls. It is well known that a VSI-PWM rectifier and inverter with capacitor dc link is regarded as one of the most important structures for a three phase to three phase power converter [4]. The leakage inductance of the induction motor is shown to emphasize the symmetric structure of the converter. This type of converter normally requires twelve switches for a rectifier and inverter composed of a self turn-off switch such as a power transistor or IGBT with an anti-parallel diode. Compared to a conventional Thyristor converter, the distinguishing advantages of this structure are: 1) capability of unity or even leading power factor, 2) sinusoidal input current waveforms reducing harmonic pollution, 3) bidirectional power flow. A number of low cost topologies have been suggested for fixed and variable speed drives in the low power range.

In this paper, a novel one-stage three-phase AC/AC converter topology is proposed. Different from all other existing topologies, this converter has only three legs with only nine active switches for bi-directional AC/AC power conversion.

### **II. AC-AC CONVERTER**

Three-phase ac-dc-ac converter topologies are developed based on DC link energy storage and number of DC link energy storage converters on the structure of an indirect matrix converter (IMC). The converter topologies, presented in below Fig.1, exhibit a reduced number of power transistors compared to the CMC or IMC and are therefore designated as the sparse matrix converter (SMC) and/or ultra sparse matrix converter (USMC).how many active switches are required for a particular converter is shown below table. 1.

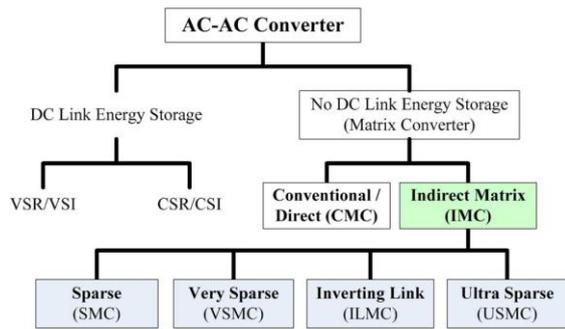


Fig.1 Classification of AC-AC converter topologies.

Converter type	Transistors	Diodes	Isolated driver potentials
CMC	18	18	6(CC),9(CE)
IMC	18	18	8
SMC	15	18	7
VSMC	12	30	10
USMC	9	18	7

Table.1 Realization effort of different matrix converter topologies

2.1 Back-to-Back Two Level VSC

These converters may also be regarded as topologies with a saved number of switches, despite their employment of a large number of diodes. Unlike VSCs that inevitably require the dc-link stage, the matrix converter presents a radical change in topology and directly converts a fixed ac input voltage to an adjustable ac output voltage. It features sinusoidal input-output, controllable power factor, and is capable of bidirectional energy transfer from the supply to the load or vice versa. Since there is no dc link circuit, the dc capacitor in the VSC is not necessary here, leading to cost reduction as well as improved reliability and longevity. However, the conventional matrix converter (CMC) normally requires 18 active switches and its switching scheme is complex.

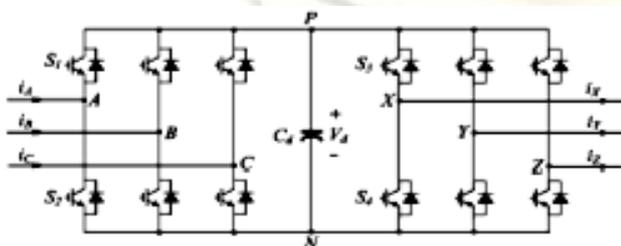


Fig. 2 Circuit diagram of B2B 2L-VSC.

The high semiconductor cost and complex control have made this topology less attractive. Similar to the situation of VSCs, efforts to reduce the number of active switches for a matrix converter have been made in recent publications, where a couple of topological variants such as the sparse matrix converter (SMC) were proposed. The SMC provides equivalent functionality to the CMC. It

employs 15 switches with the semiconductor cost still higher than that of the B2B 2 L-VSC.

Switching states	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	V <sub>AN</sub>	V <sub>XN</sub>
1	On	Off	On	Off	V <sub>d</sub>	V <sub>d</sub>
2	Off	On	Off	On	0	0
3	On	Off	Off	On	V <sub>d</sub>	0
4	Off	On	On	Off	0	V <sub>d</sub>

Table.2 Switching states and converter leg voltages for B2B 2L-VSC

The reduction of the number of switches in the proposed converter topology imposes certain switching constraints for the switching pattern design. In the B2B 2L-VSC shown in Fig.2, the rectifier leg voltage  $V_{an}$ , which is the voltage at node A with respect to the negative dc bus N, can be controlled 2 L-VSC. by switches S1 and S2 in the rectifier, whereas the inverter leg voltage  $V_{xn}$  can be controlled by S3 and S4 in the inverter. This means that the rectifier and inverter leg voltages can be controlled independently. The B2B 2L-VSC has four switching states per phase, as defined in Table 2.

III. PROPOSED NINE SWITCH CONVERTER TOPOLOGY

The figure below shows the proposed three-phase nine-switch converter topology. This converter has only three legs with three switches installed on each of them. The novelty here is that the middle switch in each individual leg is shared by both the rectifier and the inverter, thereby reducing the switch count by 33% and 50% in comparison to the B2B 2L-VSC and CMC, respectively. The input power is delivered to the output partially through the middle three switches and partially through a quasi-dc-link circuit. For the convenience of discussion, we can consider that the rectifier of the nine-switch converter is composed of the top three and middle three switches, whereas the inverter consists of the middle three and bottom three switches.

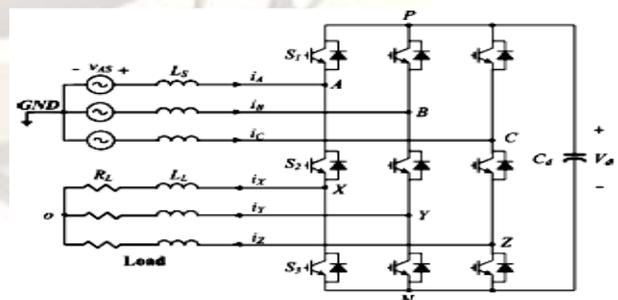


Fig.3 Proposed Nine-switch AC/AC converter with a quasi-dc link

The converter has two modes of operation: 1) constant frequency (CF) mode, where the output frequency of the inverter is constant and also the same as that of the utility supply, while the inverter output voltage is adjustable; and 2) VF mode, where both magnitude and frequency of the inverter output voltage are adjustable.

The CF-mode operation is particularly suitable for applications in UPS, whereas the VF mode can be applied to Variable-speed drives [6]. For the nine-switch topology, the control of the input and output voltages has to be accomplished through the three switches on each leg. Because the middle switches are shared by the rectifier and inverter, the proposed converter has only three switching states per phase, as listed in Table 3. It can be observed that switching state 4 for the B2B 2L-VSC does not exist in the nine-switch converter, which implies that the inverter leg voltage  $V_{XN}$  cannot be higher than the rectifier leg voltage  $V_{AN}$  at any instant. This is, in fact, the main constraint for the switching scheme design of the nine-switch converter.

The output voltage of the rectifier is ripple DC such type of ripples can be eliminated by using the modulation techniques the harmonics also reduced at the inverter output side.

Switching states	$S_1$	$S_2$	$S_3$	$V_{AN}$	$V_{XN}$
1	On	On	Off	$V_d$	$V_d$
2	Off	On	On	0	0
3	On	Off	On	$V_d$	0

Table. 3 Switching states and converter leg voltages for proposed topology.

### 3.1 Voltage Source Inverters(VSI)

The main objective of static power converters is to produce an ac output waveform from a dc power supply. According to the type of ac output waveform, the topologies can be considered as voltage source inverters (VSIs), where the independently controlled ac output is a voltage waveform. These structures are the most widely used because they naturally behave as voltage sources as required by many industrial applications, such as adjustable speed drives (ASDs), which are the most popular application of inverters [4]. Similarly, these topologies can be found as current source inverters (CSIs), where the independently controlled ac output is a current waveform. These structures are still widely used in medium-voltage industrial applications, where high-quality voltage waveforms are required.

There are namely two types of Voltage Source Inverters,

- 1) Single Phase VSI
  - a. Half Bridge VSI
  - b. Full Bridge VSI

### 2) Three Phase VSI

Single-phase VSIs cover low-range power applications and three-phase VSIs cover the medium- to high-power applications. The main purpose of these topologies is to provide a three-phase voltage source, where the amplitude, phase, and frequency of the voltages should

always be controllable. Although most of the applications require sinusoidal voltage waveforms (e.g., ASDs, UPSs, FACTS, VAR compensators), arbitrary voltages are also required in some emerging applications (e.g., active filters, voltage compensators). Considering the advantages and the type of application needed three phase VSIs are most widely used, which is explained in detail in next section.

### 3.2 Three Phase Voltage Source Inverters

The standard three-phase VSI topology is shown in Fig.4 and the eight valid switch states are given in Table 4. As in single-phase VSIs, the switches of any leg of the inverter ( $S_1$  and  $S_4$ ,  $S_3$  and  $S_6$ , or  $S_5$  and  $S_2$ ) cannot be switched on simultaneously because this would result in a short circuit across the dc link voltage supply. Similarly, in order to avoid undefined states in the VSI, and thus undefined ac output line voltages, the switches of any leg of the inverter cannot be switched off simultaneously as this will result in voltages that will depend upon the respective line current polarity [4]. Of the eight valid states, two of them (7 and 8 in Table 4) produce zero ac line voltages. In this case, the ac line currents freewheel through either the upper or lower components. The remaining states (1 to 6 in Table 4) produce non-zero ac output voltages. In order to generate a given voltage waveform, the inverter moves from one state to another.

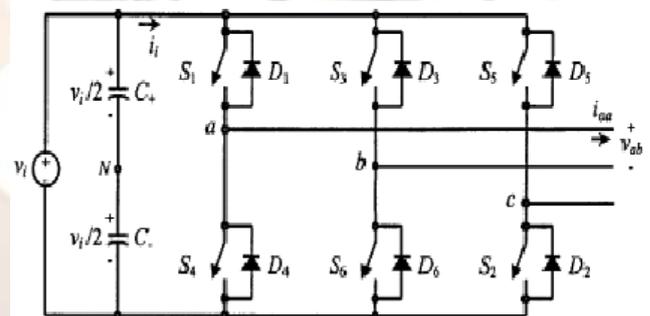


Fig. 4 Three-phase VSI topology

State	State	$i_{ab}$	$v_b$	$v_a$	Space Vector
$1, 2,$ and $6$ are on and $4, 5,$ and $3$ are off	1	$v$	0	$-v$	$V_1 = 1 + j0.5$
$2, 3,$ and $1$ are on and $5, 6,$ and $4$ are off	2	0	$v$	$-v$	$V_2 = j1.155$
$3, 4,$ and $2$ are on and $6, 1,$ and $5$ are off	3	$-v$	$v$	0	$V_3 = -1 + j0.5$
$4, 5,$ and $3$ are on and $1, 2,$ and $6$ are off	4	$-v$	0	$v$	$V_4 = -1 - j0.5$
$5, 6,$ and $4$ are on and $2, 3,$ and $1$ are off	5	0	$-v$	$v$	$V_5 = -j1.155$
$6, 1,$ and $5$ are on and $3, 4,$ and $2$ are off	6	$v$	$-v$	0	$V_6 = 1 - j0.5$
$1, 3,$ and $5$ are on and $4, 6,$ and $2$ are off	7	0	0	0	$V_7 = 0$
$4, 6,$ and $2$ are on and $1, 3,$ and $5$ are off	8	0	0	0	$V_8 = 0$

Table 4 Valid switching states for a three-phase VSI

Thus the resulting ac output line voltages consist of discrete values of voltages that are  $V_i$ , 0, and  $-V_i$  for the topology shown in Fig. 4. The selection of the states in order to generate the given waveform is done by the

modulating technique that should ensure the use of only the valid states.

### 3.3 Pulse Width Modulation in Inverters

Output voltage from an inverter can also be adjusted by exercising a control within the inverter itself. The most efficient method of doing this is by pulse-width modulation control used within an inverter. In this method, a fixed dc input voltage is given to the inverter and a controlled ac output voltage is obtained by adjusting the on and off periods of the inverter components [4]. This is the most popular method of controlling the output voltage and this method is termed as Pulse-Width Modulation (PWM) Control. The different PWM techniques are as under:

- (a) Single-pulse modulation
- (b) Multiple pulse modulation
- (c) Sinusoidal pulse width modulation (SPWM)

#### 3.3.1 SPWM for Three Phase VSI

This is an extension of the one introduced for single-phase VSIs. In this case and in order to produce 120° out-of-phase load voltages, three modulating signals that are 120° out of phase are used. Fig.5 shows the ideal waveforms of three-phase VSI SPWM [4]. In order to use a single carrier signal and preserve the features of the PWM technique, the normalized carrier frequency  $m_f$  should be an odd multiple of 3. Thus, all phase voltages ( $V_{aN}$ ,  $V_{bN}$ , and  $V_{cN}$ ) are identical but 120° out of phase without even harmonics; moreover, harmonics at frequencies a multiple of 3 are identical in amplitude and phase in all phases. For instance, if the ninth harmonic in phase  $aN$  is

$$V_{aN9}(t) = v^{\wedge}_9 \sin(9\omega t) \quad (1)$$

The ninth harmonic in phase  $bN$  will be

$$\begin{aligned} V_{bN9}(t) &= v^{\wedge}_9 \sin(9\omega t - 120^\circ) \\ &= v^{\wedge}_9 \sin(9\omega t - 1080^\circ) \\ &= v^{\wedge}_9 \sin(9\omega t) \end{aligned} \quad (2)$$

Thus, the ac output line voltage  $V_{ab} = V_{aN} - V_{bN}$  will not contain the ninth harmonic. Therefore, for odd multiple of 3 values of the normalized carrier frequency  $m_f$ , the harmonics in the ac output voltage appear at normalized frequencies  $f_h$  centered around  $m_f$  and its multiples, specifically, at

$$h = lm_f \pm k \quad l=1,2,3 \quad (3)$$

Where  $l=1, 3, 5$  for  $k=2, 4, 6$ ; and  $l=2, 4, 6$  for  $k=1, 5, 7$ ; such that  $h$  is not a multiple of 3. Therefore, the harmonics will be at  $m_f \pm 2, m_f \pm 4 \dots 2m_f \pm 1, 2 \pm 5 \dots, 3m_f \pm 2, 3m_f \pm 4 \dots, 4m_f \pm 1, 4m_f \pm 5 \dots$

For nearly sinusoidal ac load current, the harmonics in the dc link current are at frequencies given by

$$h = lm_f \pm k \pm 1 \quad l=1,2 \quad (4)$$

Where  $l=0, 2, 4, \dots$  for  $k=1, 5, 7, \dots$  and  $l=1, 3, 5, \dots$  for  $k=2, 4, 6, \dots$  such that  $h = l * m_f \pm k$  is positive and not a multiple of 3. For instance, Fig. 5.5.1(h) shows the sixth harmonic ( $h=6$ ), which is due to  $h = (1 * 9) - 2 - 1 = 6$ .

The identical conclusions can be drawn for the operation at small and large values of  $m_f$  as for the single-phase configurations. However, because the maximum amplitude of the fundamental phase voltage in the linear region ( $m_a \leq 1$ ) is  $v_i/2$ , the maximum amplitude of the fundamental ac output line voltage is  $v^{\wedge}_{ab1} = (\sqrt{3}v_i)/2$ .

Therefore, we can write,

$$v^{\wedge}_{ab1} = m_a (\sqrt{3}v_i)/2 \quad 0 < m_a < 1 \quad (5)$$

To further increase the amplitude of the load voltage, the amplitude of the modulating signal  $v^{\wedge}_c$  can be made higher than the amplitude of the carrier signal  $v^{\wedge}_A$ , which leads to over modulation. The relationship between the amplitude of the fundamental ac output line voltage and the dc link voltage becomes nonlinear as in single-phase VSIs. Thus, in the over modulation region, the line voltages range in

$$(\sqrt{3}v_i)/2 < v^{\wedge}_{ab1} = v^{\wedge}_{bc1} = v^{\wedge}_{ca1} < (4/\pi) (\sqrt{3}v_i)/2 \quad (6)$$

#### 3.4 Space Vector Pulse Width Modulation for 3-phase VSI

The topology of a three-leg voltage source inverter is shown in Fig.6. Because of the constraint that the input lines must never be shorted and the output current must always be continuous a voltage source inverter can assume only eight distinct topologies [4]. These topologies are shown on Fig.6. Six out of these eight topologies produce a non zero output voltage and are known as non-zero switching states and the remaining two topologies produce zero output voltage and are known as zero switching-states.

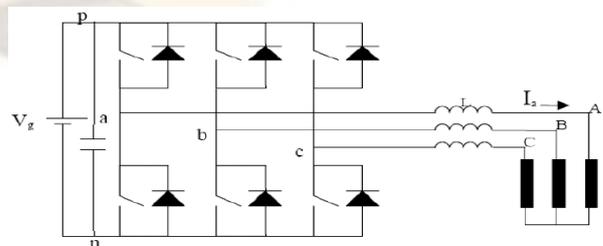


Fig.6 Topology of a three-leg voltage source inverter

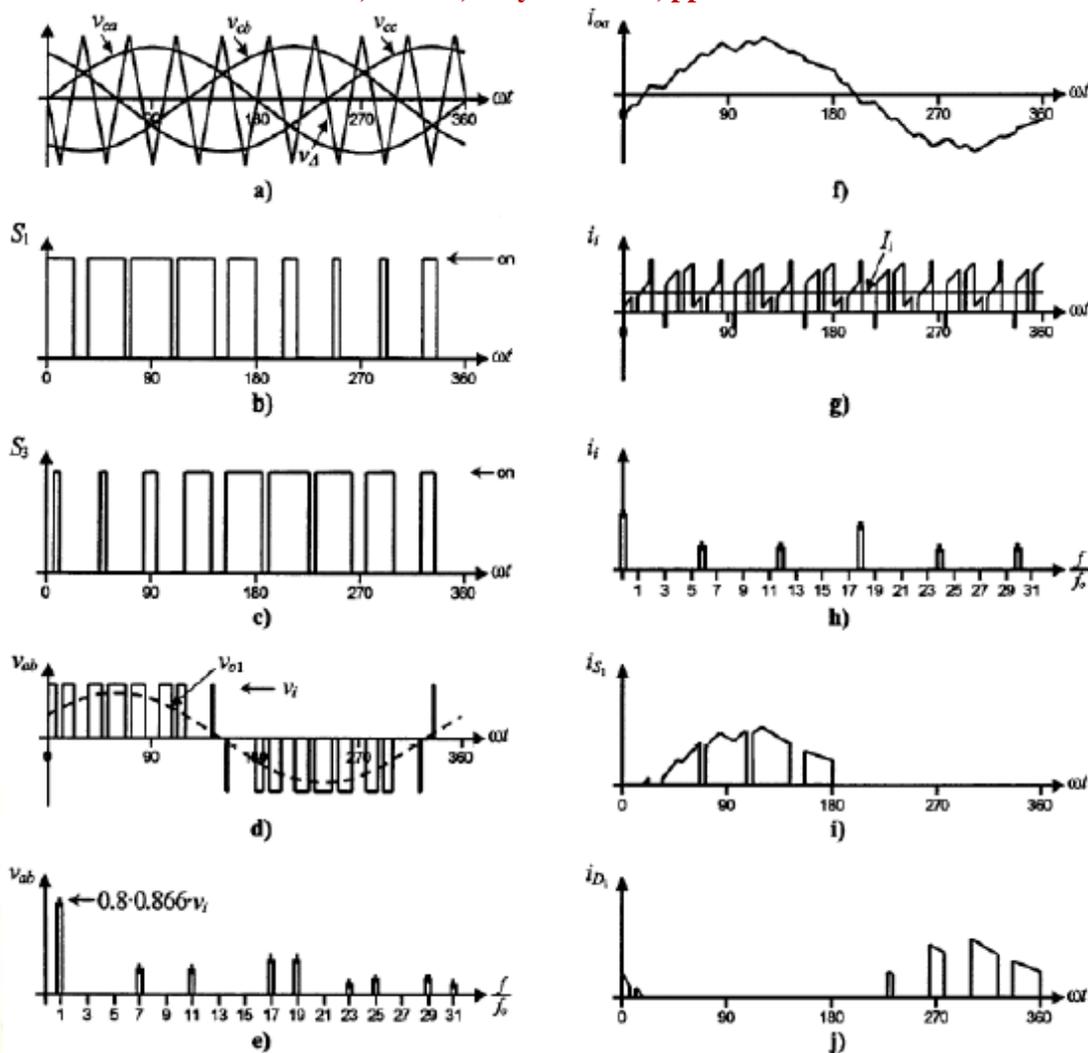


Fig. 5 The three-phase VSI. Ideal waveforms for the SPWM ( $m_a = 0.8$ ,  $m_f = 0.9$ ): carrier and modulating signals; (b) switch S1 state; (c) switch S3 state; (d) ac output voltage; (e) ac output voltage spectrum; (f) ac output current; (g) dc current; (h) dc current spectrum; (i) switch S1 current; (j) diode D1 current.

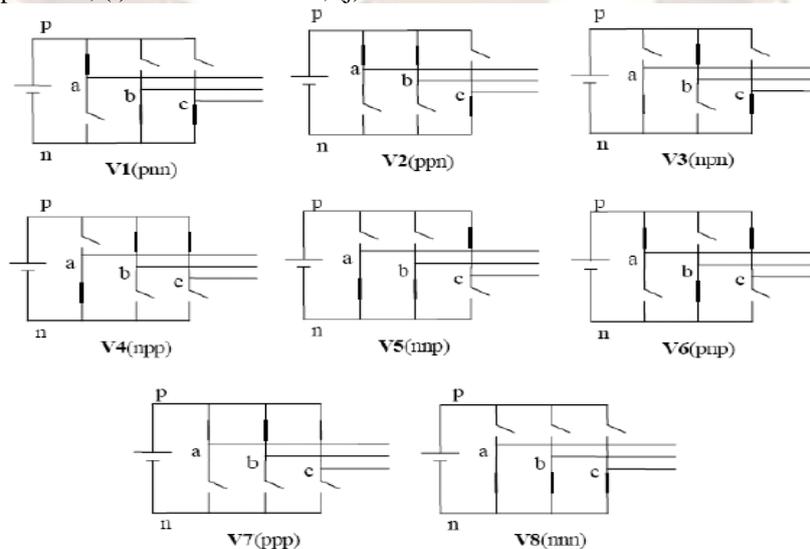


Fig.7 Eight switching topology of voltage source inverter

3.4.1 Voltage Space Vectors

Space vector modulation (SVM) for three-leg VSI is based on the representation of the three phase quantities as vectors in a two-dimensional ( $\alpha \beta$ ) plane. This is illustrated here for the sake of completeness. Considering topology 1 of Fig.7, which is repeated in Fig.8 we see that the line voltages  $V_{ab}$ ,  $V_{bc}$ , and  $V_{ca}$  are given by

$$\begin{aligned} V_{ab} &= V_g \\ V_{bc} &= 0 \\ V_{ca} &= -V_g \end{aligned} \tag{7}$$

This can be represented in the  $\alpha \beta$ , plane as shown in Fig.9, where voltages  $V_{ab}$ ,  $V_{bc}$ , and  $V_{ca}$  are three line voltage vectors displaced 120 in space. The effective voltage vector generated by this topology is represented as **V1** (pnn) in Fig.9. Here the notation “pnn” refers to the three legs/phases a,b,c being either connected to the positive dc rail (p) or to the negative dc rail (n). Thus “pnn” corresponds to “phase a” being connected to the positive dc rail and phases b and c being connected to the negative dc rail.

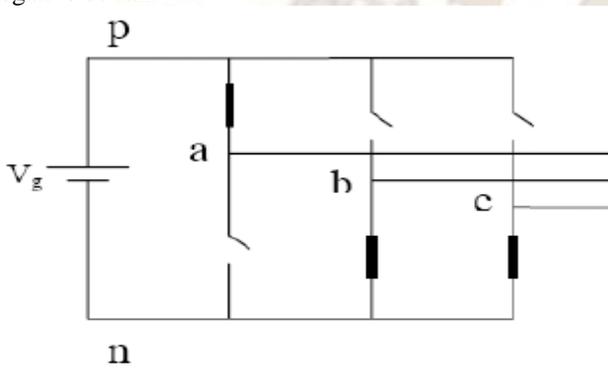


Fig.8 Topology1-V1 (pnn) of a voltage source inverter

3.4.2 Representation of topology 1 in  $\alpha\text{-}\beta$  plane

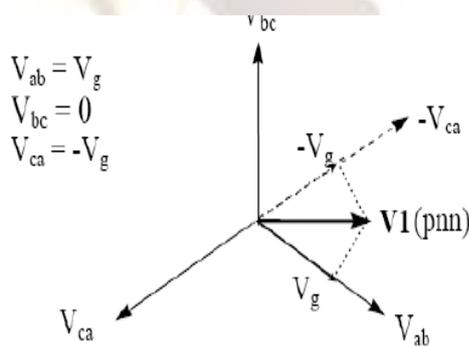


Fig.9 Representation of topology 1 in the  $\alpha\text{-}\beta$  plane

Proceeding on similar lines the six non-zero voltage vectors (**V1** - **V6**) can be shown to assume the positions shown in Fig.10. The tips of these vectors form a regular hexagon (dotted line in Fig.10). We define the area enclosed by two adjacent vectors, within the hexagon, as a sector.

3.4.3 Non zero voltage vectors in the  $\alpha\text{-}\beta$  plane

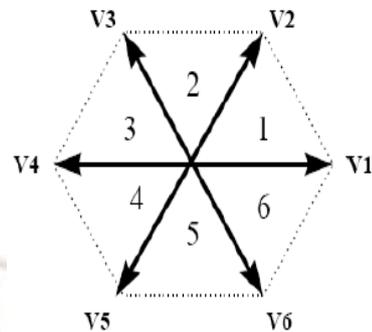


Fig.10 Non-zero voltage vectors in the  $\alpha\text{-}\beta$  plane

Considering the last two topologies of Fig.7, which are repeated in Fig.11 for the sake of convenience, we see that the output line voltages generated by this topology are given by

$$\begin{aligned} V_{ab} &= 0 \\ V_{bc} &= 0 \\ V_{ca} &= 0 \end{aligned} \tag{8}$$

These are represented as vectors, which have zero magnitude and hence are referred to as zero-switching state vectors or zero voltage vectors. They assume the position at origin in the  $\alpha\beta$ , plane as shown in Fig.12. The vectors **V1**-**V8** are called the switching state vectors (SSVs).

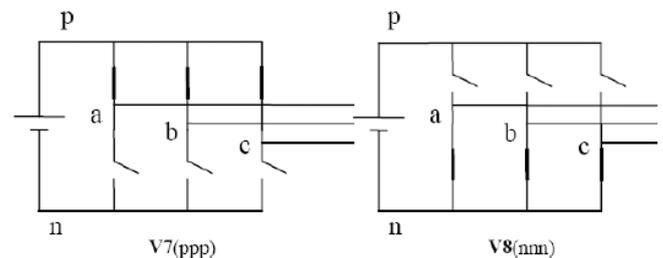


Fig.11 Zero output voltage topologies.

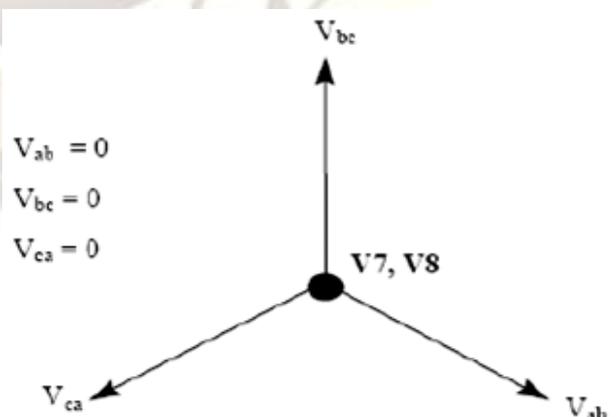


Fig.12 Representation of the zero voltage vectors in the  $\alpha\text{-}\beta$  plane

IV. SPACE VECTOR MODULATION

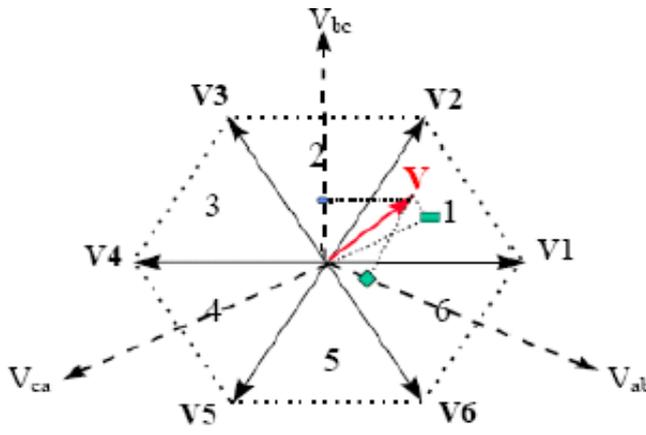


Fig.13 Output voltage vector in the  $\alpha$ - $\beta$  plane

The space vector PWM (SVM) method is an advanced computation-intensive PWM method and is possibly the best among all the PWM techniques for variable-frequency drive applications. Because of its superior performance characteristics, it has been finding wide speed applications in recent years. The desired three phase voltages at the output of the inverter could be represented by an equivalent vector  $V$  rotating in the counter clockwise direction as shown in Fig.13. The magnitude of this vector is related to the magnitude of the output voltage (Fig.14) and the time this vector takes to complete one revolution is the same as the fundamental time period of the output voltage.

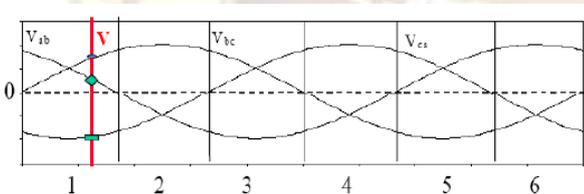


Fig.14 Output line voltages in time domain

Let us consider the situation when the desired line-to-line output voltage vector  $V$  is in sector 1 as shown in Fig 6.5.3. . This vector could be synthesized by the pulse-width modulation (PWM) of the two adjacent SSV's  $V1$  (pnn) and  $V2$  (ppn), the duty cycle of each being  $d1$  and  $d2$ , respectively, and the zero vector ( $V7$ (nnn) /  $V8$ (ppp) ) of duty cycle  $d0$ :

$$d_1 V_1 + d_2 V_2 = V = m V_g e^{j\theta} \tag{9}$$

$$d_1 + d_2 + d_0 = 0 \tag{10}$$

Where,  $0 \leq m \leq 0.866$  is the modulation index. This would correspond to a maximum line-to-line voltage of  $1.0V_g$ , which is 15% more than conventional sinusoidal PWM as shown.

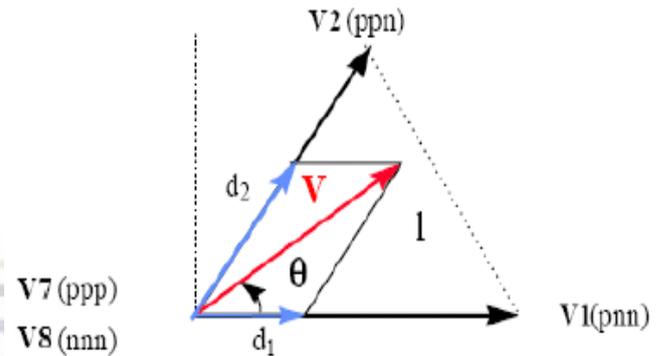


Fig.15 Synthesis of the required output voltage vector in sector 1

All SVM schemes and most of the other PWM algorithms use Eqns. (9) and (10) for the output voltage synthesis. The modulation algorithms that use non-adjacent SSV's have been shown to produce higher THD and/or switching losses and are not analyzed here, although some of them, e.g. hysteresis, can be very simple to implement and can provide faster transient response. The duty cycles  $d1$ ,  $d2$ , and  $d0$ , are uniquely determined, and Eqns. (9) and (10), the only difference between PWM schemes that use adjacent vectors is the choice of the zero vector(s) and the sequence in which the vectors are applied within the switching cycle.

The degrees of freedom we have in the choice of a given modulation algorithm is:

- 1) The choice of the zero vector; whether we would like to use  $V7$ (ppp) or  $V8$ (nnn) or both,
- 2) Sequencing of the vectors
- 3) Splitting of the duty cycles of the vectors without introducing additional commutations.

4.1 Output voltages of three-phase inverter

$S1$  through  $S6$  are the six power transistors that shape the output voltages. When an upper switch is turned on (i.e., a, b or c is "1"), the corresponding lower switch is turned off (i.e., a', b' or c' is "0").

Eight possible combinations of on and off patterns for the three upper transistors ( $S1, S3, S5$ )

Line to line voltage vector  $[V_{ab} \ V_{bc} \ V_{ca}]^t$

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix}, \text{ where switching variable vector } [a \ b \ c]^t \tag{11}$$

Line to neutral (phase) voltage vector  $[V_{an} \ V_{bn} \ V_{cn}]^t$

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{1}{3} V_{dc} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{12}$$

4.2 Basic switching vectors and Sectors

- 6 active vectors (V<sub>1</sub>, V<sub>2</sub>, V<sub>3</sub>, V<sub>4</sub>, V<sub>5</sub>, V<sub>6</sub>)
  1. Axes of a hexagonal.
  2. DC link voltage is supplied to the load.
  3. Each sector (1 to 6): 60 degrees.
  
- Two zero vectors (V<sub>0</sub>, V<sub>7</sub>)
  1. At origin
  2. No voltage is supplied to the load

$$P(\theta) = \frac{2}{3} \begin{bmatrix} \cos \theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta - \frac{4\pi}{3}) \\ -\sin \theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{4\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}$$

which we rewrite for the angle  $\theta=0$  and we obtain the matrix of Clarke transformation [3]. We make orthogonal the Clarke matrix (we divide every vector column through its norm) and we obtain the Concordia matrix of  $abc-\alpha\beta$  transformation:

$$[C_c] = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

V. MATLAB SIMULINK OF THE SVM GENERATORS

The Simulink scheme of the SVM generator is formed by seven subsystems disposed on the structure of the operating principle scheme, presented in fig.16, each of this having its own Simulink model. The below sections show the main blocks from the scheme, their role and the equations on which they were built [1].

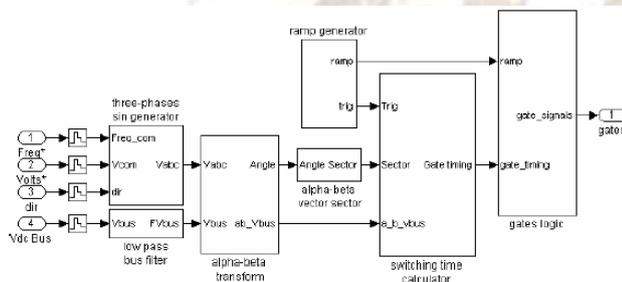


Fig.16 Simulink scheme of SVM generator

This subsystem (Fig.7.1.2) realizes three sine waves with variable frequency and amplitude, which are out of phase with each other by 120 degrees, being composed of the `sin_phi_0`, `sin_phi_240` and `sin_phi_120` blocks [6]. These have Simulink schemes, which applied sin function, being different only from the applied phase shift (0, -120, 120).

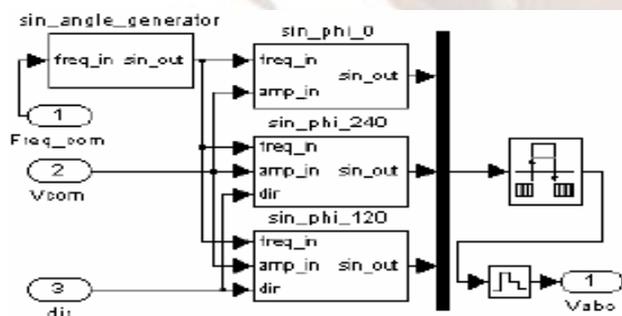


Fig.17 The three phase sine generator-Simulink scheme

To write the equations of transformation  $abc-\alpha\beta$ , we apply the matrix of initial transformation Park  $P(\theta)$ , used for  $abc-dqo$  transformation Fig.18: The Simulink scheme for transform.  $abc-\alpha\beta$

From the multiplication of  $[C_c]$  with the column vector with components  $V_a, V_b, V_c$ , we obtain:

$$V_a = \sqrt{2/3}(V_a - (1/2)V_b - (1/2)V_c) \tag{13}$$

$$V_\beta = \sqrt{2/3}((\frac{\sqrt{3}}{2})V_b - (\frac{\sqrt{3}}{2})V_c) \tag{14}$$

relations which are presented in Simulink scheme in Fig. 18. The signal *Angle* is obtained when we apply  $arctg(V_\beta/V_a)$ .

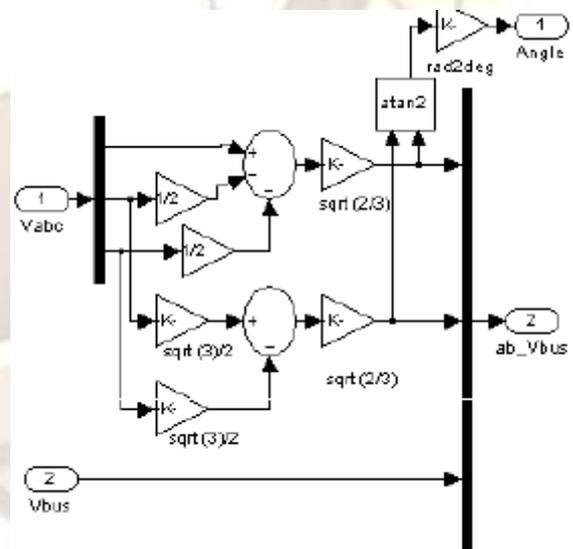


Fig.18 The Simulink scheme for transform.  $abc-\alpha\beta$

The subsystem determines the sector (I, II, III, IV, V or VI) in which the voltage vector lies, comparing the signal *Angle* with the limits of every sector: (0, 60 0), (60 0, 120 0), (120 0, 180 0), (-180 0, -120 0), (-120 0, - 60 0), (-60 0, 0) and multiply the resultant signal by coefficient: 1, 2, 3, 4, 5, 6 so that the output signal is periodical, in six stages of amplitude.

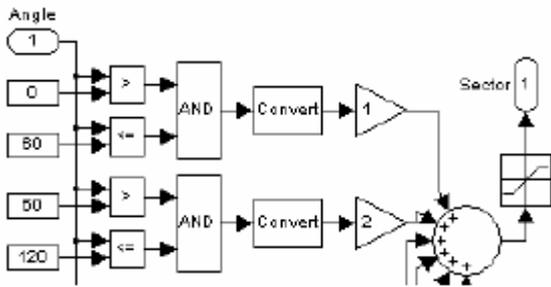


Fig.19 The  $\alpha\beta$  vector sector – Simulink scheme

In Fig.19 the Simulink partial scheme of the subsystem for I and II sector and it is completed in the same way for the other sectors are represented.

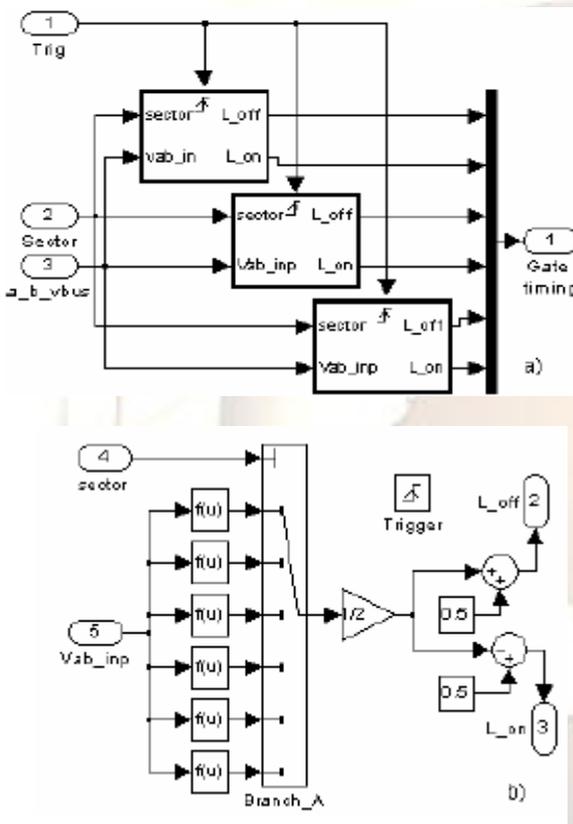


Fig. 20: a) The switching time calc- Simulink scheme  
b) Detail block corresponding to A branch

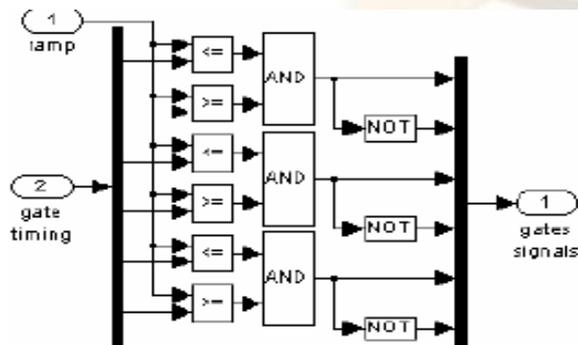


Fig.21 The Logic Gates

5.1 Simulink components in SVM

Low pass bus filter:

It is used to remove the fast transients from the DC bus voltage measurement. This measure is used to compute the voltage vector applied to the motor.

$\alpha\beta$  Transformation:

It converts the variables from three phase to two phase quantities.

Switching time calculator:

To calculate the timing of the voltage vector applied to the motor.

Gate logic:

It receives the timing sequence from the switching time calculator and the ramp from the ramp generator. This block compares the ramp and the gate timing signals to activate the Inverter switches at the proper time.

Zero order hold:

It converts the sample signal to the continuous time signals.

Rate transition:

It transfer data from the output  $f_o$  a block operating at one rate to the input of another block operating at different rate.

Saturation:

It imposes lower and upper bounds on a signal.

5.2 Simulation parameters

The performance of the proposed nine-switch converter topology is simulated with the Mat lab/Simulink software. In the simulation, the utility supply is rated at 230 V and 50 Hz with a. driving a three-phase  $RL$  load of  $RL = 8\Omega$  and  $LL = 2.5$  mH. The dc capacitor  $Cd$  is 6000  $\mu$ F. SVPWM method is used to modulate the converter for its superior performance. Over SPWM and higher dc voltage utilization the rectifier is controlled by a vector control scheme with unity power factor operation. The inverter output voltage is not detected, and therefore, is not tightly controlled. The switching frequency of both rectifier and inverter is 4500Hz and sampling time is  $T_s=20e-6$ .

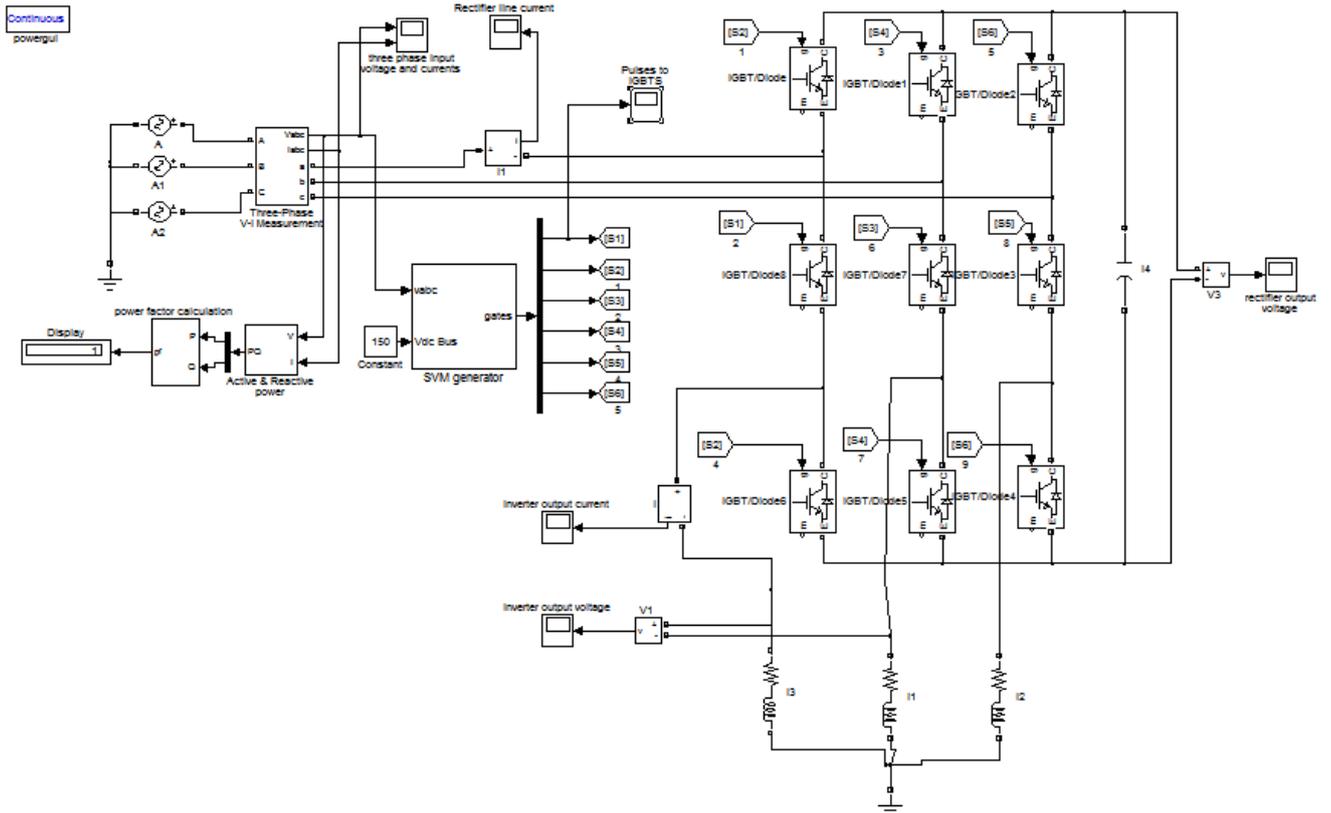


Fig.22 Simulink model of Nine Switch Converter Topology

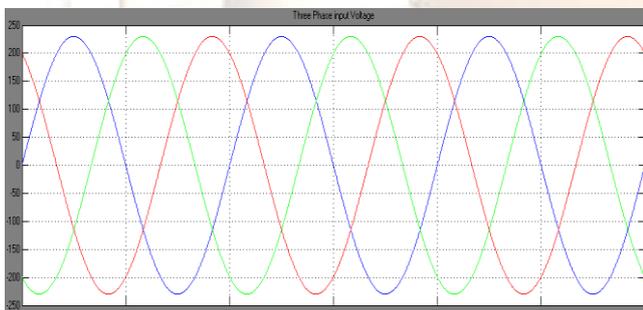


Fig.23 Three Phase Input Voltage

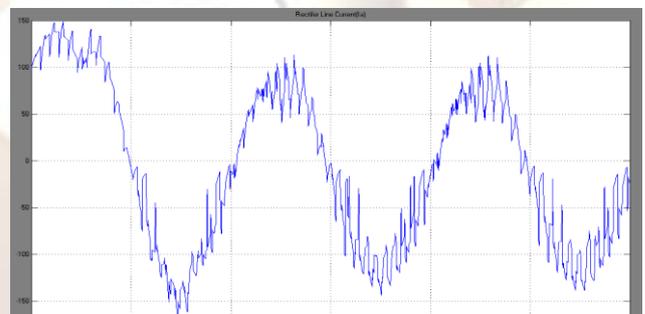


Fig.25 Rectifier Line Current ( $I_a$ )

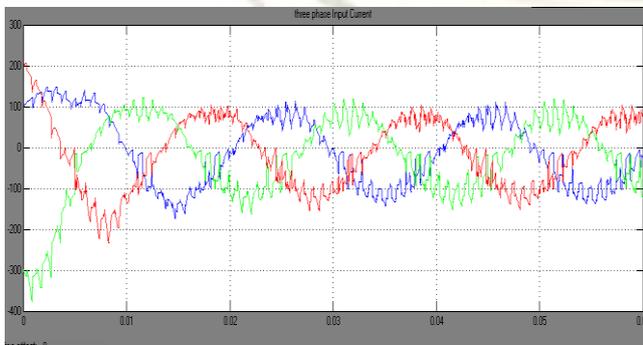


Fig.24 Three Phase Input Current

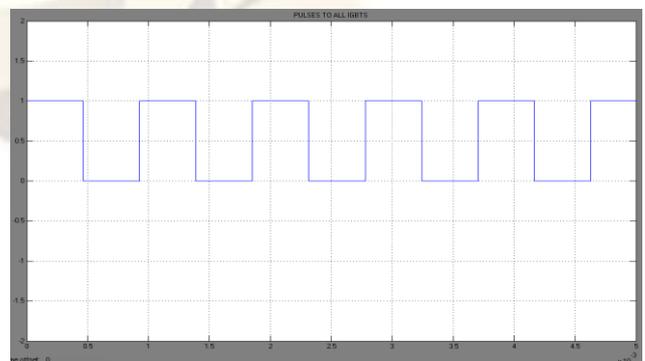


Fig.26 Pulses To IGBTs

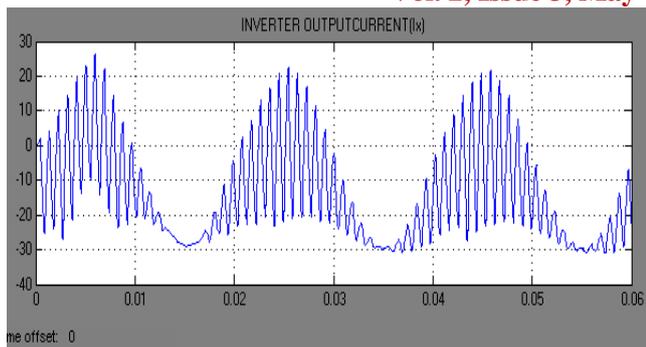


Fig.27 Inverter Output Current ( $I_x$ )

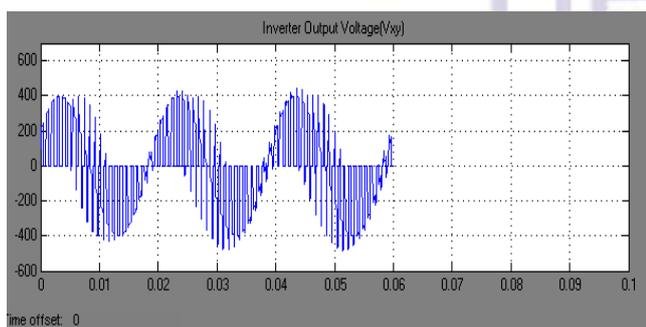


Fig 8.14 Inverter Output Voltage ( $V_{xy}$ )

- [4] K. Gi-Taek and T. A. Lipo, "VSI-PWM rectifier/inverter system with a reduced switch count," *IEEE Trans. Ind. Appl.*, vol. 32, no. 6, pp. 1331–1337, Nov./Dec. 1996.
- [6] A. Bouscayrol, B. Francois, P.
- [5] C. B. Jacobina, I. S. de Freitas, E. R. C. da Silva, A. M. N. Lima, and R. L. A. Ribeiro, "Reduced switch count DC-link AC–AC five-leg converter," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1301–1310, Sep. 2006.
- [6] Modern power electronics and Ac drives by BIMAL.K.BOSE. low price edition.

## VI. CONCLUSION

A novel three phase AC-AC converter using nine-switch SVM converter topology was proposed in this Project. The topology uses only nine IGBT devices for ac to ac conversion through a quasi dc-link circuit. Compared with the conventional back-to-back PWM VSC using 12 switches and the matrix converter that uses 18, the number of switches in the proposed converter is reduced by 33% and 50%, respectively. The proposed converter features sinusoidal inputs and outputs, unity input power factor, and low manufacturing cost. The operating principle of the converter was elaborated, and modulation schemes were developed. Simulation results are shown for proposed converter.

## REFERENCES

- [1] Congwei Liu, Bin Wu, Navid R. Zargari, Dewei (David) Xu and Jiacheng Wang "A Novel three phase three leg AC/AC converter Using Nine IGBTs", *IEEE Trans.* vol.24.N0.5 MAY 2009.
- [2] B. Singh, B. N. Singh, A. Chandra, K. AlHaddad, A. Pandey, and D. P. Kothari, "A review of three-phase improved power quality AC–DC converters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 641–660, Jun. 2004.
- [3] R. L. A. Ribeiro, C. B. Jacobina, E. R. C. da Silva, and A. M. N. Lima, "AC/AC converter with four switch three phase structures," in *Proc. IEEE PESC*, 1996, vol. 1, pp. 134–139.