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Modeling of Switched-Capacitor and Diode-Clamped Multilevel Converter for Induction Motor Application

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Abstract- **The concept of multilevel inverters, introduced about 20 years ago entails performing power conversion in multiple voltage steps to obtain improved power quality, lower switching losses, better electromagnetic compatibility, and higher voltage capability. The benefits are especially clear for medium-voltage drives in industrial applications and are being considered for future naval ship propulsion systems. The novel multilevel circuit topologies are proposed in this paper. They are called multilevel circuit topologies based on switched-capacitor and diode-clamped converters (MCT-BSD). The topology structure and the operation principle, including the working states' transitions of the diode-clamped part, the voltages balancing mechanism of the dc link capacitors, and the pulse width modulated carrier control strategy are given. The switchedcapacitor circuits contribute not only to balancing the voltages of capacitors but also to boosting the output voltage with a certain input dc voltage. Finally a three phase induction motor is driven thorough the proposed converter.**

Keywords- *Induction Motor, Multilevel Inverter, Cascaded H-Bridge*.

I. INTRODUCTION

With the advancement of power electronics and emergence of new multilevel converter topologies, it is possible to work at voltage levels beyond the classic semiconductor limits. The multilevel converters achieve high-voltage switching by means of a series of voltage steps, each of which lies within the ratings of the individual power devices. Among the multilevel Converters [1-4], the cascaded H-bridge topology (CHB) is particularly attractive in high-voltage applications, because it requires the least number of components to synthesize the same number of voltage levels.

Additionally, due to its modular structure, the hardware implementation is rather simple and the maintenance operation is easier than alternative multilevel converters. The multilevel voltage source inverter is recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output [5-11]. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources. The so-called multilevel starts from three levels. As the number of levels reach infinity, the output THD approaches zero.

To balance the voltage of dc link series capacitors, three main approaches have been proposed in the published papers: 1) using separate dc sources [9]; 2) adding some auxiliary balancing circuits [10], [11]; 3) improving the control method by selecting redundant switching states [13], [14]. In some proposed auxiliary balancing circuits, SMPS inductors or series-resonance circuits are adopted to transfer energy between unbalanced capacitors [10], [11]. By auxiliary circuits, the transferred current or power can be controlled accurately, but the additional feedback control strategies are also needed, so the control of these converters becomes more complicated, and converters are less reliable. A four-leg NPC inverter based on the flying capacitor topology is presented in [12]. The fourth leg is added to a traditional three-level inverter to balance the capacitors with its redundant states, which is able to substitute any other legs in the case of failure. But the detection of the voltages of capacitors and the directions of currents through the capacitors are needed. For a higher level converter, the detections become rather complex. For three-phase multilevel inverters with the space vector pulse width modulation (SVPWM) method [13], [14], some redundant states can be selected to balance dc link capacitor voltages without any auxiliary circuits. However, the SVPWM method works only in a low modulation index range, and results in degradation of output voltage quality. On the other hand, the control algorithm complexity of the SVPWM method is increased dramatically with the increase of level number. For a three-level diode-clamped converter, the unbalance problems are solved well by such aforesaid approaches, but for higher level ones, more suitable approaches are still needed.

The multilevel converter topologies based on switched capacitor converter and diode-clamped converter (MCT-BSD) are proposed in this paper. The switched-capacitor circuits are adopted to balance the capacitors under any load conditions, and they also participate in synthesizing the output voltage level. The diode-clamped circuits play the same role as those of the conventional diode-clamped multilevel converter. The proposed topology can not only balance dc link capacitor voltages, but also boost the output voltages with kinds of boosting modes. Furthermore, the number of dc link capacitors is two less than those of the conventional diode-clamped multilevel converter. The validity of the MCT-BSD is verified by simulations on a five-level inverter. The possibility to extend this structure to four, seven, or higher level converters is further discussed. Finally a three phase induction motor is driven thorough the proposed converter.

II. HIGH POWER CONVERTERS CLASSIFICATIONS

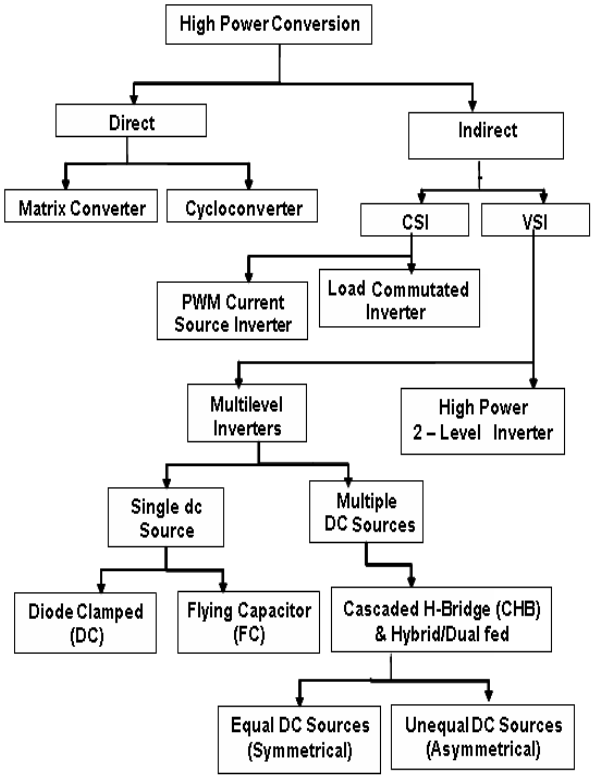

Figure 1 Classification of High power Converters

Fig.1 shows the classification of high power converters. Out of all converters Cascaded bridge configuration is more popular. Cascaded bridge configuration is again classified into 2 types 1) Cascaded Half Bridge 2) Cascaded Full Bridge or Cascaded H-Bridge. In this paper a novel cascaded hybrid H- Bridge topology is proposed for PV application.

A. Diode-Clamped Multilevel Inverter (DCMI)

The diode-clamped multilevel inverter uses capacitors in series to divide up the dc bus voltage into a set of voltage levels. To produce m levels of the phase voltage, an m-level diode-clamp inverter needs m-1 capacitors on the dc bus. A single-phase five-level diode-clamped inverter, which can produce a nine-level phase to phase voltage waveform, is shown in Fig. 2.

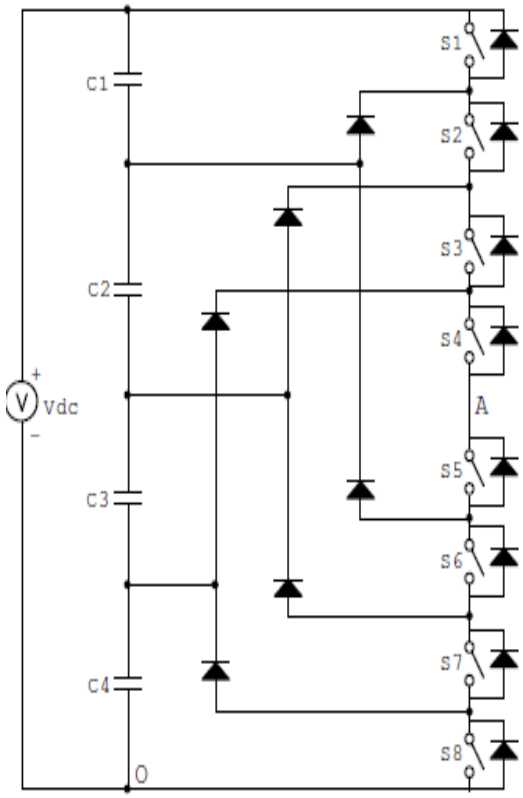

Figure 2 A single-phase five-level diode-clamped inverter.

The dc bus consists of four capacitors, i.e., C_1, C_2, C_3, and C_4. For a dc bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level, $V_{dc}/4$, through clamping diodes. DCMI output voltage synthesis is relatively straightforward. To explain how the staircase voltage is synthesized, point O is considered as the output phase voltage reference point. Using the five-level inverter shown in Fig. 2, there are five switch combinations to generate five level voltages across A and O.

B. Flying-Capacitor Multilevel Inverter (FCMI)

Probably the most important multilevel topology to appear recently is the flying capacitor inverter, or imbricated cells multilevel inverter, proposed by Meynard and Foch. A FCMI shown in Fig. 3 uses a ladder structure of dc side capacitors where the voltage on each capacitor differs from that of the next capacitor. To generate m-level staircase output voltage, m-1 capacitors in the dc bus are

needed. Each phase-leg has an identical structure. The size of the voltage increment between two capacitors determines the size of the voltage levels in the output waveform.

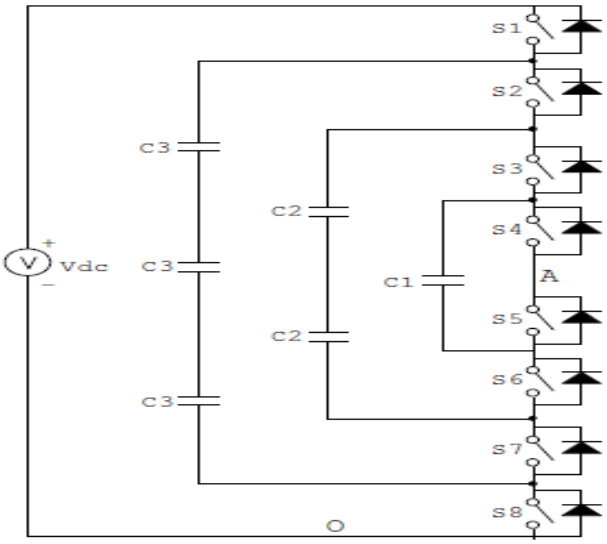

Figure 3 A single-phase five-level flying-capacitor inverter.

Here the switch pair-capacitor 'cell' is isolated and inserted within a similar cell – hence the term imbricated cells inverter. This inner pair of switches and their associated capacitor now 'flies' as the outer pair of devices switch. The combination of conducting switches and capacitors ensures that the voltage across any blocking switch is always well defined.

C. Cascaded-Inverters with Separated DC Sources

The last structure introduced here is a multilevel inverter, which uses cascaded inverters with separate dc sources (SDCSs). The general function of this multilevel inverter is the same as that of the other two previous inverters. The multilevel inverter using cascaded-inverter with SDCSs synthesizes a desired voltage from several independent sources of dc voltages, which may be obtained from batteries, fuel cells, or solar cells. This configuration recently becomes very popular in ac power supply and adjustable speed drive applications. This new inverter can avoid extra clamping diodes or voltage balancing capacitors. A single-phase two-cell series configuration of such an inverter is shown in Fig 4.

Each SDCS is associated with a single-phase full-bridge inverter. The ac terminal voltages of different level inverters are connected in series. By different combinations of the four switches, S_1-S_4, each inverter level can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$, and zero. The ac output of each of the different level of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. Note that the number of output phase voltage levels is defined in different way from those of two previous inverters. In this topology, the number of output phase voltage levels is defined by m=2s+1, where s is the number of dc sources.

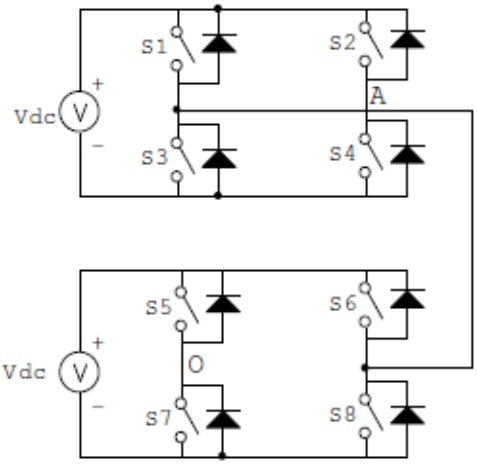

Figure 4 Single-phase structure of a two-cell cascaded inverter.

III. DYNAMIC MODEL OF INDUCTION MOTOR

The induction machine d-q or dynamic equivalent circuit is shown in Fig. 5 and 6. One of the most popular induction motor models derived from this equivalent circuit is Krause's model detailed in [5]. According to his model, the modeling equations in flux linkage form are as follows:

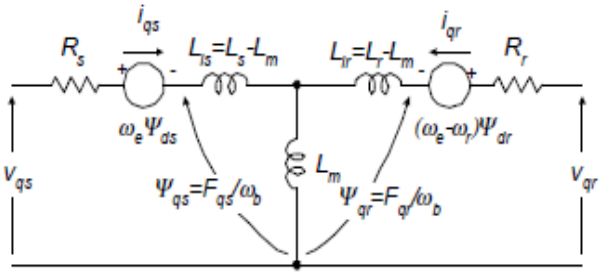

Fig. 5 Dynamic q-axis model

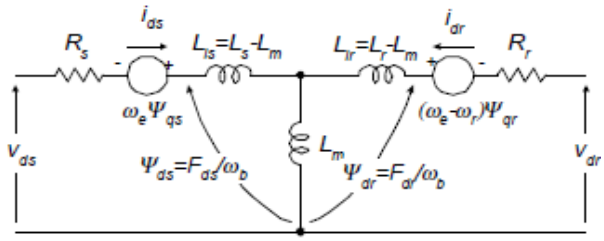

Fig. 6 Dynamic d-axis model

$$\frac{dF_{qs}}{dt} = \omega_b\left[v_{qs} - \frac{\omega_e}{\omega_b}F_{ds} + \frac{R_s}{x_{ls}}\left(F_{mq} + F_{qs}\right)\right] \quad (1)$$

$$\frac{dF_{ds}}{dt} = \omega_b\left[v_{ds} + \frac{\omega_e}{\omega_b}F_{qs} + \frac{R_s}{x_{ls}}\left(F_{md} + F_{ds}\right)\right] \quad (2)$$

$$\frac{dF_{qr}}{dt} = \omega_b\left[v_{qr} - \frac{(\omega_e - \omega_r)}{\omega_b}F_{dr} + \frac{R_r}{x_{lr}}\left(F_{mq} - F_{qr}\right)\right] \quad (3)$$

$$\frac{dF_{dr}}{dt} = \omega_b\left[v_{dr} + \frac{(\omega_e - \omega_r)}{\omega_b}F_{qr} + \frac{R_r}{x_{lr}}\left(F_{md} - F_{dr}\right)\right] \quad (4)$$

$$F_{mq} = x^*_{ml}\left[\frac{F_{qs}}{x_{ls}} + \frac{F_{qr}}{x_{lr}}\right] \quad (5)$$

$$F_{md} = x^*_{ml}\left[\frac{F_{ds}}{x_{ls}} + \frac{F_{dr}}{x_{lr}}\right] \quad (6)$$

$$i_{qs} = \frac{1}{x_{ls}}\left(F_{qs} - F_{mq}\right) \quad (7)$$

III. MATLAB/SIMULINK MODELING AND SIMULATION RESULTS

Fig. 7 Shows the Matlab/Simulink switched capacitor and diode clamped multilevel inveter.

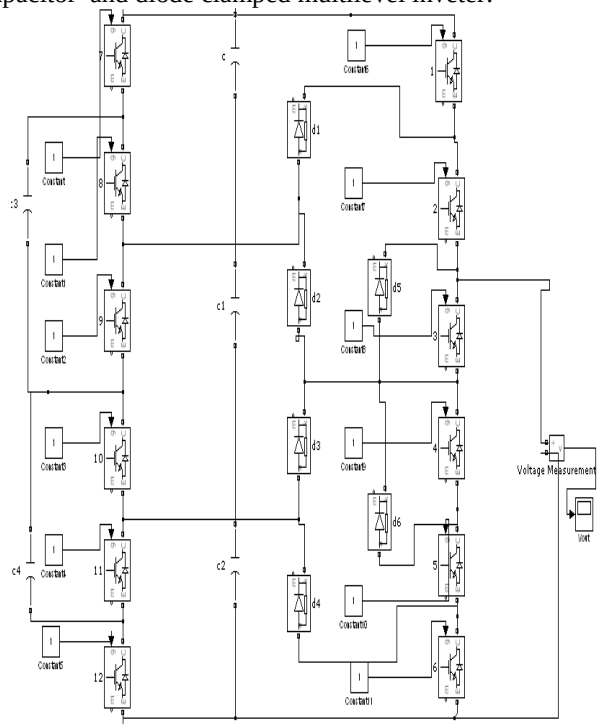

Figure. 7 Matlab/Simulink model

Fig. 8 shows the level shifted PWM signal of the proposed converter. Since converter is designed for five levels so it has four carriers.

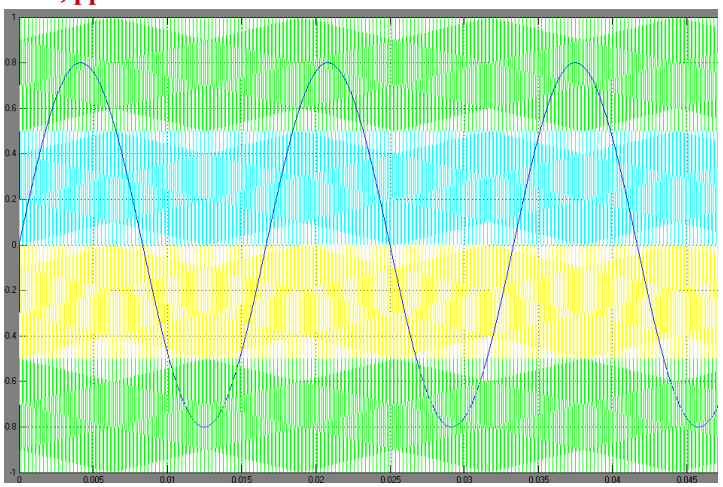

Figure. 8 PWM signals

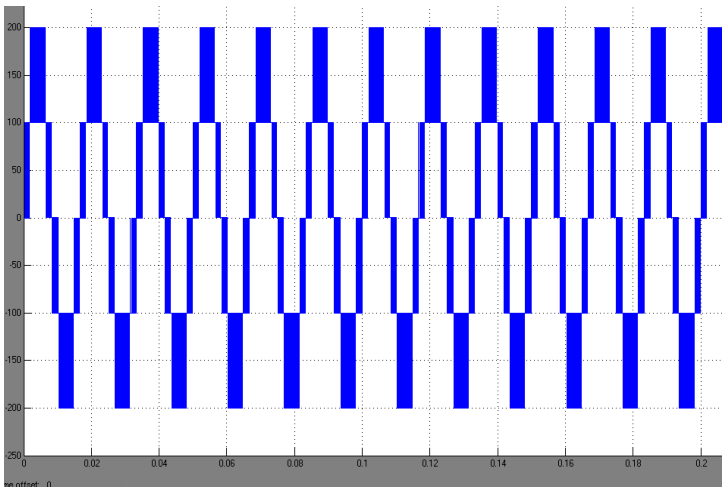

Figure 9 Five level output without filter

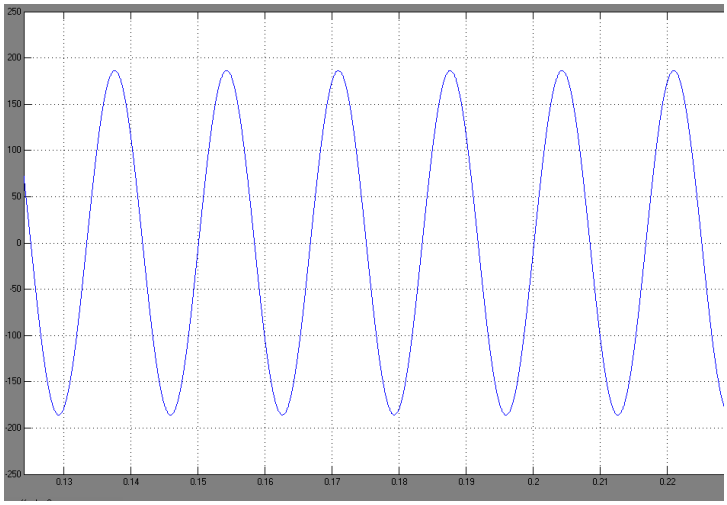

Figure 10 Output with filter

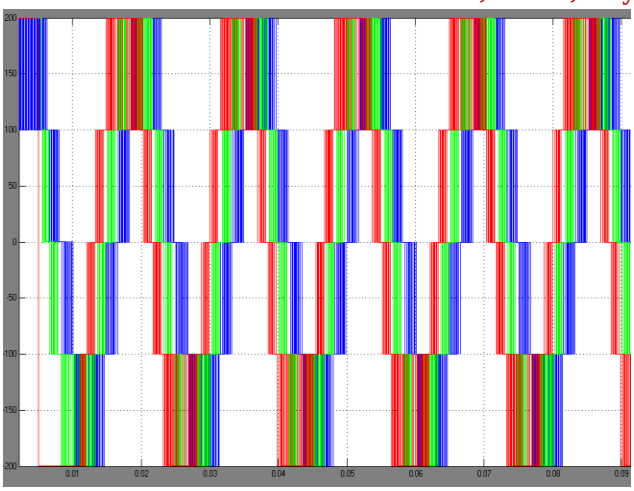

Figure 11 Three phase output

This waveform represents the output voltage of the three phase multilevel inverter.

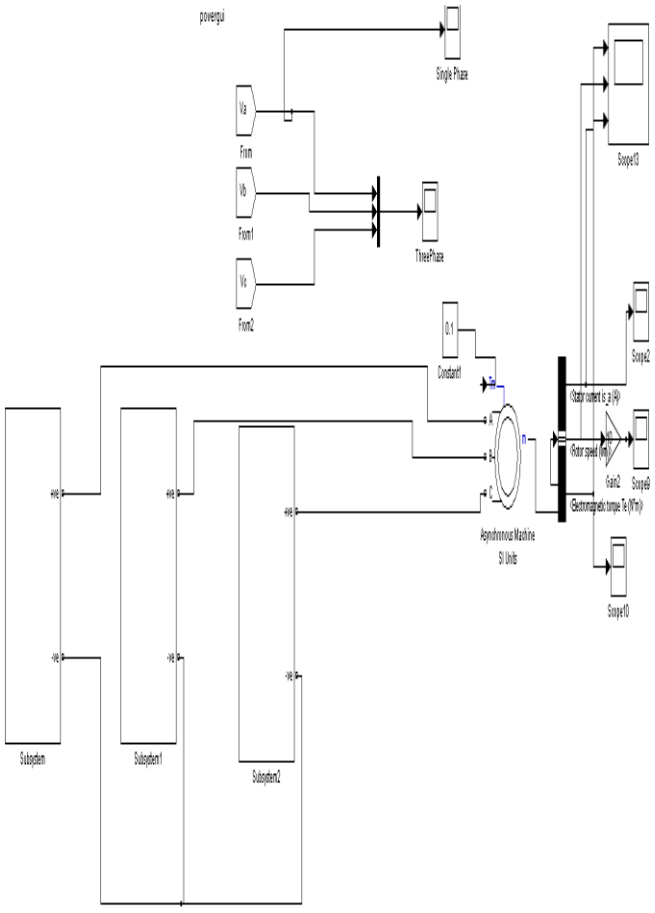

Figure 12 Three phase converter with Induction Motor Drive

Fig. 12 shows the Matlab/Simulink model of three phase converter with induction motor drive.

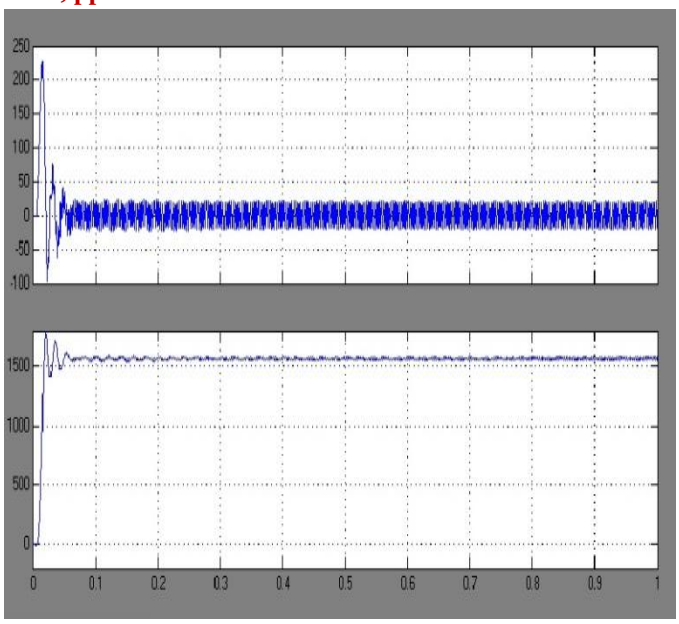

Figure.13 Electromagnetic Torque and Speed curves of SQCIM

The first waveform represents the Electromagnetic Torque and rotor speed characteristics of the Squirrel cage Induction motor

IV. CONCLUSION

The novel multilevel topologies are proposed in this paper, and they consist of a switched-capacitor converter and a diodeclamped converter. The structure and the operation principle of this topology are introduced. The switched-capacitor circuits are applied to balance the voltage of dc link capacitors and flying capacitors with any load conditions, as well as participate in synthesizing the output voltage levels. Both advantages of the switched-capacitor and the diode-clamped circuits are brought into full play in the MCT-BSD by the combination of the two circuits. Not only this new topology balances dc link capacitors, but also it can step up the output voltage with kinds of boosting modes, which will contribute to lessening the turns ratio of the input transformer, even to cutting out it. Compared to the other switched-capacitor topology, the less switching devices and dc link capacitors are needed in the MCT-BSD. Finally a Matlab/Simulink based model is developed and simulation results are presented.

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