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Choosing Appropriate Utilization Factor and Metal Layer Numbers for an Efficient Floor Plan in VLSI Physical Design

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ABSTRACT
In this paper the effects of choosing a Utilization Factor on total wire length, top metal layer length, congestion and DRC violations have been explained. In addition, how the number of metals used to route between the standard cells will affect total wire length, number of vias, congestion and number of DRC (Design Rule Constraints) violations has been studied. It's observed that a Utilization Factor of 0.5 to 0.6 is good when PG (Power and Ground) planning is done on lower metal layers and a Utilization factor of 0.6 to 0.7 is good when PG planning is done on higher metal layers. Also a minimum of 3 metal layers must be used to make the design routable.

Keywords – **Congestion, Floor Plan, PG planning, Place and Route, Utilization Factor.**

I. INTRODUCTION

In VLSI Physical Design, floor planning is one of first and most fundamental step. The rest of the physical design, mainly placement of standard cells, congestion and timing are as good as our floor plan [1]. An important step in floor planning is to specify appropriate core area to place macros and standard cells and also to decide appropriate metal layers to do Power and Ground planning. In general floor plan can be specified in terms of (1) Aspect ratio (height x width) and dimensions of the core (2) Utilization Factor (UF) (3) In terms of die area.

In this paper, how to decide the best utilization factor for a design, which metals are generally preferred for Power and Ground (PG) planning and situations where PG planning is done on lower metal layers, but still making the design routable are discussed. Here a timing driven placement of standard cells is done and a 6 layer metal process is used.

The experiments in this paper are mainly classified into two phases: **Phase 1** - Lower metal layers (M1 and M2) used for PG planning. **Phase 2** – Top metal layers (M5 and M6) used for PG planning. Here all the simulations are done on Cadence ® Soc-Encounter RTL-to-GDS II system, Version 9.1.

II. PHASE 1: USING LOWER METAL LAYERS

In this phase we use lower metal layers such as Metal 1 (M1) and Metal 2 (M2) for Power and Ground planning. For core power rings (VDD and VSS) we use M1 and M2, where the top and bottom rings are laid on M1 (Horizontal Layer) and the left and right rings are laid on M2 (Vertical Layer) with a width of 4.8 microns and a spacing of 1.8 microns each. Vertical power stripes are laid on M2 with a width of 4.8 microns, spacing of 1.8 microns and a set-to-set distance of 33 microns. Special route for follow pins i.e. to connect VDD and VSS pins of all the standard cells is done on M1. Fig.1 shows the PG planning of phase 1 for a particular Utilization Factor.

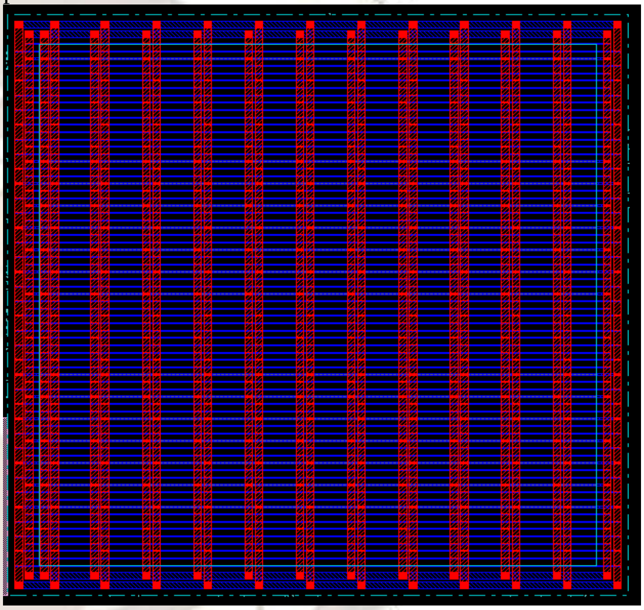

Fig. 1. Chip with PG planning done on M1 and M2 layers

III. PHASE 2: USING HIGHER METAL LAYERS

In this phase we use higher metal layers such as Metal 5 (M5) and Metal 6 (M6) for Power and Ground planning. For core power rings (VDD and VSS) we use M5 and M6, where the top and bottom rings are laid on M5 (Horizontal Layer) and the left and right rings are laid on M6 (Vertical Layer) with a width of 4.8 microns and a spacing of 1.8 microns each. Vertical power stripes are laid on M6 with a width of 4.8 microns, spacing of 1.8 microns and a set-to-set distance of 33 microns. Special route for follow pins is done on M1. Fig. 2 shows the PG planning of phase 2 for a particular Utilization Factor. Fig. 3 shows a place and routed chip with filler cells added.

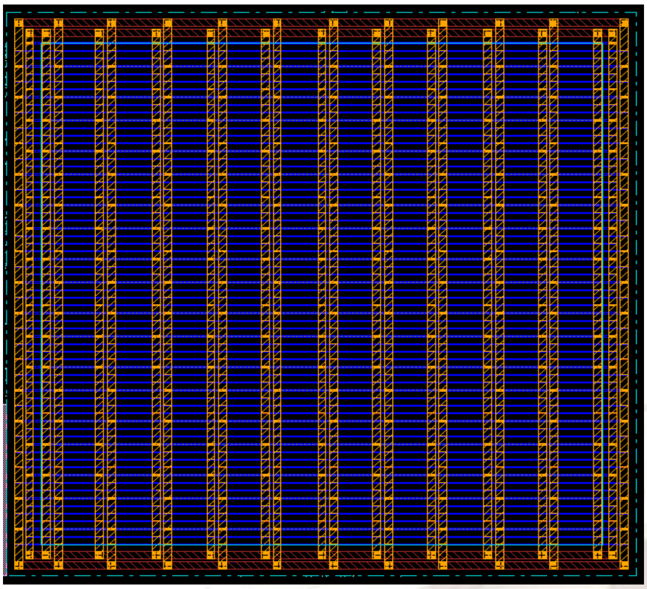

Fig.2. Chip with PG planning done on M5 and M6 layers

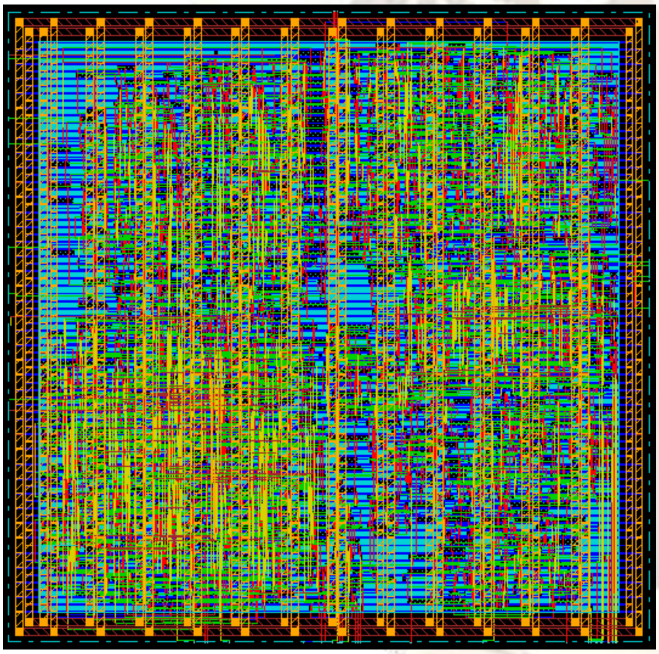

Fig.3. Place and Routed chip with filler cells added

IV. EXPERIMENTAL RESULTS

All the experiments were performed on Cadence® Soc-Encounter RTL-to-GDS II system. For each phase, three parameters were observed: (1) Utilization Factor versus Total wire length with number of metal layers fixed at 5. (2) Utilization Factor versus Metal 6 length (Top most metal layer) with all the metals used (M1 to M6 metal layers). (3) Number of Metal layers versus Total wire length with Utilization factor fixed at 0.5. Also for each of the above three parameters, Number of vias, Number of DRC violations, Congestion and Time to do Place and Route were also studied.

A. UTILIZATION FACTOR VERSUS TOTAL WIRE LENGTH

Utilization factor (UF) is defined as

$$UF = \frac{Area\ of\ the\ Standard\ cells}{Total\ Area\ Allocated} \qquad (1)$$

Here the UF is varied from 0.8 to 0.3 and the total wire length used for each value is tabulated. When we say the UF is 0.8, it means we allocate an area of $\frac{1}{0.8}$ times of the standard cells area, for the tool to place macros, standard cells and do routing between them. Here the number of metal layers used is fixed to 5. Fig. 4 shows the variation of total wire length used for routing for different values of UF. Fig. 5 and Fig. 6 show the distribution of total wire length for each individual metal.

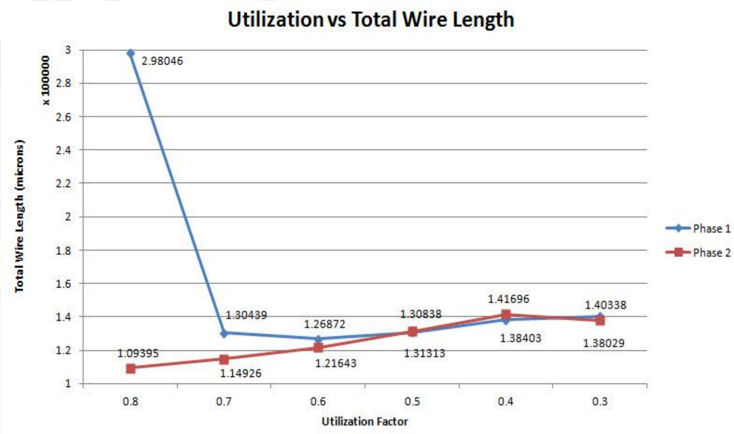

Fig.4. Utilization vs. Total wire length

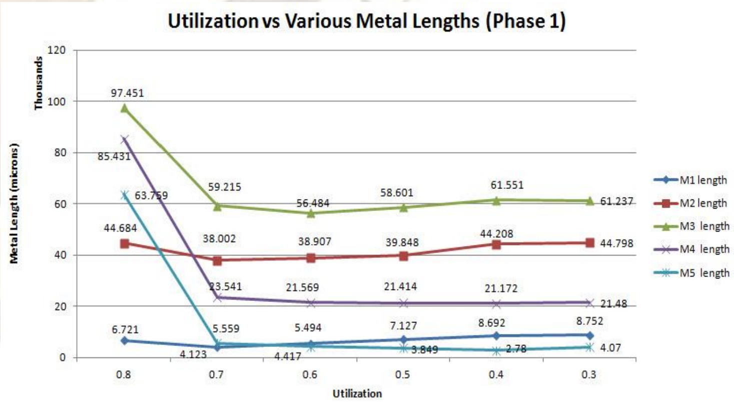

Fig.5. Utilization vs. Various metal lengths (Phase 1)

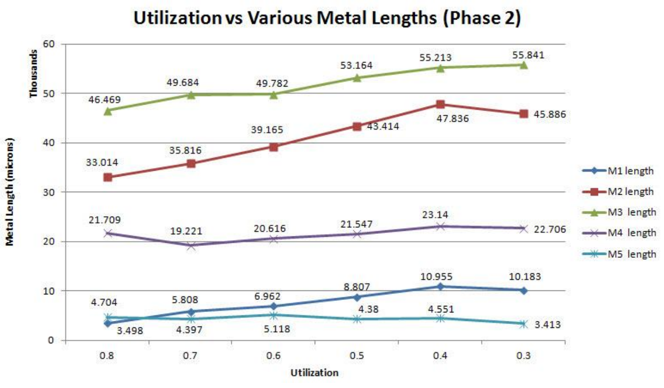

Fig.6. Utilization vs. Various metal lengths (Phase 2)

From Fig. 4 we observe that for Phase 1 for a UF = 0.8 the wire length is the maximum, gradually decreases till UF = 0.6, increases till 0.4 and then again starts decreasing. This is because in Phase 1 the PG planning is done on M1 and M2 layers and for UF = 0.8 the area allocated is less, so in order to avoid shorts with M1 and M2, minimum amount of routing is done on M1 and M2 (see in Fig. 5). Also as the cells are placed very close to each other and in order to avoid minimum spacing violations, shorts (DRC violations) between the nets, the tool does a complex, long de-tour routing on M3, M4 and M5 with a preference to M3 (Optimal Layer). As the UF decreases to 0.6 (Optimal distance), the area to place cells increases therefore the tool starts routing the cells with normal routes. As the UF increases to 0.4, the standard cells are separated with large distances (more than the optimal distance), so they are routed with longer routes and care is taken to avoid maximum DRC violations for which top layers are used. For UF of 0.3 and beyond, even though the tool has a lot of space to place the cells and route between them, it prefers not to do so, to meet timing (as it is a timing driven placement).

In Phase 2 (from Fig. 2 and Fig. 6) as the PG planning is done on M5 and M6, the tool does majority of the routing on lower layers and as the routing is done on lower layers, complex de-tour routing is not needed between the cells. As UF increases to 0.4, the separation between cells also increases, therefore longer routes are done (on M2 and M3). For UF of 0.3 and beyond, even though the tool has a lot of space to place the cells and route between them, it prefers not to do so, to meet timing.

From Fig. 7 we observe that for Phase 1 and UF = 0.8 the total number of vias are very large in number than its corresponding value for Phase 2, as relatively large number of vias are laid on M3 (via from M3 to M4) and M4 (via from M4 to M5), in order to avoid DRC violations with M1 (Special route nets) and M2 (vertical power stripe nets). As UF decreases, the number of vias almost become constant as now the space to place the standard cells gradually increases, as a result complex de-tour routing is avoided and same layer routing is preferred. From Fig. 8 and Fig. 9 we see that maximum numbers of vias are laid on M1 and M2, this shows that the tool gives more priority to lower layers for routing.

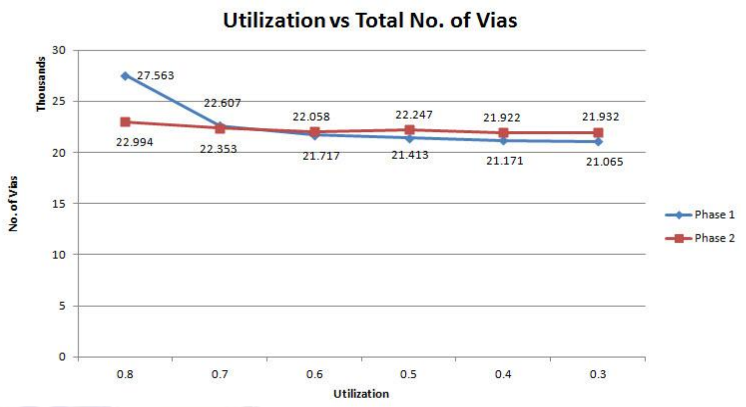

Fig.7. Utilization vs. Total No. of vias

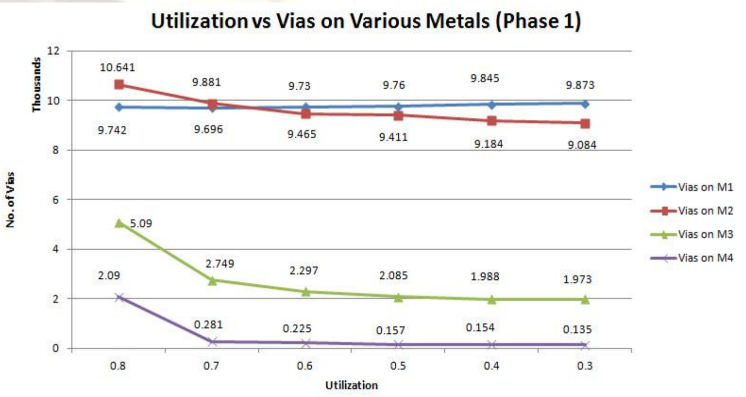

Fig.8. Utilization vs. Vias on various metals (Phase 1)

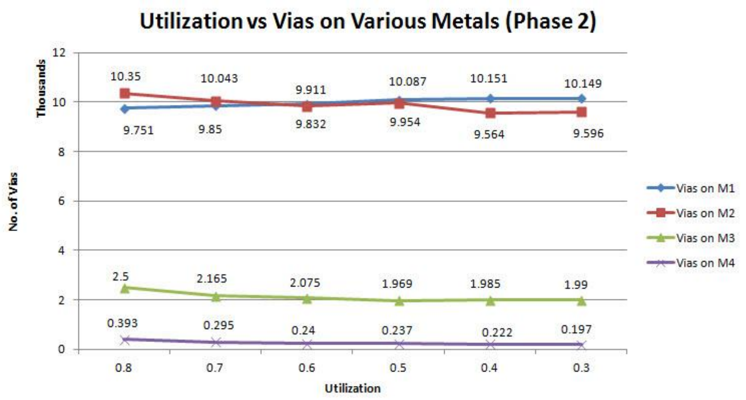

Fig.9. Utilization vs. Vias on various metals (Phase 2)

From Fig. 10 and Fig. 11 we observe that there are maximum numbers of DRC violations in Phase 1 and none in Phase 2. It's because as the PG planning is done on lower metal layers (M1 and M2) in Phase 1, there are a lot of minimum spacing violations and shorts, where as in Phase 2 as the PG planning is done on higher layers no such problems exist. Also in Phase 1 as the UF decreases, we have more space to place and route the standard cells, therefore lesser the violations.

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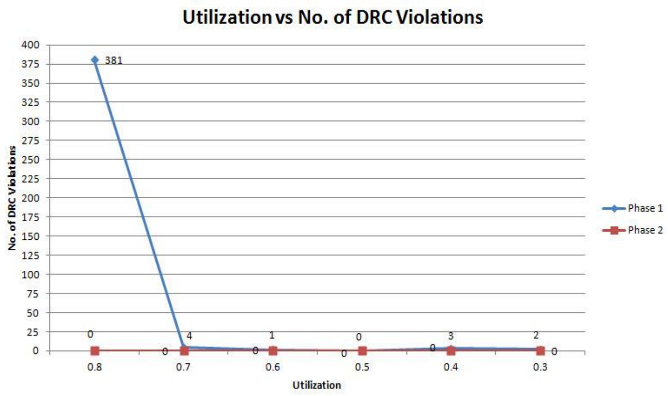

Fig.10. Utilization vs. No. of DRC violations

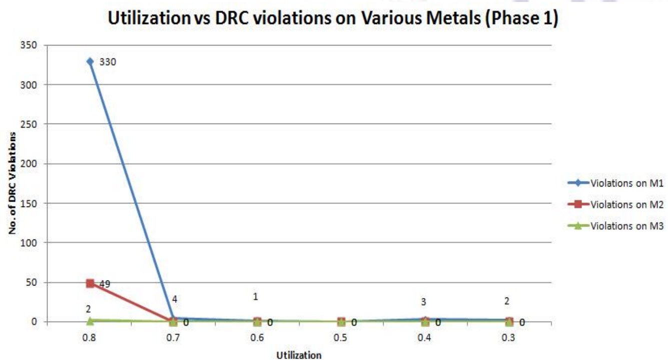

Fig.11. Utilization vs. DRC violations on metals (Phase 1)

Congestion is defined as the number of Horizontal (H) and Vertical (V) tracks that are over/under utilized in a G cell (Global cell). Worst layer G cell over congestion gives information regarding the worst percentage over congestion among all the G cells. Fig. 12 and Fig. 13 show that as the UF decreases, congestion decreases as we have more space i.e. more G cells to route. After UF = 0.3 the congestion slightly increases because, even though the tool has a lot of space to place the cells and route between them, it prefers not to do so, to meet timing. Also Phase 1 has more congestion than Phase 2 because the lower layer metal tracks are occupied by M2 for PG vertical stripes.

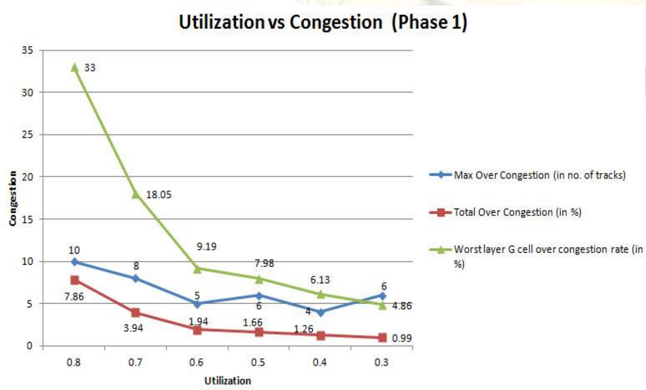

Fig.12. Utilization vs. Congestion (Phase 1)

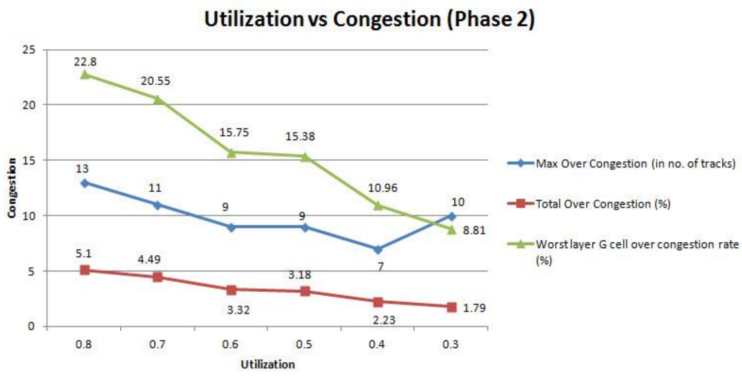

Fig.13. Utilization vs. Congestion (Phase 2)

From Fig. 14 we can see that the time to route between the cells is very large when compared to time to place the standard cells, this is because in Phase 1 the tool does complex de-tour routing in order to minimize the DRC violations. But in Phase 2 (Fig. 15) as PG planning is done on higher metal layers and as there are no DRC violations the tool can place and route the standard cells very easily.

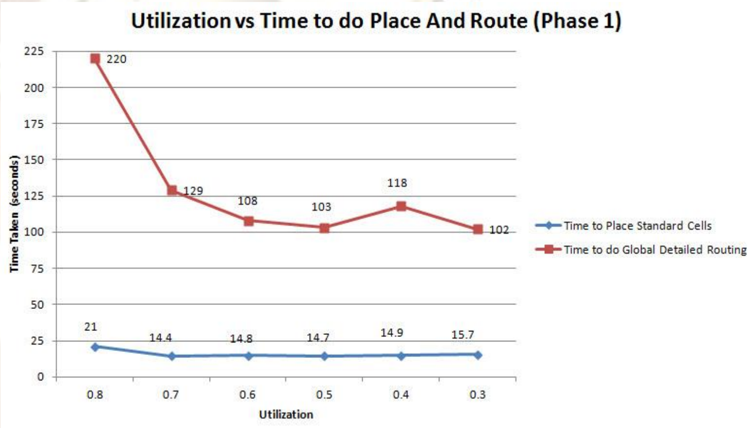

Fig.14. Utilization vs. Time to do PNR (Phase 1)

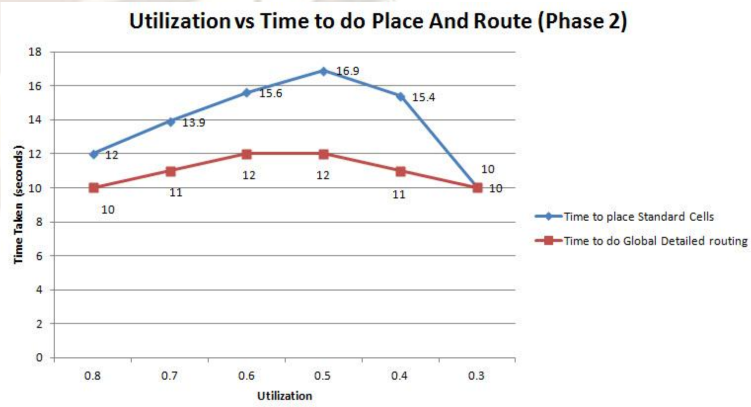

Fig.15. Utilization vs. Time to do PNR (Phase 2)

B. UTILIZATION FACTOR VERSUS METAL 6 LENGTH

Here we use all 6 metal layers to do routing. From Fig. 16, it is observed that as the Utilization Factor decreases i.e. as the available area increases the amount of metal 6 used for routing decreases in both Phase 1 and Phase 2. By this we can say that the tool uses higher layers for routing only when required (as in Phase 1 with UF = 0.8 to avoid DRC violations higher layers are used) and prefers the lower and middle layers for routing between the standard cells. The same can be observed from Fig. 17 and Fig. 18. From the later two figures it is also observed that M1 is sparsely used for routing as it is mostly used within the standard cells.

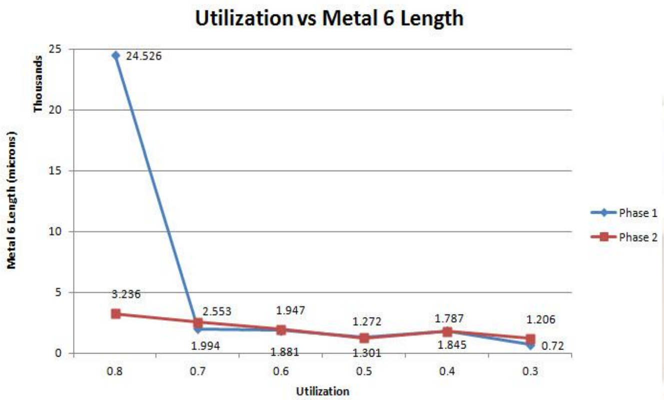

Fig.16. Utilization vs. Metal 6 length

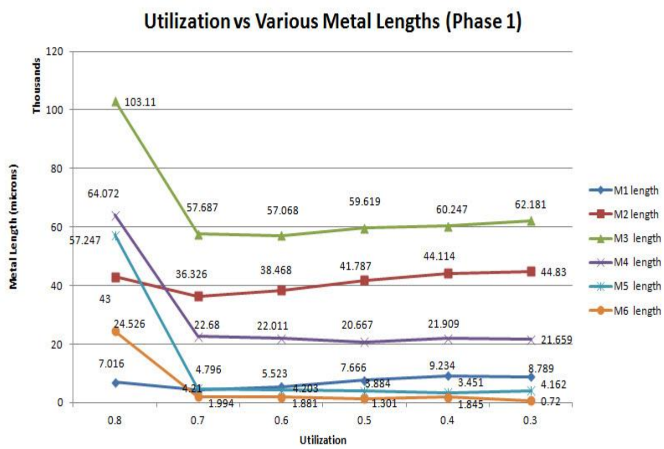

Fig.17. Utilization vs. Various metal lengths (Phase 1)

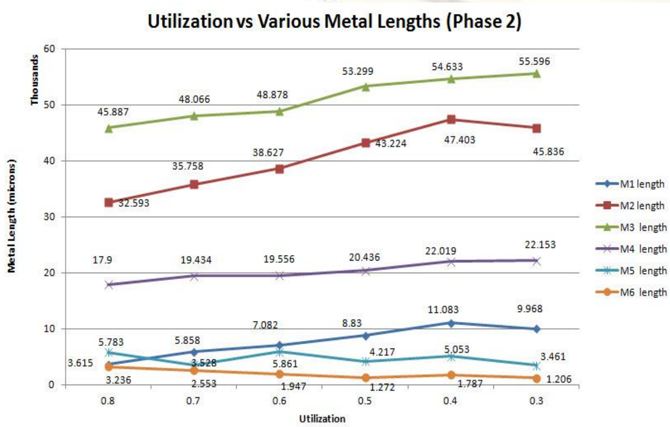

Fig.18. Utilization vs. Various metal lengths (Phase 2)

C. TOTAL WIRE LENGTH VERSUS NO. OF METAL LAYERS USED

From Fig. 19 we can infer that by using fewer number of metals to route between the standard cells spread across the core area, the tool has to do complex de-tour routing i.e. use long nets, to avoid DRC violations. But when more number of metals are at the tools disposal, it can route between far away cells by switching to higher layers instead of a long, same metal layer routing. In this way it can also avoid DRC violations. The same can be observed from Fig. 20 and Fig. 21.

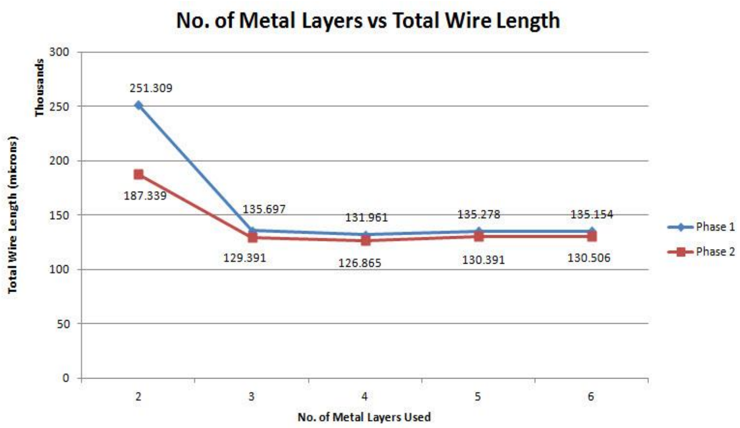

Fig.19. No. of metal layers vs. Total wire length

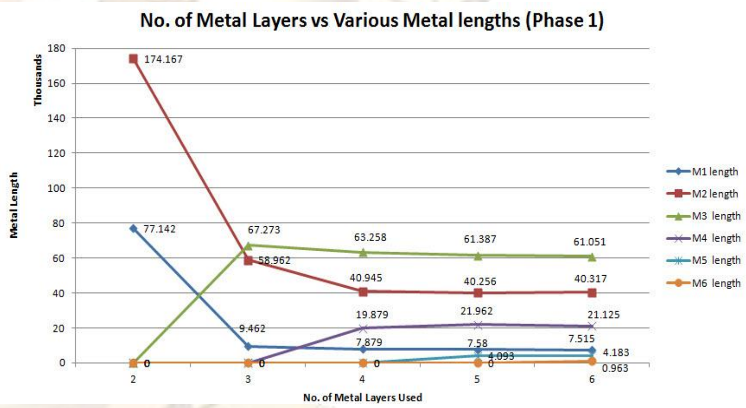

Fig.20. No. of metal layers vs. Metal lengths (Phase 1)

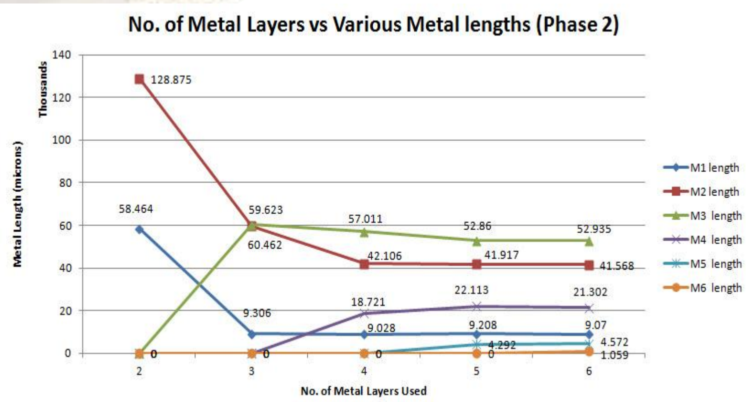

Fig.21. No. of metal layers vs. Metal lengths (Phase 2)

From Fig. 22, Fig. 23 and Fig. 24 we can observe that when fewer numbers of metals are used the tool tries to move to the highest possible metal layer to avoid DRC violations for each and every route, therefore we see more number of vias when we use only 2 metal layers. But as the number of metal layers increase the tool tries to balance between higher metal layer switching and same metal layer routing, therefore the number of vias decrease. Also when more number of layers are available for the tool, it tries to use them, (but to the minimum extent possible) therefore the via count increases.

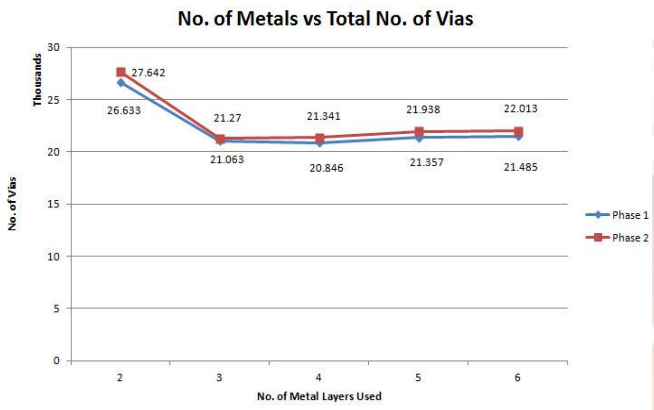

Fig.22. No. of metals vs. Total no. of vias

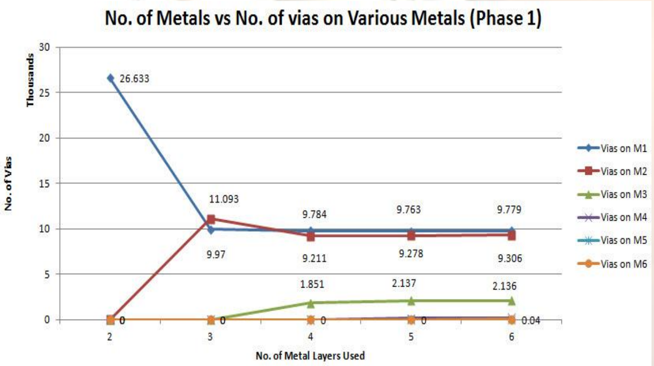

Fig.23. No. of metals vs. vias on various metals (Phase 1)

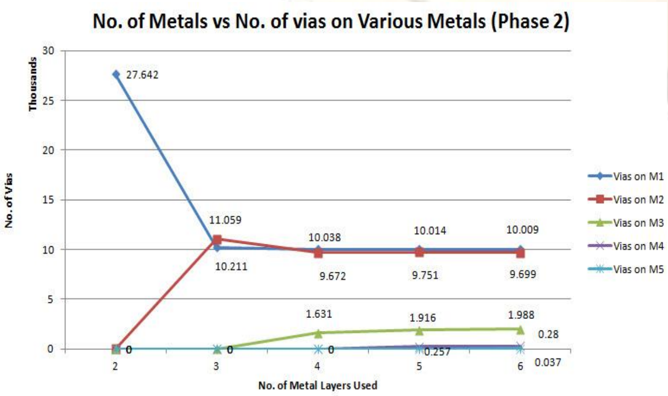

Fig.24. No. of metals vs. vias on various metals (Phase 2)

From Fig. 25 it can be observed that with fewer number of metals available for the tool it's not possible for it to avoid DRC violations, but as the number of metals increase it has the option of moving to higher layers and avoiding DRC violations, therefore the DRC violations decrease with an increase in the number of metal layers used for routing.

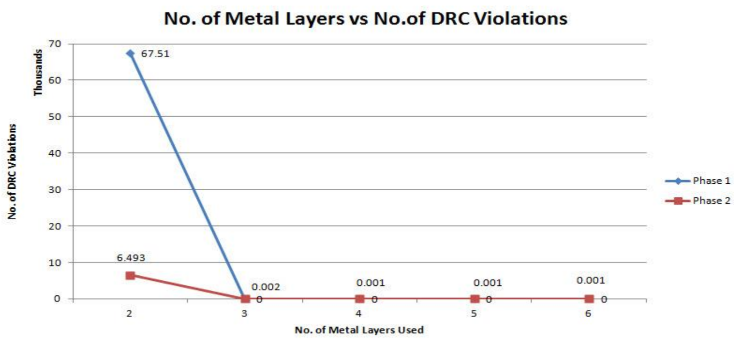

Fig.25. No. of metal layers vs. No. of DRC violations

From Fig. 26 and Fig. 27 it can be observed that with fewer numbers of metals the tool has less number of routing tracks to route between all the cells, therefore more is the congestion and as the number of metal layers increase, the number of available routing tracks available also increase, as a result the congestion decreases. (Note: For a 2 metal layer process each G cell has equal number of M1 and M2 routing tracks, for a 3 metal layer process each G cell has equal number of M1, M2 and M3 routing tracks and so on..).

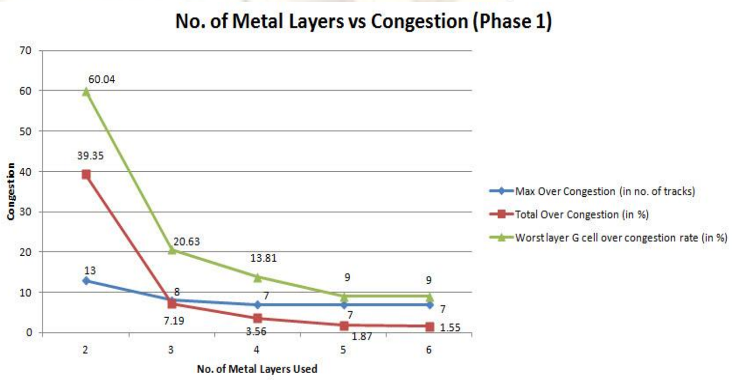

Fig.26. No. of metals vs. Congestion (Phase 1)

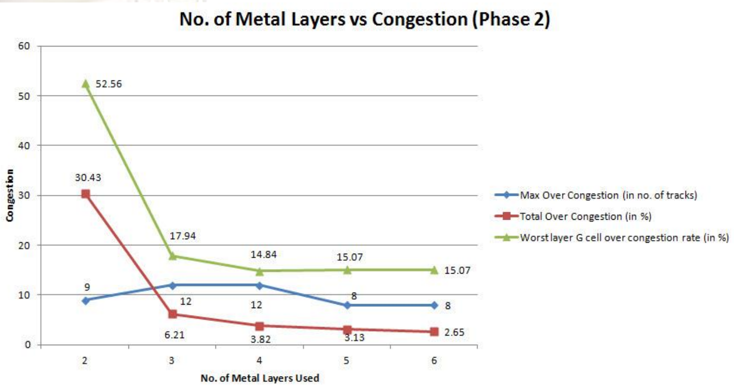

Fig.27. No. of metals vs. Congestion (Phase 2)

From Fig. 28 and Fig. 29 it can be observed that as placement of standard cells is independent of the number of metal layers used for routing, time taken to place the cells is almost constant in Phase 1 and Phase2. In both the phases when two metals are used for routing, time taken is more as complex de-tour routing is done to minimize DRC violations. In case of detailed routing for Phase 1 the time taken to do routing increases with an increase in the number of metal layers. The reason for this is, in order to avoid DRC violations with M2 power stripes an optimal usage of M2 and M3 metal layers must be done, which results in more time. In case of Phase 2 as PG planning is done on higher layers, the time to route between the cells decreases. In both phases the sudden decrease in the time taken to route using 5 metal layers is strange and will be explored in a later paper.

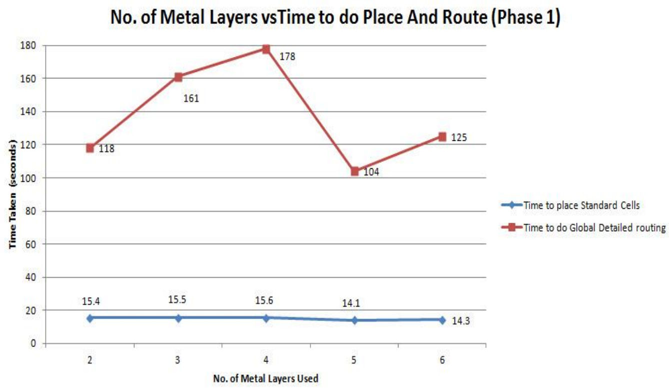

Fig.28. No. of metal layers vs. Time to do PNR (Phase 1)

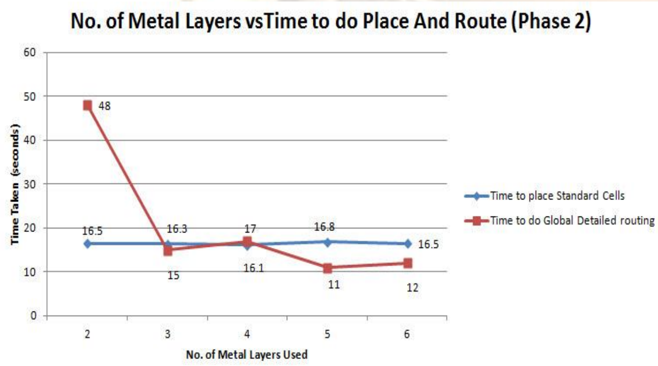

Fig.29. No. of metal layers vs. Time to do PNR (Phase 2)

V. Conclusion

Choosing an appropriate Utilization Factor, PG planning with appropriate metals and sufficient number of metals to route between the standard cells is very important. Therefore when PG planning is done on lower metal layers a UF of 0.5 to 0.6 is good and when PG planning is done on higher metal layers a UF of 0.6 to 0.7 is good. To route the standard cells a minimum of 3 metal layers must be used. Therefore in order to minimize congestion, place and route time, increase the yield and decrease the cost per unit chip, a UF of 0.7 and a 5 layer metal process is advised.

References

[1] Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, *Digital Integrated Circuits*, 2nd Edition (Prentice Hall, ISBN 978-81-203-2257-8).

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