

## Stress Analysis and Temperature Impact of Negative Bias Temperature Instability (NBTI) on a CMOS inverter circuit

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### ABSTRACT-

Negative Bias Temperature Instability (NBTI) has become an important reliability concern for ultra-scaled Silicon IC technology with significant implications for both analog and digital circuit design. As the Integrated Circuits (IC) density keeps on increasing with the scaling of CMOS devices in each successive technology generation, stress analysis or reliability concerns mainly Negative Bias Temperature Instability (NBTI) becomes a major challenge. Stress Analysis becomes important for any digital circuit as it predicts the life time of the circuit in terms of the degradation of device parameters. NBTI degrades the performance of a PMOS transistor under a negative gate stress. The after effects of NBTI include: (a) threshold voltage increase of PMOS transistor, (b) drain current degradation, and (c) speed degradation. Elevated temperature and the negative gate stress play an important role in degradation of Gate Oxide. Before any circuit design Stress Analysis becomes important for any device in order to get the complete performance of the circuit. Negative bias temperature instability (NBTI) has become the dominant reliability concern for nanoscale PMOS transistors. In this paper basically we have studied the Stress Analysis and the impact of temperature of NBTI on a CMOS inverter circuit.

**Keywords** - EZwave, Inverter, NBTI, Reliability, Stress, Threshold Voltage, Temperature

### I. INTRODUCTION

The sustained growth in Integrated Circuits (IC) density and speed has been accomplished by CMOS scaling. The scaling reduces gate oxide thickness in each successive technology generation. Industrial data reveal that as oxide thickness reaches 4nm, reliability concerns (especially NBTI) becomes a major challenge [1, 2]. NBTI occurs under negative gate voltage (e.g.,  $V_{gs} = -V_{DD}$ ) and is measured as an increase in the magnitude of threshold voltage. It mostly affects the PMOS transistor [3] and degrades the device drive current, circuit speed, noise margin, and other factors. The threshold voltage change caused by NBTI for the PMOS transistor has become the dominant factor to limit the life time, which is much shorter than that defined by hot-carrier induced degradation (HCI) of the NMOS transistor. NBTI degradation in

MOSFETs is explained by the reaction-diffusion model described in next section.

Stress analysis involves, studying the NBTI effect on a PMOS transistor when it is conducting. It is well known that NBTI impacts PMOS transistors during circuit operation, and the degradation occurs when PMOS transistor is in a conducting state. So, accurate NBTI degradation analysis requires analysis of logic states. Degradation of specific PMOS transistor depends on part of lifetime, in which this transistor is under stress, in other words, on stress probability. The NBTI occurs when the PMOS transistor is negative biased, in particular at elevated temperature. For a CMOS inverter circuit as shown below figure 1 represents the stress and relaxation phase when gate voltage is zero ( $V_G=0$ ) and  $V_{DD}$  ( $V_G=V_{DD}$ ) respectively.

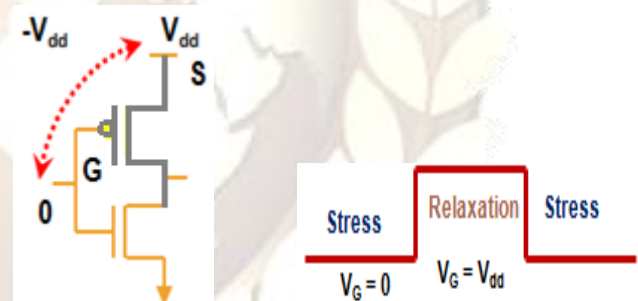


Figure 1: Pulse showing stress and relaxation phase of a PMOS

For a PMOS transistor, there are two phases of NBTI, depending on its bias condition. These two phases are illustrated in Fig. 1, assuming the substrate is biased at  $V_{DD}$ . In Phase I, when  $V_g=0$  (i.e.,  $V_{gs} = -V_{DD}$ ), positive interface traps are accumulating over the stress time with H diffusing towards the gate. This phase is usually referred as “stress” or “static NBTI”. In Phase II, when  $V_g=V_{DD}$  (i.e.,  $V_{gs}=0$ ), holes are not present in the channel and thus, no new interface traps are generated; instead, H diffuses back and anneals the broken Si-H. As a result, the number of interface traps is reduced during this stage and the NBTI degradation is recovered. Phase II is usually referred as “recovery” and has a significant impact on the estimation of NBTI during the dynamic switching. Static NBTI (i.e. under constant voltage (DC) stress condition) leads to a severe threshold voltage ( $V_T$ ) shifts, while the mechanism was described in [4]. However, because of associated recovery phenomena the dynamic NBTI (i.e., under AC stress), a less

severe parameters' shifts over long time compared with that under DC stress condition. The following figure 2 shows that the final threshold voltage ( $V_T$ ) shift is the combined effect of Stress and Recovery Phase.

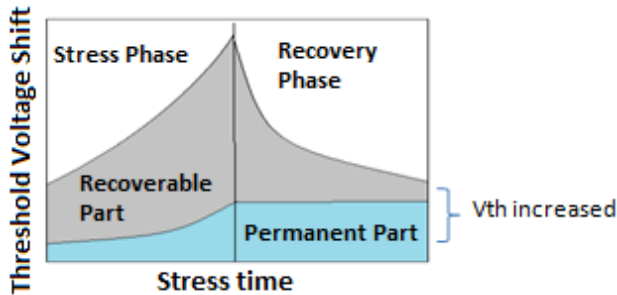


Figure 2: Temporary & Permanent phase of NBTI

Based on the Traps generation there are two components of NBTI, they are classified as Permanent (Non-Recoverable) and temporary (Recoverable). Permanent NBTI is due to the new interface traps generation i.e. the electric field is able to break Si-H bonds located at the silicon-oxide interface. Temporary NBTI is due to some pre-existing traps present in the gate oxide. The pre existing traps get filled with the holes coming from the channel of PMOS. This is called temporary because the traps can be emptied when the stress voltage is removed. Even after the removal of the stress the final increase in threshold voltage is mainly due to the permanent NBTI and partly due to temporary NBTI as shown in the fig. 2 as Stress phase and Recovery phase.

A gradual shift of threshold voltage ( $V_T$ ) over time is commonly observed in p type metal-oxide-semiconductor field-effect transistors (p-MOSFET or PMOS). This shift is mainly caused by: (1) voltage stress on the gate oxide (2) temperature, (3) the duty cycle of the stressing voltage (static stress as compared to dynamic stress). This effect has become more severe as: Transistor dimensions have shrunk, the electric field applied to the gate oxide has increased and the operating voltage has become lower. NBTI degrades the gate oxide by the interface states creation and hole trapping in the vicinity of the interface. An interface trap is created when a negative voltage is applied to the gate of a PMOS device for a prolonged time. An interface trap is located near the Si-oxide boundary where holes (positive charge) can get stuck, and hence, they shift the threshold voltage. NBTI is a result of continuous trap generation in Si-SiO<sub>2</sub> interface of PMOS transistors. In bulk MOSFET structure, undesirable Si dangling bonds exist due to structural mismatch at the Si-SiO<sub>2</sub> interface. These dangling bonds act as charged interfacial traps. Charge can flow between the semiconductor and the interface states. The net charge in these interface states is a function of the position of the fermi level in the bandgap. Hydrogen passivation is applied to the Si surface after the oxidation process to transform dangling Si atoms to Si-H bonds. However, with time, these Si-H bonds can easily break during operation (i.e., negative bias for PMOS). The broken bond acts as interfacial traps and increases the threshold

voltage ( $V_T$ ) of the device, thus affecting the performance of the IC. NBTI impact gets even worse in scaled technology due to the higher operation temperature and the usage of ultra thin oxide (i.e., higher oxide field). The following conditions holds good for the NBTI effect

- (1) PMOS needs to be inverted i.e. Formation of channel (Presence of charge particles) but doesn't need any current flow.
- (2) Needs negative electric field across oxide layer (Enhanced at relatively high negative gate voltage  $V_g$ s).
- (3) High temperature.

Thinner oxides have brought the poly-silicon gate closer the Si/SiO<sub>2</sub> interface. Note that diffusion of hydrogen away from the Si/SiO<sub>2</sub> interface controls NBTI-specific interface trap generation at the Si/SiO<sub>2</sub> interface. Since hydrogen diffusion through poly-silicon is faster than that in oxide, scaling of gate oxides has increased NBTI susceptibilities.

## II. IMPACT ON PARAMETERS

As discussed above the main parameter which is affected by the NBTI is Threshold Voltage ( $V_T$ ). NBTI raises threshold voltage above the initial value and hence subsequently degrades the other parameters like drain current, transconductance etc which depend on threshold voltage. The relationship between threshold voltage and interface trapped charges is given by,

$$V_T = V_{FB} - 2\Phi_F - |Q_B|/C_{ox} \quad \text{Where}$$

$$\phi_F = (kT/q)\ln(N_D/n_i), |Q_B| = (4qK_S \epsilon_0 \phi_F N_D)^{1/2}$$

and,

$$V_{FB} = \phi_{MS} - \frac{Q_F}{C_{OX}} - \frac{Q_{it}(\phi_S)}{C_{OX}}$$

Where  $Q_F$  is the fixed charge density,  $Q_{it}$  is interface trap density  $C_{OX}$  is the gate oxide capacitance and  $\Phi_{MS}$  is the work function between metal and semiconductor. The MOS drain current  $I_D$  (sat) and transconductance  $g_m$  is related with threshold voltage as,

$$I_D = \left(\frac{W}{2L}\right)\mu_{eff} C_{OX} (V_G - V_T)^2$$

$$g_m = \left(\frac{W}{2L}\right)\mu_{eff} C_{OX} (V_G - V_T).$$

Thus we see that the Threshold voltage  $V_T$  of a MOS is dependent on  $Q_F$  and  $Q_{it}$ . As the threshold voltage is increased due to the NBTI (increase in interface traps) the drain current  $I_D$  and transconductance  $g_m$  also degrades.

A shift in the threshold voltage ( $V_T$ )  $\Delta V_{th}$  of the PMOS transistor is proportional to the interface trap generation due to NBTI, which can be expressed as [5],

$$\Delta V_{th} = (1 + m) \frac{qN_{it}(t)}{C_{OX}}$$

Where  $m$  represents equivalent  $V_T$  shifts due to mobility degradation (or model parameter),  $q$  is the electronic charge, and  $N_{it}(t)$  is the interface trap generation, which is the most important factor in evaluating performance degradation due to NBTI.



III. CONCEPT OF INTERFACE CHARGES AND NBTI MECHANISM ONLY IN PMOS

NBTI Mechanism is better understood by the Reaction Diffusion model (RD model) [6], which explains the physics behind the degradation of the PMOS devices in terms of different sub-processes involving the bond breaking process and generation of interface traps.

According to the RD model, NBTI degradation originates from Silicon Hydrogen bonds (Si-H) breaking at Silicon-Silicon dioxide (Si-SiO<sub>2</sub>) interface during negative stress ( $V_{gs} = -V_{DD}$ ), as shown in Figure 3. The broken Silicon bonds (Si<sup>-</sup>), dangling silicon act as interface traps that are responsible for higher  $V_T$  and lower drain current.

An interface trap is an interfacial trivalent silicon atom with an unsaturated (unpaired) valence electron at the SiO<sub>2</sub>/Si interface. Unsaturated Si atoms are additionally found in SiO<sub>2</sub> itself. Interface traps  $N_{it}$  generation is due to the dissociation of Si-H bonds at the Si/SiO<sub>2</sub> interface and subsequent movement of released hydrogen species away from the interface (diffusion), which leaves behind Si<sup>-</sup> dangling bonds (interface traps). Inversion layer holes tunnel into the oxide and interact with Si-H bonds. The holes get captured and take away one electron from the Si-H bonds and make them weak. The weakened Si-H bonds then get broken by thermal excitation or otherwise. The released hydrogen species either diffuse away from the Si/SiO<sub>2</sub> interface and leaves behind Si<sup>-</sup> ( $N_{it}$  generation), or reacts back with Si<sup>-</sup> and form Si-H ( $N_{it}$  passivation). It is worth noting that the magnitude of  $N_{it}$  is equal to the number of released H atoms at any given instant of time. The time evolution of  $N_{it}$  generation is modeled by the following equations.

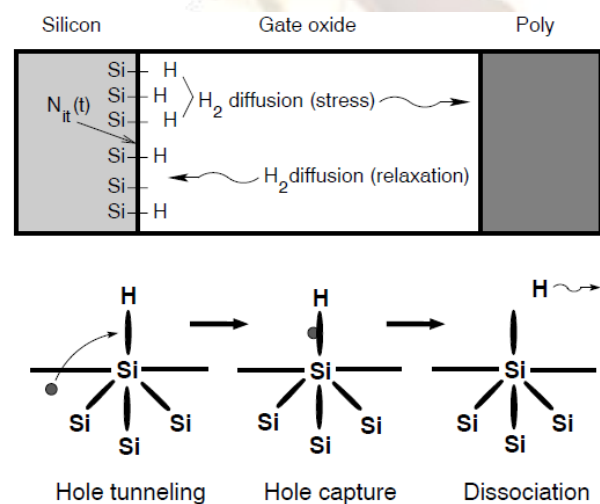
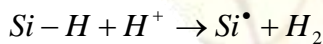
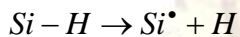


Figure 3: Representation of RD model [6]

The H atoms released from Si-H bond breaking contribute to three sub-processes including: (a) diffusion towards the gate, (b) combination with other H atoms to produce H<sub>2</sub>, or (c) recovery of the broken bonds. Similarly, H<sub>2</sub> participate in the

diffusion towards poly gate or dissociation to produce H atoms. The bias temperature stress-induced  $V_T$  shifts are generally known to be the consequence of underlying buildup of interface traps and oxide-trapped charge due to stress-initiated electrochemical processes involving oxide and interface defects, holes and/or electrons, and variety of species associated with presence of hydrogen as the most common impurity in MOS devices. An interface trap is an interfacial trivalent silicon atom with an unsaturated (unpaired) valence electron at the SiO<sub>2</sub>/Si interface. Unsaturated Si atoms are additionally found in SiO<sub>2</sub> itself, along with other oxide defects, the most important being the oxygen vacancies. Both oxygen vacancies and unsaturated Si atoms in the oxide are concentrated mostly near the interface and they both act as the trapping centers responsible for buildup of oxide-trapped charge. Interface traps readily exchange charge, either electrons or holes, with the substrate and they introduce either positive or negative net charge at interface, which depends on gate bias: the net charge in interface traps is negative in n-channel devices, which are normally biased with positive gate voltage, but is positive in p-channel devices as they require negative gate bias to be turned on. On the other hand, charge found trapped in the centers in the oxide is generally positive in both n- and p-channel MOS transistors and cannot be quickly removed by altering the gate bias polarity. The absolute values of threshold voltage shifts due to stress-induced oxide-trapped charge and interface traps in n- and p-channel MOS transistors, respectively, can be expressed as [14]:

$$\Delta V_{Tn} = \frac{q\Delta N_{ot}}{C_{OX}} - \frac{q\Delta N_{it}}{C_{OX}}$$

$$\Delta V_{Tp} = \frac{q\Delta N_{ot}}{C_{OX}} + \frac{q\Delta N_{it}}{C_{OX}}$$

where q denotes elementary charge,  $C_{ox}$  is gate oxide capacitance per unit area, while  $\Delta N_{ot}$  and  $\Delta N_{it}$  are stress-induced changes in the area densities of oxide-trapped charge and interface traps, respectively. The amounts of NBT stress-induced oxide-trapped charge and interface traps in n- and p-channel devices are generally similar, but above consideration clearly shows that the net effect on threshold voltage,  $\Delta V_T$ , must be greater for p-channel devices, because in this case the positive oxide charge and positive interface charge are additive. As for the question on the role of stress bias polarity, it seems well established that holes are necessary to initiate and/or enhance the bias temperature stress degradation, which provides straight answer since only negative gate bias can provide holes at the SiO<sub>2</sub>/Si interface. Moreover, this is an additional reason[3] why the greatest impact of NBTI occurs in p-channel transistors since only those devices experience a uniform negative gate bias condition during typical CMOS circuit operation.

There can be two types of NBTI stress, it can be DC or AC stress. Once NBTI stress is removed from the device, a fraction of Interface traps  $N_{it}$  can self-anneal, resulting in  $V_{th}$

degradation being partially recovered. This recovery mechanism can be observed when a device is subject to a strain of stressing pulses. These conditions are called “AC” stress. Within the context of reliability, AC stress actually designates a large-signal pulse-like stress signal. During the first phase of the clock cycle,  $V_{th}$  increases due to the stress applied, and then it decreases again in the second half of the cycle when the stress is removed as shown in the figure 4 below. As shown in the figure, a CMOS inverter is drawn and when the  $V_g$  i.e. input gate voltage is zero (i.e.  $V_{gs} = -V_{DD}$ ), the PMOS will be in the Stress phase and when  $V_g$  is  $V_{DD}$  (i.e.  $V_{gs} = 0$ ) then PMOS will be in relaxation phase as shown. During Stress phase the effect of NBTI comes into picture.

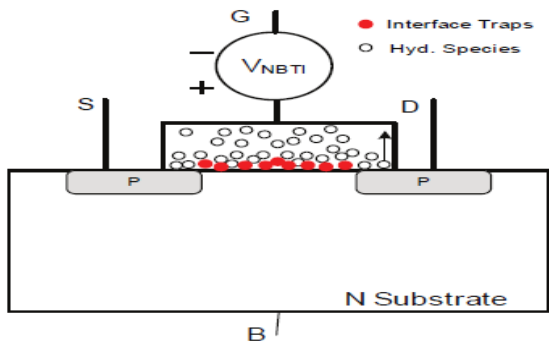


Figure 4: PMOS transistor degradation due to NBTI

But the degradation rate is different (smaller) from “DC” stress conditions when the device is permanently stressed. This has often led to the conclusion that AC stress was less problematic than DC stress. The degradation rate under AC stress conditions actually depends on the duty cycle of the applied stress signal [8][10].

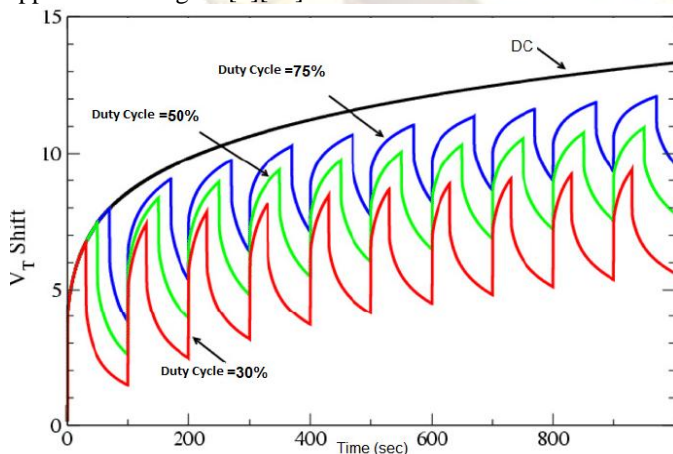


Figure 5: NBTI Degradation under DC and AC stress with different duty cycles [9]

#### IV. SIMULATION RESULTS AND DISCUSSION

ELDO is a circuit simulator developed by Mentor Graphics, which delivers all the capability and accuracy of the SPICE level simulation for complex analog circuits and SoC designs. NBTI reliability simulation in Eldo is based on a model, which

models the difference between the fresh and aged devices by calculating the NBTI stress which is dependent on the applied gate stress and the temperature. The following results are of a CMOS inverter circuit (for 45nm design), which has been simulated in the tool ELDO. The below results are shown in the waveform viewer EZWave, used to view the output waveforms of ELDO file. Firstly a CMOS inverter circuit is described by a .cir file in the ELDO using the slow model of 45nm technology. Then simulation is carried out with this .cir file. During simulation, first stress file is generated in which stress for each device is calculated as per the ELDO’s UDRM model and aged simulation uses this stress file to find the degradation.

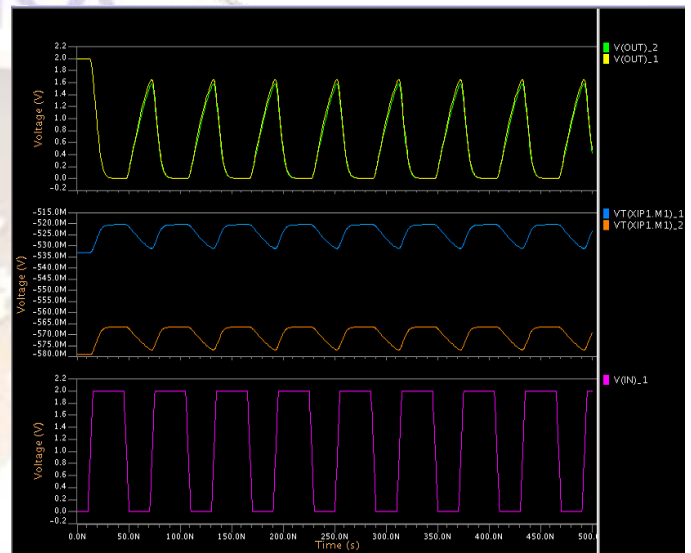


Figure 6: Inverter plots showing output, threshold and input voltage

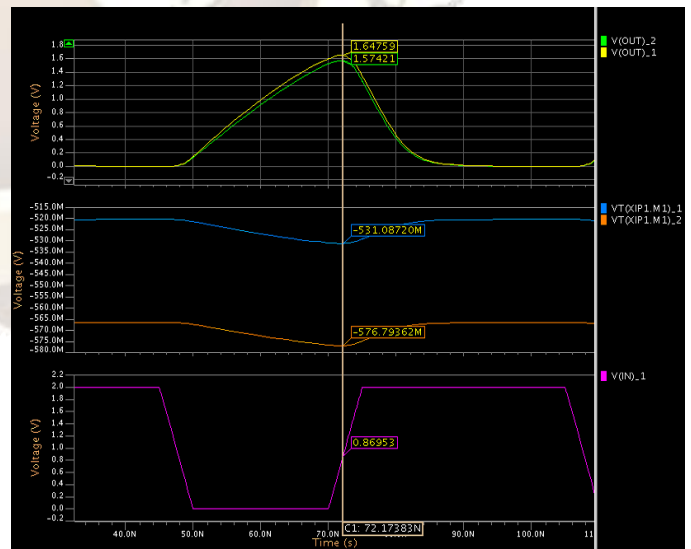


Figure 7: Magnified version of figure 7 at a particular time stamp

The above figures 7 and 8 show the output voltage, threshold voltage and input voltage of inverter circuit. The values shown are for the input pulse whose magnitude is 2V, rise time and fall time is 5nsec, pulse width is 30nsec and period is 60nsec.

The transient analysis is done for 500ns in ELDO and the whole simulation is run for the period of 2years (i.e. output is checked after 2 years). The V (OUT)\_1 value in yellow color is fresh output and V (OUT)\_2 with green color is output after 2 years. At a particular time stamp of 16.19718ns the values are (shown in the rectangular boxes):

At room temperature i.e. at  $t=25^{\circ}\text{C}$ , the results are as follows for the input V (IN) 0.86953V

Type of Simulation	V(OUT) in V	$V_{TH}(XIP1.M1)$ in V
Fresh(V(OUT)_1)	1.64759	-0.53108720
After 2 yrs(V(OUT)_2)	1.57421	-0.57679362

Apart from these values the instantaneous stress is also plotted for the PMOS (XIP1.M1) as shown in the Fig 9. We can see the degradation in the output after 2 yrs due to stress in the PMOS devices.

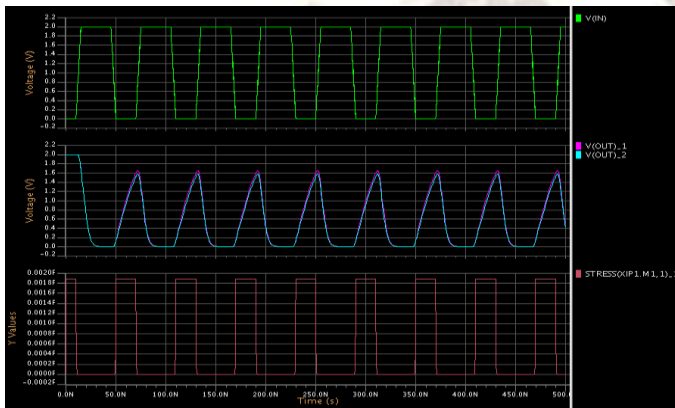


Figure 8: CMOS inverter plot showing instantaneous Stress along with input and output

To see the temperature effect the temperature of the simulation is increased to  $125^{\circ}\text{C}$ . So when the temperature is increased to  $125^{\circ}\text{C}$  the output is,

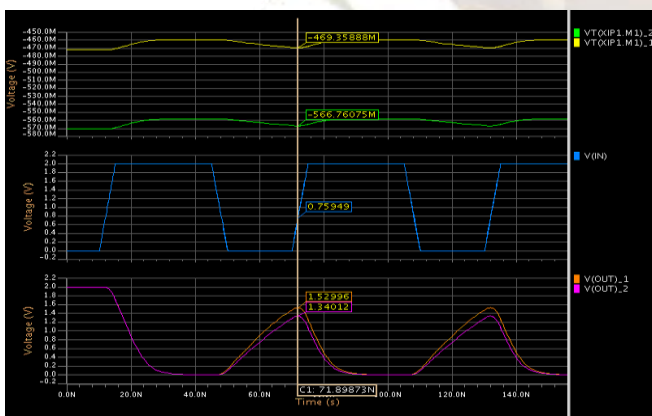


Figure 9: Input, Output and Threshold voltage of a CMOS inverter when temperature is  $125^{\circ}\text{C}$

At temperature  $127^{\circ}\text{C}$ , the results are as follows for V (IN) 0.75949V,

Type of Simulation	V(OUT) in V	$V_{TH}(XIP1.M1)$ in V
Fresh(V(OUT)_1)	1.52996	-0.46935888
After 2 yrs(V(OUT)_2)	1.34012V	-0.56676075

## V. CONCLUSION

Based on the simulation results with an industrial 45nm technology, it is observed that the degradation of output voltage due to NBTI in a CMOS inverter can be as high as 4.5% for a stress period of two years. As far as temperature variation is concerned, the degradation is increased to about 12% at a temperature of  $125^{\circ}\text{C}$ . So Lower temperature is also desirable for robust nanoscale design. The transistor reliability will be a severe problem in future technology nodes which makes the device life time shorter than predicted.

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