

## **REDUCTION OF LEAKAGE POWER IN 8T SRAM CELL USING VIRTUAL GROUND**

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### **Abstract**

This paper describes stability problems in 6T SRAM cell and their solutions with 8T SRAM cell. 8T SRAM with the virtual ground concept has been proposed which reduces leakage power. Comparison of 8T SRAM cell proposed with conventional 6T SRAM cell with respect to leakage power are proved by simulation and experimentally using the tool cadence (180nm technology).

**Keywords:** Cell stability, Leakage power, Virtual ground.

### **1. Introduction**

The embedded memories account to 65 percent of the area in modern SoC. The memory area increases with the complexity of SoC and by the year 2018, it is expected to go to 90 percent. Most of the memory is composed of the SRAM cells. With increasing variability in the future CMOS manufacturing processes, the SRAM cell stability, which depends on the balance of transistors, becomes a major concern. As the device dimensions decrease, the SRAM cell becomes more and more susceptible to process variations. The effect of random variations in logic paths can be overcome to a certain extent by placing multiple stages, but in the case of memory, each SRAM cell must function according to the specifications [1]. In addition to the data stability issues, the increasing leakage energy consumption of the embedded memory circuits is also a growing concern. In modern high performance microprocessors, more than 40 percent of the total active mode energy is consumed due to leakage currents [2].

In the conventional six transistor SRAM cell, the read and write operations impose conflicting constraints on the transistors. Due to this any improvement done to enhance the stability for one operation will result in performance degradation in the other operation. The problem of improving the SRAM cell stability is further aggravated by lower supply voltages. As the supply voltage decreases, the threshold voltage variation account for a large fraction of the supply voltage. Many design techniques have been proposed to overcome the variability problems. A higher supply voltage exclusively for the SRAM array apart from the normal supply voltage is one way to enhance the noise margins of the SRAM cell [3]. In this case, the supply voltage of the SRAM cell will not scale with the technology. Further, it may increase if the variability problems become prominent. The supply voltage can be dynamically modulated for read, write and standby operations to achieve the required noise margin [4]. These separate the read and write operation from the standby operation. While these techniques provide better noise margins, they add to the complexity of the circuit. Also these techniques may result in increase of dynamic power consumption during the read and write operations. An 8T SRAM cell with two extra transistors and virtual ground has been proposed which is used to separate the read and write current path and avoid accidental cell flipping during read operation. This cell provides significant large SNM during Read operation improves cell stability, reduces leakage power and read power consumption.



### 2.2.2 Read failure

The read operation results in formation of a voltage divider network comprising of the access transistors N3 or N4 with the pull down transistors N1 or N2 respectively. This results in an increase of voltage in node storing logic value '0'. Due to process variations, if this voltage rises above the trip voltage of the inverter then the logic value stored in the cell gets corrupted resulting in a failure. This failure is defined as a read failure.

### 2.2.3 Write failure

Consider a SRAM cell storing a logic value of '1'. If '0' needs to be written to the cell, then voltage level at the node with '1' needs to pull down to voltage below the trip voltage of the inverter. This voltage is determined by the voltage divider network formed by transistors P1, N3 or P2, N4. Due to process variations, if the voltage is not pulled below the trip point within the time period of WL being high then this results in failure. This failure is defined as a write failure.

### 2.2.4 Hold failure

When the SRAM cell is in standby mode, the leakage power of the SRAM can be reduced by decreasing the supply voltage [7]. However if the voltage is lowered below a certain value the data stored in the SRAM may be lost. The minimum retention voltage is significantly affected by process variations. The failure of a SRAM cell to retain the data in standby mode is defined as Hold failure.

Apart from these, the interface of the SRAM cell through the bitlines with the sense amplifier may also reduce the stability of the SRAM cell during the read operation. Figure 1 shows the SRAM cell connected to the precharge circuit and a latch based sense amplifier. Consider logic value '0' in the SRAM cell. The voltage at node T is 0V and the voltage at node F is VDD. Suppose logic value '1' was read in the previous read operation through the sense amplifier. Even though the SEN signal is low, the sense amplifier retains the value at nodes ST and SF. Thus ST remains at VDD and SF remains at 0V. During the read operation, after the precharge operation, the wordline WL, column select signal CS and sense amplifier enable signal SEN are enabled. The node ST is connected to node T through transistors PN1 and N1. Due to the bi-directional nature of the pass transistors PN1 and PN2, there is a chance that node ST may drive node T to VDD thus switching the state of the SRAM cell. This failure is dependent on the size of transistor N1 of the SRAM cell and transistor SP1 of the sense amplifier. If the width of SP1 is much larger than that of N1, then the probability of this failure is extremely high.

## 3. Proposed 8T SRAM Cell

In the proposed 8T SRAM cell, two extra transistors are used to separate the read and write current path and avoid accidental cell flipping during read operation. This cell provides significant large SNM during Read operation.

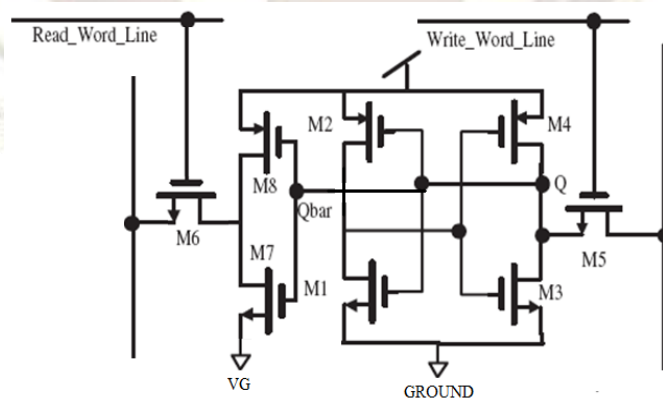


Figure 2: Proposed 8T SRAM cell with virtual ground

### 3.1.1 8T Write Operation

Transistor M5 is turned on by enabling the write\_word\_line. For writing '1' write\_bit is charged to logic '1' then  $Q$  charges to logic '1' and  $Qbar$  discharges to logic '0'. For writing '0' write\_bit is charged to logic '0' then  $Q$  discharges to logic '0' and  $Qbar$  charges to logic '1'.

### 3.1.2 8T Cell Read Operation

Before read operation starts Read\_bit is precharged to zero and then M6 is turned on by enabling the Read\_word\_line. During Read '0' M8 and M7 are turned ON and OFF respectively. So the Read\_bit line starts to charge. Sense amplifier detects 0.22v rise in the Read\_bit line and gives output as logical '0'. During Read '1' M8 and M7 are turned OFF and ON respectively. So the Read\_bit line remains at 0v only. Sense amplifier detects this and gives output as logical '1'.

Read operation is done by M6, M7 and M8 MOSFETs. The read path doesn't include the node's  $Q$  or  $Qbar$  which causes no disturbance to the memory circuit during read operation. Hence the main problem of stability in the conventional cell is avoided in the 8T cell.

### 3.1.3 Role of virtual ground

Whenever  $Q$  is '0' and Read\_Word\_Line is not enabled M7 causes unnecessary leakage. This can be avoided by connecting M7 to the virtual ground instead of ground. Virtual ground acts as ground when Read\_Word\_Line is enabled and in other case it provides logical '1'. On overall this reduces a considerable amount of leakage power.

## 4. Characteristics of Proposed 8T SRAM Cell

The determination of characteristics of the new SRAM cell and the comparison with the existing architectures are conducted. Cadence was used for circuit level simulation. The target technology chosen was 180nm. Scaled dimensions for the transistors were assumed with a lambda of 90nm. The minimum length and width of a transistor were assumed to 180nm and 240nm respectively. The supply voltage was assumed to be  $VDD=1.8V$ . Initially the leakage of the SRAM cell is analyzed. Later, process variations are introduced and the variations of these characteristics are presented. The power of the memory architecture is dependent on the application. Hence the best case and worst case for both these characteristics are presented. A memory bank which consists of 128 rows and 8 columns array of proposed 8T SRAM is designed. Another 128\*8 conventional 6T SRAM is also designed for comparison.

### 4.1 Leakage Power

Leakage power of a SRAM cell is the power consumed by the SRAM cell when it is in standby mode. Figure7 shows the comparison of the leakage power of the SRAM cells. Since the transistors of the proposed SRAM cell are sized to minimum, the leakage power is less when compared to the other conventional SRAM cells even though the 8 transistor SRAM cell has an extra path for discharging the read bitline.

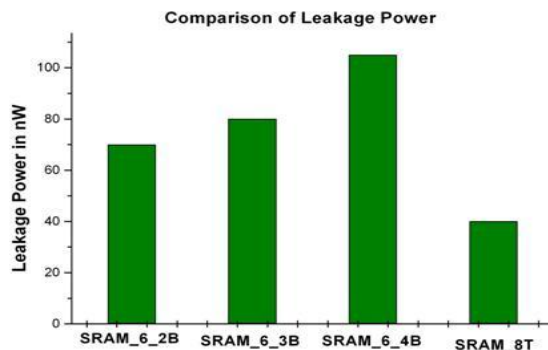


Figure3: Leakage Power Consumption various SRAM cells

## **5. CONCLUSION**

In this paper leakage power reduction in 8T SRAM cell is shown with the use of virtual ground concept when compared to conventional 6T SRAM cell signal. By designing 8T SRAM cell with the help of virtual ground concept, the read SNM is increased (almost doubled). The cell also supports low power operation. This new asymmetric cell structure is capable of using differential sense technique for high speed read operation.

## **6. REFERENCES**

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