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Comparison of Multi-level inverters by reducing common mode voltages and DC-link capacitor voltage balancing for IM drives

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Abstract - In PWM inverter-fed drives, a variation of Common mode voltage (CMV) causes unbalanced voltage operation in induction motor. Multilevel inverters reduce this problem, but the complexity of the power circuit increases with an increase in the number of inverter voltage levels. In this paper, a five-level inverter is compared with two, three and four levels and this five level structure is proposed for open-end winding induction motor (IM) drives. It consists of cascaded two conventional two-level and three-level inverters. The DC link power supply requirement is also optimized by means of DC link capacitor voltage balancing, with PWM control, using only inverter switching state redundancies. In the considered configuration the two two-level inverters are shared by the two three-level inverters at both ends of the motor stator winding.

Keywords **Multi-level inverters, Common mode voltage,**
Capacitor voltage balancing, Induction motor drives.

I INTRODUCTION

The complexity of the power circuit increases as the number of voltage levels increases in the multi-level inverters. As a consequence, the neutral point clamped (NPC) inverter with more than three levels is seldom utilized for motor drives. The conventional NPC three-level inverter is characterized with the problem of neutral point voltage fluctuation and this voltage fluctuation causes unbalance in the DC-link capacitor voltages. Unbalance in capacitor voltages leads to excessive voltage stress on the switching devices and generates low order harmonic currents, resulting in torque pulsation.

As the number of levels increases, the number of DC-link capacitors will increase and balancing of the capacitor voltages becomes very difficult. Due to the low number of Redundant switching states in the voltage space vector locations, DC-link capacitor voltage balancing is very difficult in the conventional NPC inverters, especially in the high modulation range.

If a motor drive is with an open-end stator winding structure rather than with a star-connected stator winding, multi-level inverter supply schemes can be realized by supplying the two sides of the windings with inverters of a certain number of levels. Combined CMV elimination and capacitor Voltage balancing scheme for a five-level inverter-fed open-end winding IM drive has been proposed.

In this paper, combined CMV elimination and capacitor voltage balancing are discussed in conjunction with an open-end winding induction motor drive. Compared to the power circuit structure employed in, the configuration utilized in this paper is considerably simpler. The scheme described here is capable of maintaining the DC-link capacitor voltages for both motoring and generating mode of operation, without affecting the output fundamental.

II Power circuit of Five-level inverter

Power circuit configuration of the five-level inverter structure for an open-end winding induction motor drive, analyzed in this paper, is shown in Fig.1. There are a total of two two-level and two three-level inverters. Each of the two inverter systems (A and A') consists of a series-connected NPC three-level inverter and the conventional two two-level inverters. The two-level inverters are shared by both inverter systems A and A', as shown in Fig.1.

Each two-level/three level inverter combination will produce a five-level voltage space vector structure. The combined multi-level inverter will therefore produce a nine-level voltage space vector structure. However, not all of the available voltage space vectors are characterized with switching states leading to the zero CMV.

Hence only those switching states that yield zero CMV are selected for the PWM operation in this study, resulting in a combined five-level voltage space vector structure.

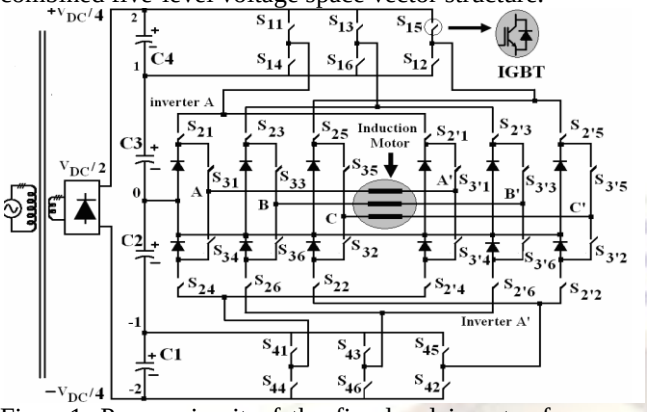

Figure1. Power circuit of the five-level inverter for open-end winding induction motor drive.

The Switching states and voltage space vector locations of five-level inverter (A or A') shown in the Fig.-2. In this fig. the shaded region indicates the 19 switching states and corresponding voltage vector locations, generating zero common-mode voltage.

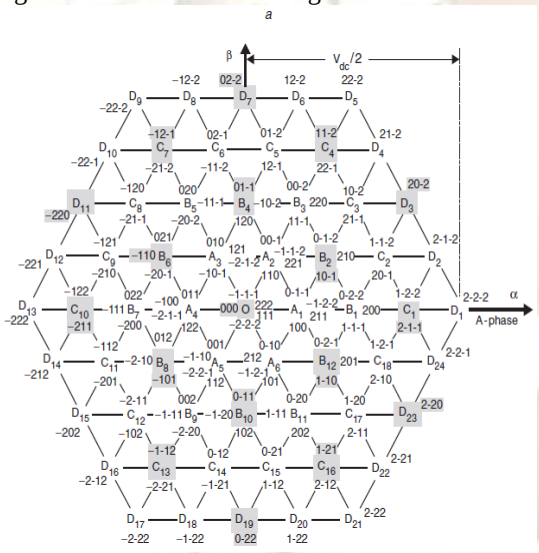

Fig : 2 Switching states and voltage space vector locations of five-level inverter (A or A')

Common-mode voltage (CMV) generated by the inverters, at both ends of the open-end winding induction motor, is expressed using the pole voltages. CMV for inverter system-A is defined as

$$V_{CMVA} = \frac{V_{AO} + V_{BO} + V_{CO}}{3}$$

While the CMV for inverter system-A' is defined as

$$V_{CMVA'} = \frac{V_{A'O} + V_{B'O} + V_{C'O}}{3}$$

Thus, the equivalent CMV for the combined inverter system (CMV generated at the inverter phases) is then

$$V_{CMV} = V_{CMVA} - V_{CMVA'}$$

From the above analysis, the resultant common mode voltage V_{CMV} can be made zero by making both V_{CMVA} and $V_{CMVA'}$ individually zero. Table-I shows all the switching states available (with zero CMV) for the voltage vectors for the 30^0 angular segment for the power circuit structure of Fig.1. The highlighted switching states of Table I are used for the open-loop control of capacitor voltages, as discussed next.

Table-I Redundant switching state combinations for the 30^0 region with zero common mode voltage

Voltage space vector location and number of available redundant switching state combinations (in brackets)	Redundant switching state combinations for particular voltage location (Inverter-A switching state, Inverter-A' switching state)
O(19)	(000,000), (01-1,01-1), (02-2,02-2), (-220,-220), (0-11,0-11), (0-22,0-22), (10-1,10-1), (11-2,11-2), (1-10,1-10), (1-21,1-21), (20-2,20-2), (2-1-1,2-1-1), (2-20,2-20), (-101,-101), (-110,-110), (-12-1,-12-1), (-1-12,-1-12), (-202,-202), (-211,-211)
A_1 (4)	(000,-101), (01-1,-110), (10-1,000), (1-10,0-11)
B_1 (9)	(000,-202), (10-1,-101), (01-1,-211), (1-10,-1-12), (02-2,-220), (2-1-1,0-11), (11-2,-110), (20-2,000), (2-20,0-22)
B_2 (4)	(000,-1-12), (10-1,0-11), (01-1,-101), (11-2,000)
C_1 (4)	(10-1,-202), (11-2,-211), (20-2,-101), (2-1-1,-1-12)
C_2 (4)	(01-1,-202), (10-1,-1-12), (11-2,-101), (20-2,0-11)
D_1 (1)	(20-2,-202)
D_2 (2)	(11-2,-202), (20-2,-1-12)
D_3 (3)	(02-2,-202), (11-2,-1-12), (20-2,0-22)

III. DC-LINK CAPACITOR VOLTAGE CONTROL – AN OPEN LOOP METHOD

In the open-loop method the power circuit of Fig.-1 with a single DC-link is analyzed for DC-link capacitor voltage balancing of all the four capacitors. Let the currents through the middle points of the

capacitors C_4, C_3; C_3, C_2; and C_2, C_1 are denoted as i_3 , i_2 and i_1 , respectively.

Then the following holds true:

$$V_{C4} - V_{C3} = \frac{1}{C}\int i_3\, dt$$

$$V_{C3} - V_{C2} = \frac{1}{C}\int i_2\, dt$$

$$V_{C2} - V_{C1} = \frac{1}{C}\int i_1\, dt$$

From the above equations, it follows that the DC-link capacitor voltages vc_4, vc_3, vc_2 and vc_1 will be equal if the currents i_3, i_2 and i_1 are Zero. Hence, to maintain the balance in the DC-link capacitor voltages, it is necessary to make all these three currents equal to zero. The aim of the selection of the switching states for the voltage vectors is here to simultaneously eliminate the common mode voltage and to eliminate the DC-link capacitor voltage unbalancing.

For the elimination of the CMV, only those switching states that have the zero CMV are switched for the PWM operation, (Table I). The same switching states from a particular location, having opposite effect on the capacitor voltages, are used in the present study for open-loop voltage control. Selection of the switching states for open-loop control of capacitor voltages is explained in the following two sections.

i) Selection of the Switching States For Open-Loop Control of Capacitor Voltages:

According to the voltage vectors, the switching states can be categorized into 5 groups. Center point 'O' is the zero voltage (*ZV*) vector point and there are 19 switching states. The voltage vectors from A_1 to A_6 are the 2LV (two-level) voltage vectors, and each vector location consists of four redundant switching states.

The voltage vectors from B_1 to B_{12} are the 3LV (three-level) voltage vectors. The voltage vectors from C_1 to C_{18} are the 4LV (four level) voltage vectors and the voltage vectors from D_1 to D_{24} are the 5LV (five-level) voltage vectors.

The switching states for the PWM operation at vector location A_1 are (000,-101) and (10-1,000). Fig.-3 shows the currents through the DC-link capacitors for these two switching states. As shown in Fig.-3, for both switching states, current through C_4 and C_1 is $i_C + i_A$. For the switching state (000,-101) currents through C_3 and C_2 are i_A and i_C, respectively, and for the switching state (10-1,000) currents through C_3 and C_2 are i_C and i_A, respectively. So, the voltages across C_4 and C_1 will be identical, as the same currents are flowing through them. But the voltages across all the four capacitors are not the same, since different currents flow through C_4 and C2. From the study of all the switching states of the voltage vector locations (Table I), it is observed that complementary states are not available to keep the four capacitor voltages identical for the power circuit of fig.-1.

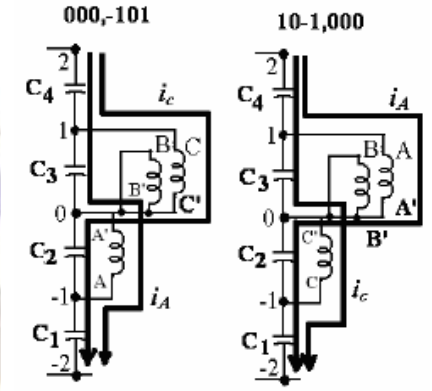

Fig-3 Connection of the three phases for the two switching states at A_1

However, it is also observed that it is possible to control the voltages, separately across capacitors C_4 and C_1 (outer two capacitors) and across capacitors C_2 and C_3 (inner two capacitors), and not all four together. To overcome this problem with the power circuit of Fig.3, a modified power circuit is used and this modified power circuit is shown in Fig-4.

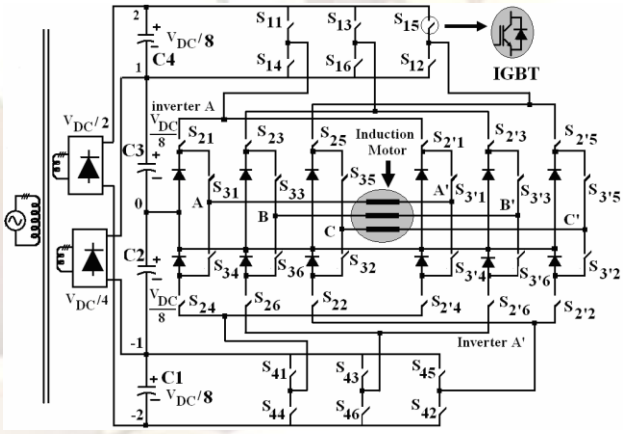

Fig-4. Modified circuit diagram of the five-level inverter-fed IM drive

Two DC-link power supplies are used for the modified scheme of Fig.4. In this circuit total voltage across the four DC-link capacitors is fixed to V_{DC} /2 and the total voltage across the two inner DC-link capacitors (C_2 and C_3) is fixed to V_{DC} /4. Hence the total voltage across the outer two capacitors (C_1 and C_4) is also fixed to V_{DC} /4. It is now enough to maintain the balance between the capacitor voltages

across C_1 and C_4 and the capacitor voltages across C_2 and C_3, separately.

ii) For the two dc-link power supplies, Selection of the switching states for the voltage vectors:

For Zero-Voltage group:

The switching state (000,000) will be selected to switch the zero voltage vectors. For this switching state there will be no currents flowing through the dc-link capacitors. Hence for the zero voltage vectors, this switching state has no effect on the dc-link capacitor voltages.

For 2-Level Voltage Group:

The switching states for the voltage vector A_1 are shown in Table-I. The direction of currents through the DC-link Capacitors for the switching states (000, -101) and (10-1,000) are shown in Fig.-3. These switching states are complementary states and are selected for PWM control in successive sampling intervals. Currents through the capacitors C_2 and C_3 are i_C and i_A, respectively, for the switching state (000,-101), and i_A and i_C, respectively, for the switching state (10-1,000). So the voltage across these two capacitors will be identical, after two sampling intervals. It can also be noted that the same current $i_A + i_C$ flows through the capacitors C_1 and C_4 during these complementary switching states and hence it has the same effect on these two capacitors. Thus, after two sampling intervals, it can be concluded that the voltages across the two groups of capacitors are identical.

Therefore it is stated that, with two DC-link voltages the capacitor voltages can be controlled using complementary switching states, in successive sampling intervals. For the other vector locations of the 2LV group (two-level operation), the same approach can be used.

For 3-Level, 4-Level and 5-Level Voltage groups:

For the voltage vector at B_1, the switching state (10-1,-101) of the 3LV group (three-level operation) is shown in Table-I. It is observed from Fig.-5 that current through C_4 and C_1 is $i_A + i_C$, resulting in identical voltage variation across these two capacitors. There are no phase currents passing through the capacitors C_2 and C_3, resulting in identical voltages across them. So this switching state has no effect on all the DC-link capacitor voltages.

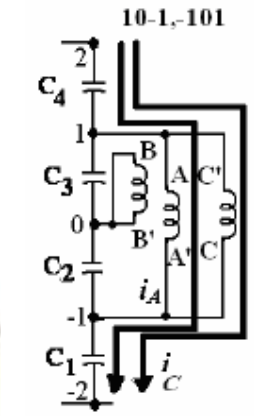

Fig.-5: Connection for the switching state of the voltage vector at B_1.

This switching state can be used for the two successive sampling intervals (Fig.-6), as it is not creating any unbalance in the capacitor voltages. It is observed that for all the 61 voltage vectors of the hexagonal structure, there are switching states that are either complementary or have no effect on the DC-link capacitor voltages. For the voltage vector in 4LV (four-level operation) and 5LV (five-level operation) groups, the effect of complementary switching states on capacitor voltage control can also be explained in similar manner.

Fig.-6: Selection of the switching states for the triangular sector $A_1 B_1 B_2$

Fig.-6 explains the selection of the switching states for the sector formed by the vector locations A_1, B_1, B_2 (Fig. 3.2) in two consecutive sampling intervals (2Ts). Switching states for the A_1 voltage vectors are (000,-101) and (10-1,000). Switching state for B_1 voltage vector is (10-1,-101) (as it is not creating any unbalance, Fig.3.6) and for the voltage vector B_2 two complementary switching states (01-1,-101) and (10-1, 0-11) are selected for PWM control.

The unbalance in the DC-link capacitor voltages will cause low order harmonics in the pole and phase voltages and can exceed the device voltage rating. So, to bring back the system to the balanced condition, in case of unbalance in DC-link capacitor voltage due to the above mentioned conditions, a closed-loop control is introduced in the following section.

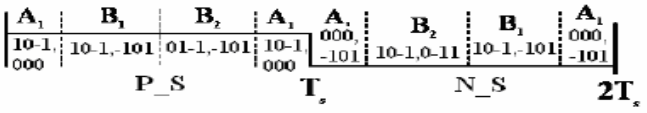

TABLE-III: Switching state combinations for voltage vectors in the 30° segment of for Closed-loop control

Voltage vector and group	Possible combinations of states of comparators 1 and 2 and selection of the switching states for Inverter-A and Inverter-A' (Inv.-A, Inv.-A')																	
	C_{1N} C_{2N}		C_{1N} C_{2H}		C_{1N} C_{2L}		C_{1H} C_{2N}		C_{1L} C_{2N}		C_{1H} C_{2H}		C_{1H} C_{2L}		C_{1L} C_{2H}		C_{1L} C_{2L}	
	P_S	N_S	P_S	N_S	P_S	N_S	P_S	N_S	P_S	N_S	P_S	N_S	P_S	N_S	P_S	N_S	P_S	N_S
O (ZV)	000,000																	
A_1 (2LV)	10-1, 000	000, -101	1-10, 0-11		01-1, -110		10-1, 000	000, -101	10-1, 000	000, -101	1-10,0-11		01-1, -110		1-10, 0-11		01-1, -110	
B_1 (3LV)	10-1, -101										2-20, 0-22		10-1, -101				02-2, -220	
B_2 (3LV)	01-1, -101	10-1, 0-11	01-1, -101	10-1, 0-11	01-1, -101	10-1, 0-11	000, -1-12		11-2, 000		01-1, -101	10-1, 0-11	01-1, -101	10-1, 0-11	01-1, -101	10-1, 0-11	01-1, -101	10-1, 0-11
C_1 (4LV)	20-2, -101	10-1, -202	20-2, -101	10-1, -202	20-2, -101	10-1, -202	2-1-1, -1-12		11-2, -211		20-2, -101	10-1, -202	20-2, -101	10-1, -202	20-2, -101	10-1, -202	20-2, -101	10-1, -202
C_2 (4LV)	01-1, -202	20-2, 0-11	11-2,-101		10-1,-1-12		01-1, -202	20-2, 0-11	01-1, -202	20-2, 0-11	11-2,-101		10-1,-1-12		11-2,-101		10-1,-1-12	
D_1 (5LV)	20-2, -202																	
D_2 (5LV)	11-2, -202	20-2, -1-12	11-2, -202	20-2, -1-12	11-2, -202	20-2, -1-12	11-2, -202	20-2, -1-12	11-2, -202	20-2, -1-12	11-2, -202	20-2, -1-12	20-2, -1-12		11-2, -202		11-2, -202	20-2, -1-12
D_3 (5LV)	11-2, -1-12																	

IV. CLOSED-LOOP CONTROL OF DC-LINK CAPACITOR VOLTAGE BALANCING

For the closed-loop control of the DC-link capacitor voltage balancing, a simple hysteresis controller is used. A Hall Effect sensor is used to sense the voltages across the DC-link capacitors. The input to the controller will be the difference of the two capacitor voltages (the controller has two inputs, the difference between the outer two capacitor voltages and the difference between the inner two capacitor voltages).

The controller will sense the unbalance in the capacitor voltages from the voltage difference. The controller will take the corrective action only if the difference of the voltages between the two capacitors exceeds the specified hysteresis band. The Error band can be specified for the hysteresis controller depending on the voltage rating of the devices and the Maximum error allowable for the system.

The Fig.7 shows the hysteresis controller block diagram for the closed loop control scheme of the DC-link capacitor voltage balancing.

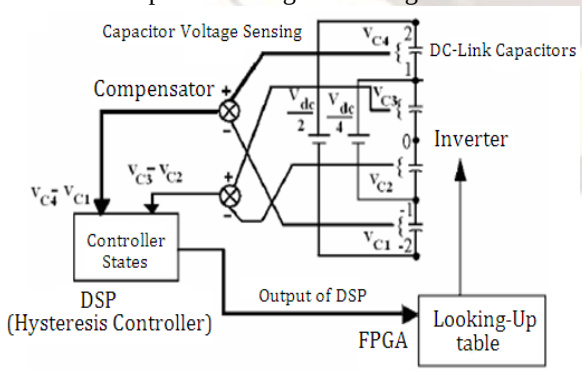

Fig.-7: Hysteresis controller for the closed-loop control of the dc-link capacitor voltage balancing

There are two comparators, as shown in Fig.-7, that continuously compare the difference between the outer two and the inner two DC-link capacitor voltages. The outputs of the comparators are fed to the hysteresis controller. There will be three different states for each group (C_1 and C_4 are in group-1, C_2 and C_3 are in group-2) of the DC-link capacitor voltages and these are identified as C_H, C_N, C_L.

Table-II shows the states for various DC-link capacitor voltage differences, for each group of capacitors. These states are called the controller states, as the controller will select those inverter switching states for balancing the voltages across the DC-link capacitors

TABLE–II: Controller states for the different dc-link capacitor voltage conditions (Capacitors C_4, C_1 and C_3, C_2).

Capacitor Voltage difference	States
$V_{C4} - V_{C1} > 0$ $V_{C3} - V_{C2} > 0$	C_{1H} C_{2H}
$V_{C4} - V_{C1} = 0$ $V_{C3} - V_{C2} = 0$	C_{1N} C_{2N}
$V_{C4} - V_{C1} < 0$ $V_{C3} - V_{C2} < 0$	C_{1L} C_{2L}

The combinations from the two comparator outputs of Fig.7 will generate nine controller output states, identified as follows:

C_{1H} C_{2H}, C_{1H} C_{2N}, C_{1L} C_{2N}
C_{1N} C_{2N}, C_{1N} C_{2H}, C_{1N} C_{2L}
C_{1H} C_{2L}, C_{1L} C_{2H}, C_{1L} C_{2L}

Table-III shows the selection strategy for the switching states of the voltage vectors (30^0 angular

regions) for the closed-loop control of the DC-link capacitor voltage balancing. From Table-III it is observed that the voltage vector A_1 has no corrective switching states for the controller states $C_{1H}C_{2N}$ and $C_{1L}C_{2N}$. In this condition two complementary switching states, at that vector point, are switched. The system will be brought back to the normal state by the switching state from other vertices of a sector, during PWM operation, in a triangular sector.

Some of the switching states of Table-III are used for both positive (P_S) and negative cycles (N_S) (two successive sampling intervals, Fig.-6), and some are only used for either positive or negative cycle. It should also be noted that some of the switching states (highlighted in Table-III), for a particular controller state, are capable of bringing the system from that state to the normal state ($C_{1N}C_{2N}$) immediately.

V. SIMULATION RESULTS

To check the controller Action at every level of operation, the closed-loop controller is disabled for a moment and then again enabled. It can be observed that the deviation due to disabling of the controller is brought back to the normal state quickly once the controller is enabled.

In two-level and three-level operation, it can be noted that there is no effect on *vc*1 and *vc*4 due to disabling of the controller, while voltages *vc*2 and *vc*3 are affected. But from four-level to 12-step mode of operation, deviation occurs in all the four capacitor voltages due to the disabling of the controller.

TWO-LEVEL INVERTER:

In Two-level inverter, the switching states can be selected for PWM control in successive sampling intervals. The capacitor voltages can be controlled using complementary switching states in successive sampling intervals. The voltage levels are 0 and V_{dc} or 0 and $-V_{dc}$. For the two level inverter, the phase voltage and phase current are shown in Fig-8.

The variation of capacitor voltages during disabling and enabling of control is shown in fig.-8. After sampling period 0.02 sec, the capacitor voltages can be balanced.

For the two-level inverter, the phase current FFT and phase voltage FFT are shown in the fig-8. The total harmonic distortion (THD) of the phase current and phase voltage are 3.75% and 116.9% respectively.

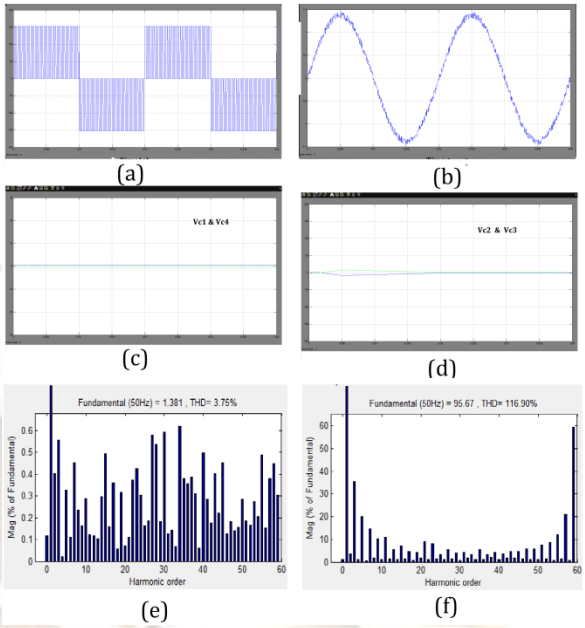

Fig-8 (a)Phase Voltage & (b)Current waveforms for the two-level operation
(c) & (d) Variation of capacitor voltages during disabling and enabling of control
(e) & (f) Spectra of the phase current and phase voltage.

THREE-LEVEL INVERTER:

In the three level inverter, the switching states have no effect on the DC link capacitor voltages and they are not creating any unbalance in capacitor voltages. The voltage levels are 0, Vdc/2 and Vdc.

For three level inverter, the phase voltage and phase current are shown in Fig-9. The variation of capacitor voltages during disabling and enabling of control is shown in fig.-9.

For the three-level inverter, the phase current FFT and phase voltage FFT are shown in the fig-9. The total harmonic distortion (THD) of the phase current and phase voltage are 2.56% and 44.3% respectively. When compared to the two-level inverter, the THD is reduced.

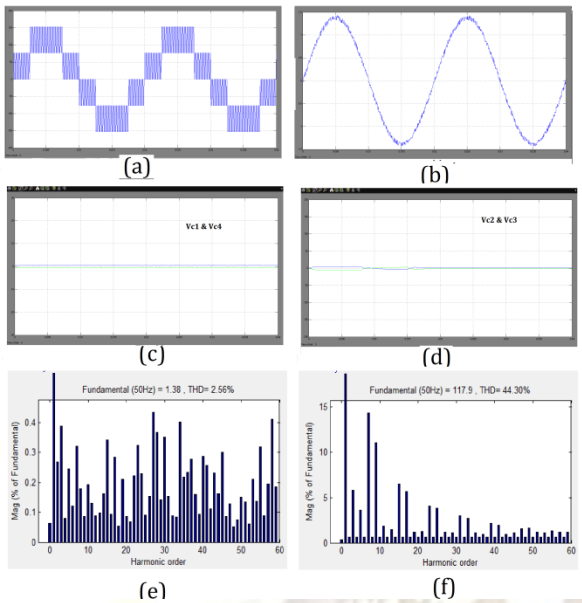

Fig-9 (a)Phase Voltage & (b)Current waveforms for the three-level operation
(c) & (d) Variation of capacitor voltages during disabling and enabling of control
(e) & (f) Spectra of the phase current and phase voltage.

FOUR LEVEL INVERTER:

In four level inverter, the switching states have no effect on the DC link capacitor voltages and they are not creating any unbalance in capacitor voltages. The voltage levels are 0, Vdc/3, 2Vdc/3 and Vdc.

For four level inverter, the phase voltage and phase current are shown in Fig-10. The variation of capacitor voltages during disabling and enabling of control is shown in fig.-10.

For the four-level inverter, the phase current FFT and phase voltage FFT are shown in the fig-10. The total harmonic distortion (THD) of the phase current and phase voltage are 1.5% and 26.32% respectively. When compared to the two-level and three-level inverters, the THD for the four-level inverter is reduced.

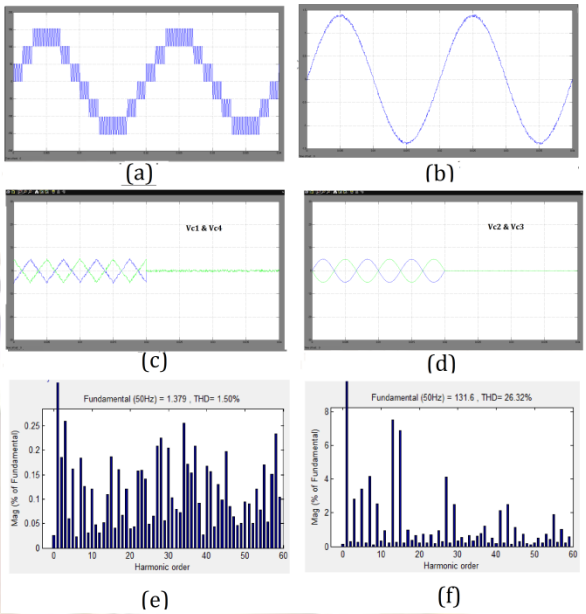

Fig-10 (a)Phase Voltage & (b)Current waveforms for the four-level operation
(c) & (d) Variation of capacitor voltages during disabling and enabling of control
(e) & (f) Spectra of the phase current and phase voltage.

FIVE-LEVEL INVERTER:

In five level inverter, the switching states are not creating any unbalance in capacitor voltages and they have no effect on the DC link capacitor voltages and they. The voltage levels are 0, 3Vdc/4, Vdc/2 , Vdc/4 and Vdc.

For five level inverter, the phase voltage and phase current are shown in Fig-11. The variation of capacitor voltages during disabling and enabling of control is shown in fig.-11.

For the five-level inverter, the phase current FFT and phase voltage FFT are shown in the fig-11. The total harmonic distortion (THD) of the phase current and phase voltage are 0.19% and 20.93% respectively. When compared to the two-level, three-level and four-level inverters, the THD for the five-level inverter is reduced.

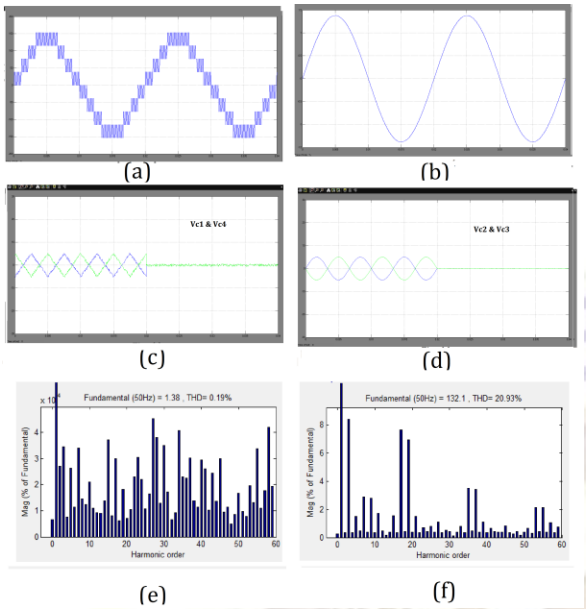

Fig-11 (a)Phase Voltage & (b)Current waveforms for the four-level operation
(c) & (d) Variation of capacitor voltages during disabling and enabling of control
(e) & (f) Spectra of the phase current and phase voltage.

Hence the total harmonic distortion is reduced, when the levels of the inverter can be increased. Therefore the comparison of the multilevel inverters is given in the table-IV. The THD is completely eliminated when the levels are increased.

Table-IV Comparison of THD

S.No.	Level of the Inverter	THD (Current)	THD (Voltag
1.	Two-Level Inverter	3.75%	116.90
2.	Three-Level Inverter	2.56%	44.30
3.	Four-Level Inverter	1.50%	26.32
4.	Five-Level Inverter	0.19%	20.93

VI CONCLUSION

A five-level inverter for the open-end winding IM drive is developed in such a manner that both common mode voltage elimination and DC-link capacitor voltage balancing are achieved, across the entire modulation range, using only the switching state redundancies. An open–end winding configuration is used for the motor and the motor is fed from both ends with multiple inverter structure, realized by cascading a three-level inverter with two two-level inverters. In the considered configuration the two two-level inverters are shared by the two three-level inverters at both ends of the motor stator winding. This will make the power circuit simpler to fabricate, when compared to any of the other existing topologies.

The simulation results using MATLAB are confirmed the capability of the developed scheme to provide the balancing of the DC-link capacitor voltages and CMV elimination for the entire range of operation, using only the switching state redundancies. The presented multi-level inverter-fed scheme can be extended to other structures with a higher overall number of levels by further cascading the conventional inverter structures.

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