

Design of MULTIPLEXER using CMOS Ternary Logic

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Abstract:-This paper presents design of 3-valued Multiplexer based on simple ternary gates. We proposed new ternary logic gates like inverter, and gates. These gates are used to design simple combinational circuit which is multiplexer with the help of transmission gate. These proposed ternary logic gates and multiplexer are verified by simulation and appear to have very low power dissipation. Also the simulation result shows that proposed ternary circuits have more desirable characteristics than conventional ternary circuits.

Keywords:-logic, Ternary, Multiplexer.

I. INTRODUCTION

A ternary, three-valued or trivalent logic (sometimes abbreviated 3VL) is any of several multi-valued logic systems. The ternary that is "three valued" has more advantages over binary logic in the design of digital systems [1], [2]. The main advantage of ternary is since each wire can transmit more multi-valued logic information than binary also reducing chip size area. Because of the less estimation interconnection cost it receives more attention than others [3]. The arithmetic operations and logical operation at higher speed can be done using ternary. Implementation of digital system with these advantages achieved using VLSI and it has very simple electronic design implementation technique [4]. Some basic circuits have been proposed in the literature and as a result several realizations of basic ternary gates have been proposed in the literature [5]. These proposed ternary gates have been useful for the design of "digital system" [6], such as the implementation of the combinational design like multiplexer, half adder. $(3N - 1)/2$ T-gates are required for the implementation of combinational logic circuit, as was demonstrated in [7] but it has some disadvantage which is, as number of gates more, the design of digital system become more complex. To overcome this disadvantage we have proposed the new ternary design based on MOS technology like INVERTER, AND gates which can be helpful for the design of digital system like multiplexer. The proposed circuits are shown to have some significant advantages relative to other ternary circuits based on the T-gate like low power dissipation, reduced propagation delay, and also reduced component count. Because of these several advantages these ternary logic have been used in several

important field like communication, digital signal processing. As is demonstrated in [8], this is an application where a significant advantage can be gained by using ternary digital hardware, namely, an increased maximum sequence length can be achieved without increasing the complexity of the digital hardware.

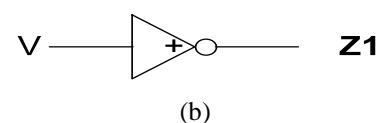
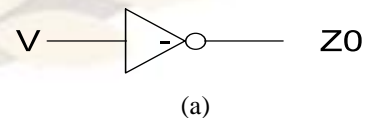
II. TERNARY LOGIC GATES

In a ternary system, three logic levels are used (1, 0.5, 0) corresponding to high, middle and low voltage. The design of digital hardware system is concerned some of the important design are the inverter, AND gate and NAND gate. In this paper, we have proposed some new ternary implementations of digital system like inverter, AND gate and NAND gate. Consider the logic for voltage level is shown in Table 1.

A. 1) Ternary Inverter with Resistor

The symbolic representation of the negative ternary inverter (NTI), positive ternary inverter (PTI) and standard ternary inverter (STI) is shown in fig.1. The three basic general type of ternary inverter with resistor has one input V and three outputs V0, V1 and V2 which is shown in fig.2. These types of ternary CMOS inverter have been design.[9],[4]

In fig 2(a) the output V0 is 1 if the input V=0 & V0 is 0 if the input V≠0. This device operate as a negative ternary inverter. The output V1 of the positive ternary inverter in fig.2 (b) is 1 if V≠1 and V1 is 0 if the V= 1. In fig.2 (c) the output of the standard ternary inverter name as V2 is 1-V. It means V2 is 1 if V is 0 and V2 is 0.5 if V is 0.5 and V2 is 0 if V is 1.



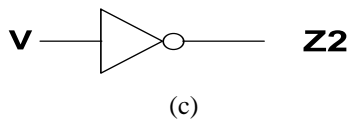


Figure 1: Ternary Inverters (a) Symbol for NTI (b) Symbol for PTI (c) Symbol for STI.

The logic value 0, 1/2 and 1 correspond to the voltage level -VCC, 0 and +VCC respectively. Implementations of these conventional inverters have been proposed by Mouftah and Jordan and Mouftah and Smith, which are shown in Fig.2. As shown in Fig. 2(c), the output V1 is 0V when both transistors are on. Hence, the total static power dissipation in resistors R1 and R2 is given by

$$P2 \cong VCC^2 \left\{ \frac{R1 + R2}{R1R2} \right\}$$

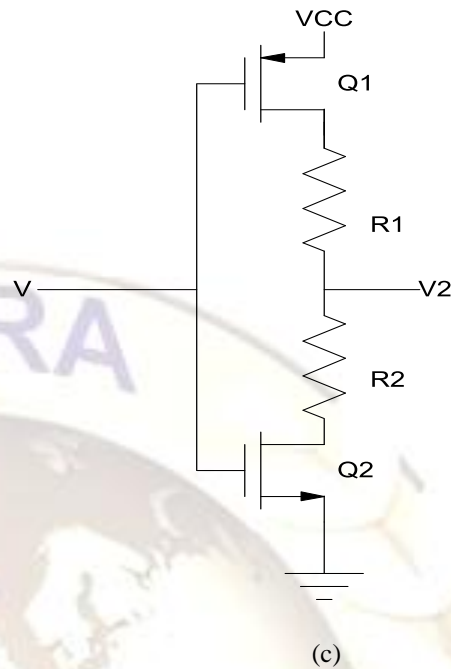
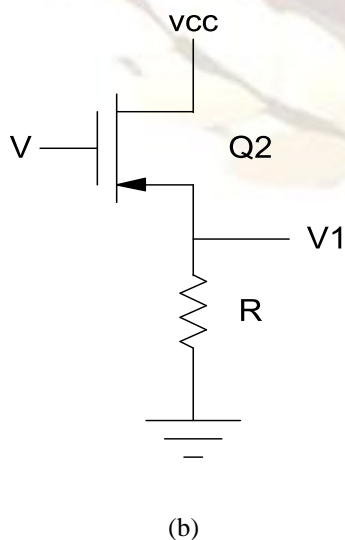
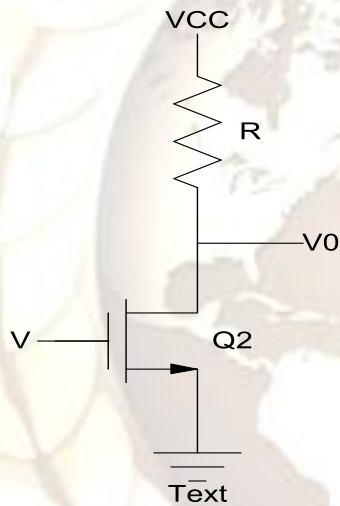


Figure 2: CMOS Ternary Inverters with Resistor (a) For NTI (b) For PTI (c) For STI.

Also, the static power dissipation for the NTI and PTI circuits when transistor in Fig. 2(a) or in Fig. 2(b) is on [10]. So the static power dissipation is given by

$$P0 = P1 \cong \frac{4VV^2CC}{R}$$

A.2) Proposed Ternary Inverter

A proposed STI circuit is shown in Fig.3 (c), the proposed STI circuit whose power dissipation is very low. The input V of the proposed STI is V_TRAN=PWL(time,0ns,0v,20ns, 0v, 39ns,0v,40ns,0.5v,60ns,0.5v,79ns,0.5v,80ns,1v,100ns,1v). The transistors Q1 and Q2 are p-channel and N-channel enhancement type and Q3 and Q4 are P-channel and N-channel depletion type.

If the input level is -VCC or +VCC, then Q1 and Q2 of PTI will be on and Q1 and Q2 of NTI will be off and P2=0. Because of this the static power dissipation in the proposed circuit is equal to zero for every input logic levels. The proposed NTI and PTI circuits are shown in Fig. 3(a) and (b). The input given to the V is Vt PWL. The W/L of Q1 and Q2 of NTI has (2.3/1) um and (1/1) um respectively. Whereas Q1 and Q2 of PTI have W/L for (2.3/1) um and (1/1) um respectively

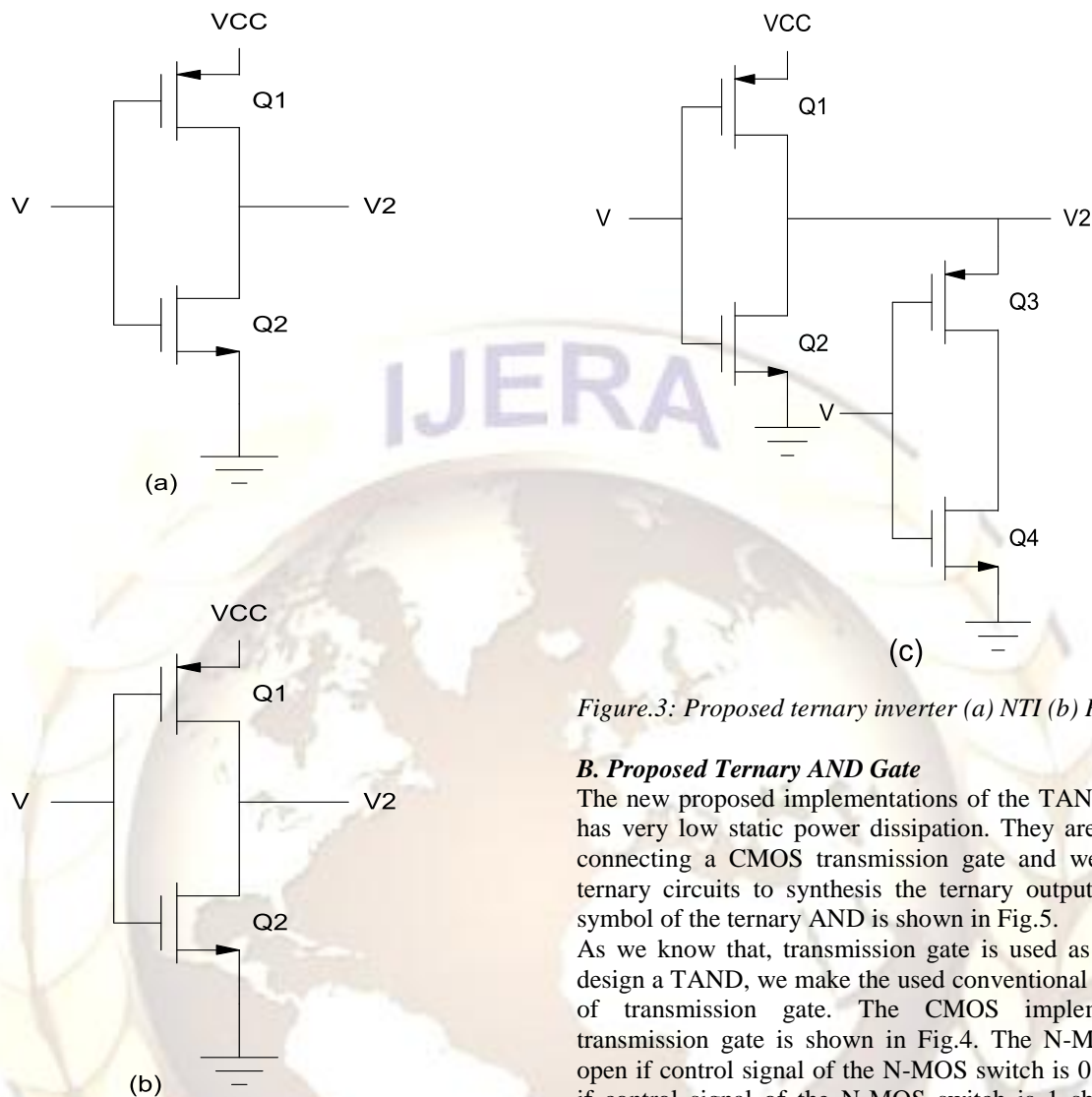


Figure.3: Proposed ternary inverter (a) NTI (b) PTI (c) STI.

B. Proposed Ternary AND Gate

The new proposed implementations of the TAND gate which has very low static power dissipation. They are designed by connecting a CMOS transmission gate and we used newer ternary circuits to synthesis the ternary output. The logical symbol of the ternary AND is shown in Fig.5.

As we know that, transmission gate is used as a switch. To design a TAND, we make the used conventional binary design of transmission gate. The CMOS implementation of transmission gate is shown in Fig.4. The N-MOS switch is open if control signal of the N-MOS switch is 0 and is closed if control signal of the N-MOS switch is 1 shown in Fig.4 (a). Similarly for P-MOS switch of is open if control signal of the P-MOS is 1 and is closed if control signal of P-MOS is 0 shown in Fig.4 (b).

From Fig.4 (e) and 4(f), input of the N-MOS switch is denoted as C and \bar{C} for P-MOS switch. The input to both is available through the binary inverter. If the input of the inverter logic 1 and inverted output \bar{C} is 0. C and \bar{C} given to N-MOS and P-MOS switch respectively which is shown in Fig.4 (e). If the input of the inverter C is 0 and inverted output \bar{c} is 1. C and \bar{C} given to N-MOS and P-MOS switch respectively which is shown in Fig.4 (f).

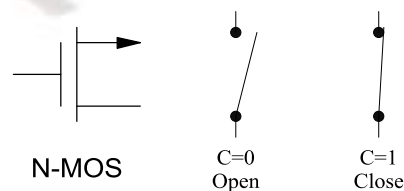


Figure.4 (a)

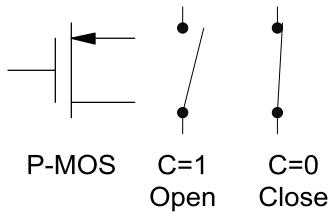


Figure 4(b)

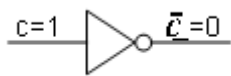


Figure.4(c)

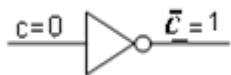


Figure 4(d)

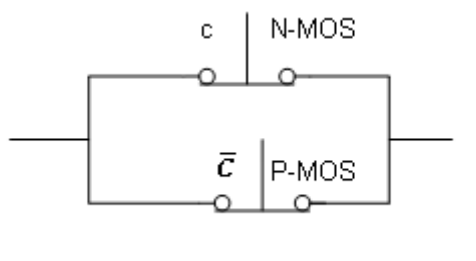


Figure.4 (e)

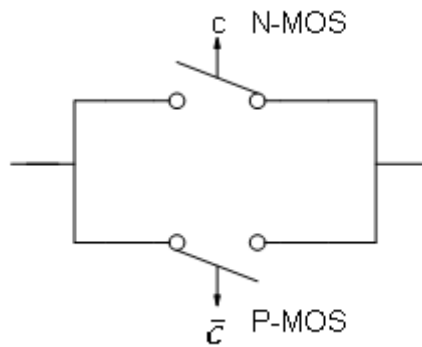


Figure 4(f)

The symbolic representation of the proposed TNAND with input namely V1&V2 is shown in Fig.5.

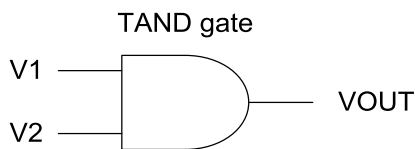


Figure.5: Symbol for TAND Gate

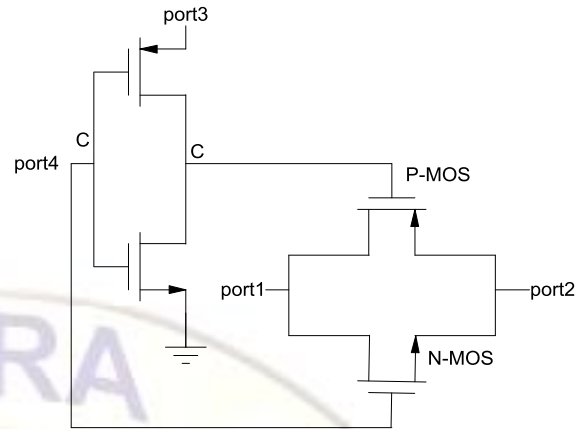


fig. 4(g)Transmission gate

The truth tables for the TAND are given in Table 1. [11]

TABLE 1

V1	V2	V1 TAND V2
0	0	0
1/2	0	0
1	0	0
0	1/2	0
1/2	1/2	1/2
1	1/2	1/2
0	1	0
1/2	1	1/2
1	1	1

As shown in Fig.6 to port 1 the input V1 is given which is $V_TRAN=PWL(\text{time},0\text{ns},0\text{V},6\text{ns},0\text{V},6.9\text{ns},0\text{V},7\text{ns},0.5\text{V},13\text{ns},0.5\text{V},13.9\text{ns},0.5\text{V},14\text{ns},1\text{V},20\text{ns},1\text{V},20.9\text{ns},0\text{V},21\text{ns},0\text{V},25\text{ns},0\text{V},25.9\text{ns},0\text{V},26\text{ns},0.5\text{V},33.9\text{ns},0.5\text{V},34\text{ns},0.5\text{V},39.9\text{ns},1\text{V},39\text{ns},1\text{V},40\text{ns},0\text{V},46.9\text{ns},0\text{V},47\text{ns},0.5\text{V},53.9\text{ns},0.5\text{V},54\text{ns},1\text{V},60\text{ns},1\text{V})$ and also input to port 2 is $V_TRAN =PWL(\text{time}, 0\text{ns}, 0\text{V}, 20.9\text{ns}, 0\text{V}, 21\text{ns}, 0.5\text{V}, 39.9\text{ns}, 0.5\text{V}, 40\text{ns}, 1\text{V}, 59\text{ns}, 1\text{V})$. After applying ternary input to transmission gate, output is taken at port 2 that is VOUT. To port 3 I_PROBE is connected to measure the power dissipation.

This new proposed implementations of TAND have very low static power dissipation measure by the I_PROBE.

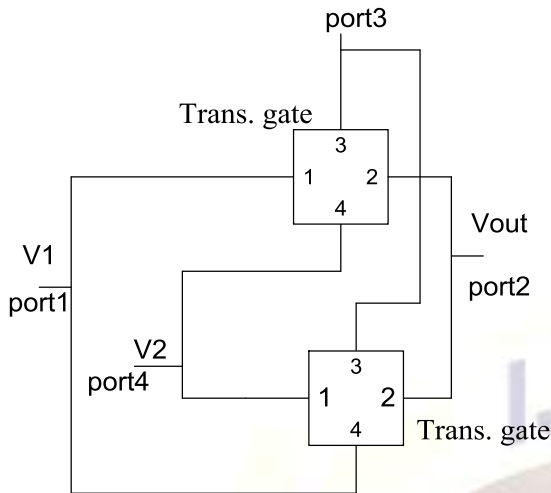


Figure 6: Ternary AND Gate

III. Ternary Multiplexer

It is a most important standard logic design. It is one of the special designs of combinational circuit which has several input and single output like 2:1, 4:1 and 8:1 multiplexer. As we can see in Fig.7 to select respective input we make the use of select line. Fig7 shows block diagram of a multiplexer with “n” input and single output.

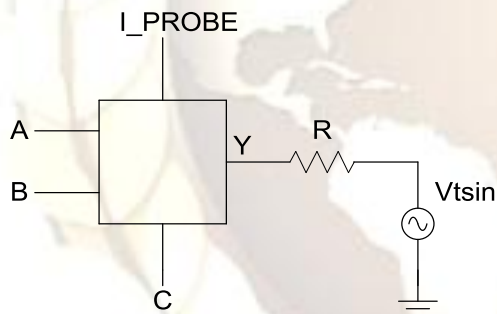


Figure 7: Proposed Ternary MUX.

TABLE 2

Select line (C)	Output(Y)
0V	A
0.5V	Z
1V	B

The input A is V_TRAN=PWL(time, 0ns,0V,6.9 ns,0V,6.9ns ,0.5V,13.9ns,0.5V,14ns,1V,20ns,1V,20ns,0V,26ns,0V,26.1 ns, 0.5V,32.9ns,0.5V,33ns,1V,40ns,1V,40ns ,0V). Also the input B is V_TRAN=PWL(time,0ns,0V,46.9ns,0V,47ns,0.5V,53.9n

s,0.5V,54ns,1V,59.9ns,1V,60ns,0V,21ns,0V,26ns,0V,26ns,0.5 V,32ns,0.5V,32ns,1V,40ns,1V,40ns,0V) and to select corresponding input we have select line C which is V_TRAN=PWL (time,0ns,0V,20ns,0V,20ns,0.5V,40ns,0.5V,40ns,1V,59ns,1V) .As per voltage level of the select line corresponding input select ,which is shown in simulation result.

IV. Simulation Result of the Ternary Logic Design

We designed a new proposed scheme to adapt ternary design. We have shown the implementation of ternary logic like Inverter, AND. These basic logic gates are used to make combinational design like half adder, half subtractor, multiplexer etc. These ternary gates are implemented with voltage-driven CMOS circuits. In the simulation, logical value 0, 1/2 and 1 correspond to 0V, 0.5V, and 1V, respectively.

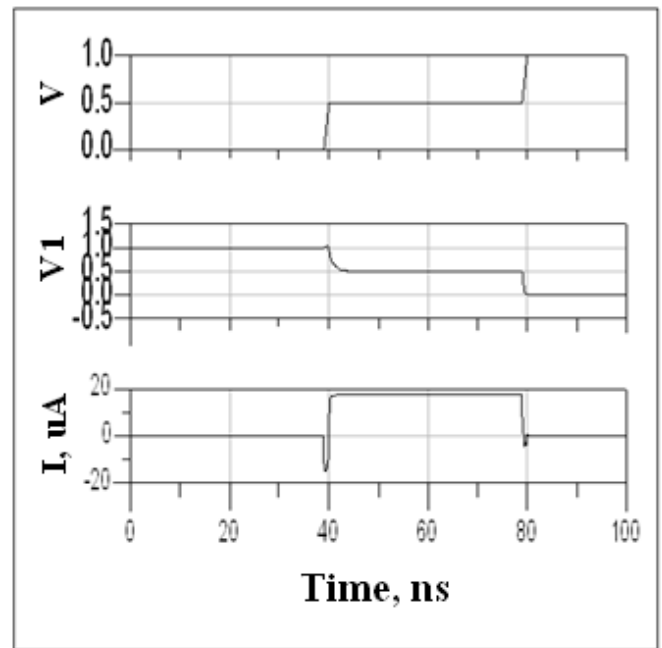


Figure 8: Simulation Result of the Proposed Ternary Inverter.

As we can see from the Fig.8, when input of the ternary inverter is 0, 0.5 and 1 then the inverted ternary output is 1, 0.5 and 0 respectively. From the graph, the power dissipation of the proposed ternary inverter shown is very small as compared to the conventional ternary inverter [3]. The static power dissipation of proposed ternary circuit is negligible because either N-MOS is off or P-MOS is off for the output which is 0, 0.5 or 1.

From Simulation result of the TAND which is shown in Fig. 9 the output of TAND is 0 if one of the input of TAND is 0.the output of TAND is 0.5 if one input is 0.5 and other input is 1 out of both. Output is same as input if both input are same.

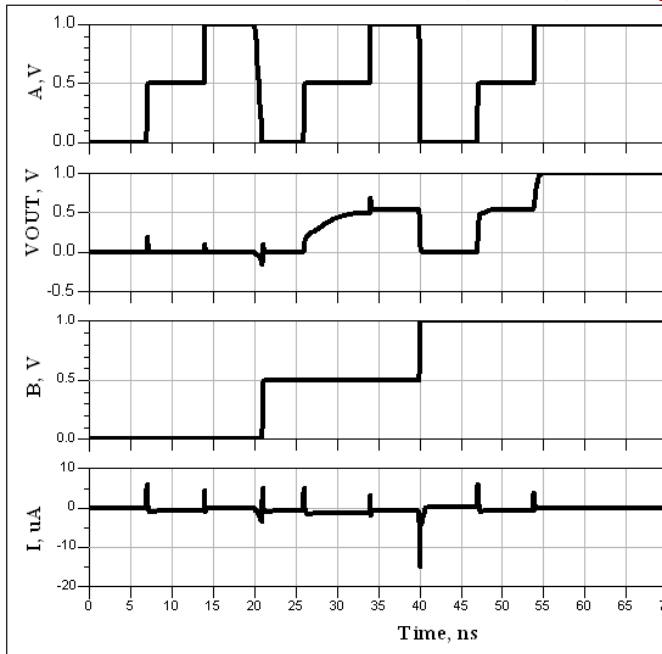


Figure 9: Simulation Result of TAND Gate

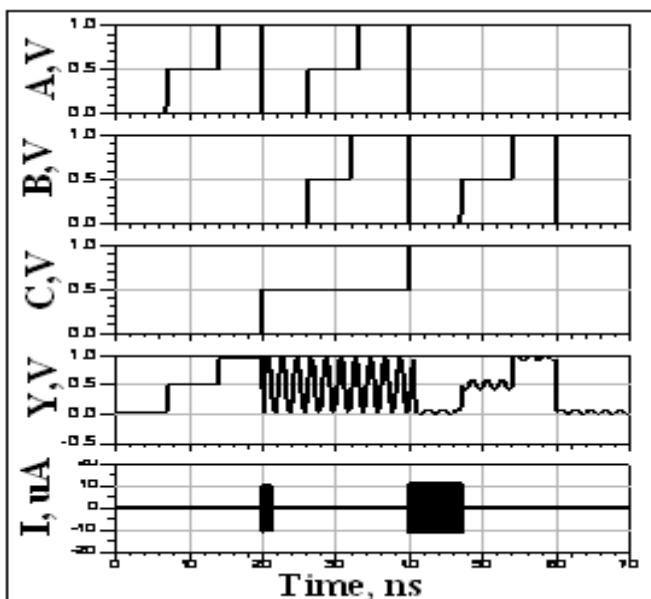


Figure 10: Simulation Result of TMUX.

As we can see in graph of ternary MUX which is shown in Fig.10 then input A of the TMUX is selected, if the voltage level of select line C is 0V. The voltage level of C is 0.5V then output goes in high impedance state. The main advantage of the TMUX is to achieve high impedance state using ternary logic. The input B is selected if the voltage level of the C is 1V. So according to select line C corresponding input is selected and accordingly output of TMUX gets displayed. As shown in fig. 10, using I_PROBE we show the power dissipation which is too negligible.

V. CONCLUSION

In this section, first we have proposed new ternary INVERTER, AND gate then we proposed combinational circuit which is MULTIPLEXER. This ternary system is capable of transmitting more information as compare to binary system. The proposed ternary design offers most important advantage that is it has very low power dissipation relative to conventional circuits and that lead to significant reductions in propagation delay. The procedure for designing C MOS ternary combinational circuits can be used to construct CMOS ternary sequential circuits. Ternary logic offers several advantages in the particular area like communication, memory and digital signal processing

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