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Implementation Of Low Power High Performance Combinational Circuits Using Output Prediction Logic

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ABSTRACT
Output Prediction Logic (OPL) is a recently developed circuit technique that is twice as fast as domino logic, and several times faster than Static CMOS logic .Output Prediction Logic (OPL), a technique that can be applied to conventional CMOS logic families to obtain considerable speedups. When applied to static CMOS, OPL retains the restoring character of the logic family. Different cmos logics styles have been compared with respect to power consumption, delay, energy efficient and robust to noise and variation .Output prediction logic Speedups of 2X to 3X over conventional static CMOS are demonstrated for a variety of circuits, ranging from chains of gates, to data path circuits, and to random logic benchmarks. we show that OPL differential CMOS is more than 40% faster than the single-rail OPL-dynamic logic family. we believe it will scale much better than domino with future processing technologies.

Keywords – **output predict logic (OPL), low power (LP), delay locked loop (DLL)**

I. INTRODUCTION
The increasing demand for low-power very scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level. At the circuit level, considerable potential for power savings exists by means of proper choice of a logic style for implementation combinational circuits. This is because all the importance parameters governing power dissipation switching capacitance, transition activity, and short –circuit currents –are strongly influenced by the chosen logic style. Depending on the application, the kind of circuit to be implemented, and the design technique used, different performance aspects become important In the past, the parameters like high speed, small area and low cost were the major areas of concern, whereas power Considerations are now gaining the attention of the scientific community associated with VLSI design. In recent years, the growth of personal computing devices (portable computers and real time audio and video based multimedia applications) and wireless communication systems has made power dissipation a most critical design parameter. In the absence of low-power design techniques such applications generally suffer from very short battery life, while packaging and cooling them would be very difficult and this is leading to an unavoidable increase in the cost of the product. In multiplication, reliability is strongly affected by power consumption. Usually, high power dissipation implies high temperature operation, which, in turn, has a tendency to induce several failure mechanisms in the system.

Dynamic circuit families such as domino are commonly used in today's high-performance microprocessors for obtaining timing goals that are not possible using static CMOS circuits. Their increased performance is due to reduced input capacitance, lower switching thresholds, and circuit implementations that typically use fewer levels of logic due to the use of efficient and wide complex gates. However, dynamic circuits have notable disadvantages. In the case of domino, logic must be mapped to a unate network, which usually requires duplication of logic. Perhaps the main disadvantage going forward is its increased noise sensitivity (compared to static CMOS). The only way to increase its noise margin is to sacrifice some of its performance gain How to retain the good attributes of static CMOS, namely high noise immunity and easy technology mapping, while obtaining greater speed is an elusive goal.

Output prediction logic (OPL) is a new technique that can be applied to a variety of inverting logic families to increase speed while retaining the attributes of the underlying family. OPL relies on the alternating nature of logical output values for inverting gates on a critical path. That is, for any critical path, the logical output values of the gates along that path will be alternating ones and zeros. By correctly predicting exactly one half of the gate outputs, OPL obtains

significant speedups (at least 2X) over the underlying logic families (e.g. static CMOS, Pseudo-nMOS and dynamic logic).

II. RELATED WORK

Integrated circuits contain a plurality of signal paths which essentially carry information (data and control signals) across the circuit. Each signal path is made up of a plurality of circuit elements connected together serially (i.e., in series). Each of these signal paths experiences a delay as signals travel across the circuit. These signal path delays occur due to the time required for signals to propagate through each of the plurality of circuit elements from the input to the output of the signal path. Each circuit element has its own switching delay known as the switching delay of a circuit element. This circuit element switching delay is the time required for a circuit element to switch logic states from either a high-to-low logic state (logic 1→0) or from a low-to-high logic state (logic 0→1). The path switching delay is determined by the accumulation of time it takes for a signal to pass through each of the circuit elements in a particular path. This time, in turn, is based on the total switching delay of each circuit element in the path. Paths with the highest number of combined switching delays of circuit elements are known as speed paths or critical paths. These critical paths dictate how fast an integrated circuit can operate. The maximum frequency an integrated circuit can operate at depends directly on how fast signals can propagate across the worst-case critical paths

2.1 Dynamic circuit families such as domino are commonly used in today's high-performance microprocessors

1. Increased performance due to:
2. Reduced input capacitance
3. Lower switching thresholds
4. Fewer levels of logic (due to the use of wide gates)
5. Dynamic logic yields average speed improvement of 60% over

Dynamic CMOS circuits are defined as those circuits which have an additional clock signal inputs along with the default combinational circuit inputs of the static systems. Dynamic systems are faster and efficient than the static systems. MOS does not require the capacitances to be connected externally; thereby CMOS dynamic systems are very advantageous. However, they suffer from some major drawbacks. They are:

1. Charge Leakage Issues
2. Charge sharing Problems
3. Clock Skew Difficulties

1. Charge Leakage Issues - The operation of a dynamic gate depends on the storage of information on the MOS capacitors. The source-drain diffusions form parasitic diodes with the substrate. If source (or drain) is connected to a capacitor CL with some charge on it, the charge will be slowly dissipated through the reverse--biased parasitic diode. The leakage current is a function of temperature. The current is in the range 0.1nA to 0.5nA per device at room temperature. The current doubles for every 10°C increase in temperature. Moreover, there will be some sub-threshold leakage current. Even when the transistor is OFF and the current can still flow from the drain to source. This component of current increases when the gate voltage is above zero and approaches the threshold voltage, this effect becomes more pronounced. A sufficiently high threshold voltage Vt is recommended to alleviate this problem. The charge leakage results in gradual degradation of HIGH level voltage output with time, which prevents it to use a low clock rate. This makes it unattractive for many applications, such as toys, watches, etc, which are operated at lower frequency to minimize power dissipation from battery. As a consequence, the voltage on the charge storage node slowly decreases. This needs to be compensated by refreshing the charge at regular intervals.

2. Charge sharing Problems - Dynamic circuits suffer from charge sharing problem because of parasitic capacitances at different nodes of a circuit. This result is lower voltage levels at the output terminals. In such circuit designs redistribution of charges take place leading to charge sharing problems. Charge sharing problem can be solved by introducing a delay circuit in the path of the clock that will compensate for the discharge delay between the first and second stage of the dynamic circuit. It may be noted that the delay is a function of the complexity of the discharge path. This 'self-timing' scheme is fairly simple and often used is CMOS PLA and memory design. Also the use of NORA and DOMINO circuits could solve the problem. - 3. Clock Skew Problem - It is common to use several stages of dynamic circuits to realize a Boolean function. Although same clock is applied to all these stages, it suffers delay due to resistance and parasitic capacitances associated with the wire that carry the clock pulse. This delay is approximately proportional to the square of the length of the wire. As a result, different amounts of delays are experienced at different points in the circuit and the signal state changes that are supposed to occur in coincidence may never actually occur at the same time. This is known as clock skew problem and it results in hazard and race conditions.

The path switching delay is the accumulation of all switching delays of each of the inverters. This

path switching delay occurs not only for inverters, but for any inverting logic functions such as NAND gates, NOR gates, AOI (and-or-invert), OAI (or-and-invert), and etcetera. Switching delays may be optimized in order to facilitate a signal propagating along a critical path from input to output with reduced switching delays. Conventionally, circuit path delays are optimized in two ways. The first way is to reduce the number of logic stages by combining multiple stages into a single stage. The second way is to reduce the amount of switching delay that a particular stage requires. Such reduction in delay can be accomplished using several techniques known in the art such as transistor resizing, reducing output load, improving input transition time, breaking the complex cells into simpler cells, and etcetera. Other Methods to reduce the switching delays of the logic gates in a path include pre charging logic gates (i.e., dynamic logic) and skewing logic gates through transistor resizing. In the case of using dynamic logic, a method for optimizing switching delays of a path in an integrated circuit using dynamic logic gates includes using output prediction logic (OPL) circuits. In OPT circuits every logic gate includes dynamic logic with a pre charge circuit. FIG. 1B illustrates a method for optimizing switching delay of logic gates in a circuit path using output prediction logic (OPL) according to the prior art . However, in OPL circuits there is a somewhat cumbersome requirement of clock signal generation with a very small delay difference between two consecutive logic stages that results in the need to design each clock path with some precision. The generation of clocks with such small delay difference is not straight forward and requires complicated techniques like Delay Locked Loops (DLLs) and carefully designed clock networks. Secondly, the need to supply every stage with a separate clock signal adds to a substantial clocking overhead in the design that requires extra metal resources and careful routing. Also, there are serious concerns about sensitivity to process variation and noise since any significant glitching variation could trigger a regenerative cascading effect across the path. These issues and possibly others may give rise to adoption challenges among the IC design community for this technique.

III. PROPOSED LOGIC STYLE

In static CMOS logic, every gate is an inverting logic gate. Because of this inverting property, every output on a critical path must fully transition from 0 to 1, or 1 to 0 in the worst case. This is shown in Fig. 1, where we assume the primary input transitions high. This is why static CMOS is inherently slow. **A** circuit designer must take into account this worst-case delay scenario for a static CMOS critical path.

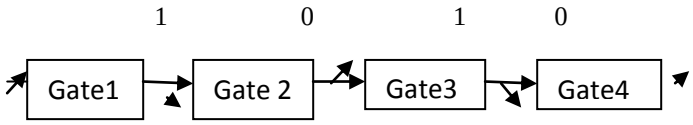


Fig.1 static cmos worst case-behavior

Output prediction logic (OPL) greatly reduces the worst-case behavior of a critical path .OPL predicts that every inverting gate output on a critical path will be a logic one after the transition are completed .since all gates are inverting, as in static CMOS the OPL predictions will be correct exactly one-half the time .every other gate will not have to take any transition

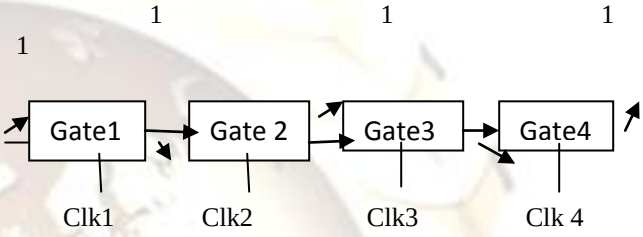


Fig.2 OPL predicting ones

There is, however, a key problem with this idea. A one at every output (and therefore input) is not a stable state for an inverting gate. The one will erode (possibly going to zero) in the latter gates of a critical path. The solution to this problem is to tri-state each gate with a clock, in which case ones at inputs and a one output is no longer a contradiction for an inverting gate. The gates remain tri-stated until their inputs are ready for evaluation. In this manner, predicted output values are maintained until new input values dictate otherwise Successive clocks are delayed by a clock separation as shown in Fig. ***3.***

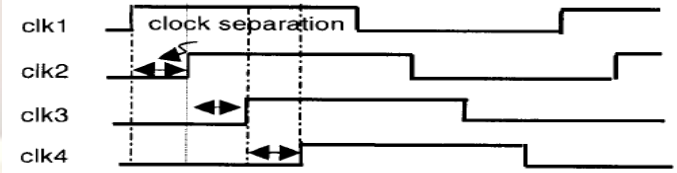


Figure 3. Clocking.

3.1 Output Prediction Logic

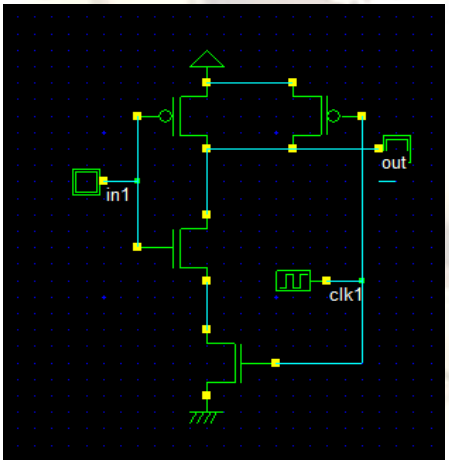
Output prediction logic (OPL) is a new technique that can be applied to a variety of inverting logic families to increase speed while retaining the attributes of the underlying family. OPL relies on the alternating nature of logical output values for inverting gates on a critical path.

That is, for any critical path, the logical output values of the gates along that path will be alternating ones and zeros. By correctly predicting exactly one half of the

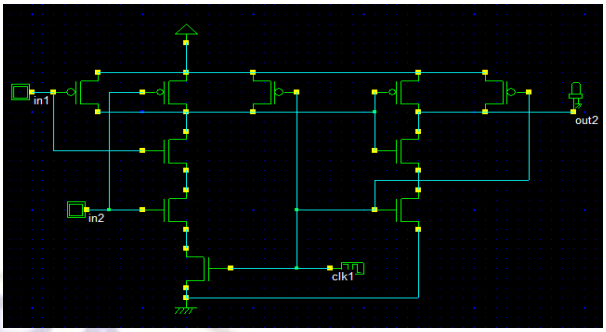
gate outputs, OPL obtains significant speedups (at least 2X) over the underlying logic families (e.g. static CMOS, pseudo-nMOS and dynamic logic). When applied to static CMOS, OPL yields circuits that are typically 2 to 3 times faster than conventional static CMOS implementations. Although OPL employs clocks, OPL-static is inherently restoring logic and has the same noise margins as Conventional static CMOS. OPL-static is also highly tolerant to clock skew, guaranteeing functionally correct results regardless of skew. Additionally, OPL-static uses the same synthesis tools as static CMOS (e.g. Synopsys). OPL can be applied to the same net lists as conventional static CMOS with a simple cell-for-cell substitution. For the efficient implementation of wide NOR gates, designers often choose gates from pseudo-nMOS or dynamic logic families. OPL can be applied to these families as well. For example, a CLA adder implementation using OPL-pseudo-nMOS for wide-input NORs obtained a speedup of 5.4X over an optimized static CMOS implementation. These speedups were obtained while employing very conservative noise margins.

we introduce OPL and show how it is applied to static CMOS circuits. we apply OPL to pseudo-nMOS and dynamic circuit styles. A means of generating the required clocks is outlined in quantifies the performance enhancement obtained with OPL when applied to chains of gates, a CLA adder and random logic benchmarks.

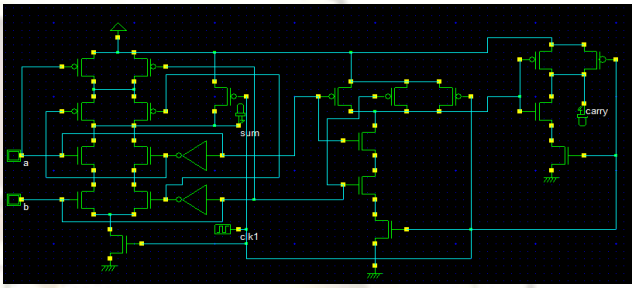
IV. FIGURES



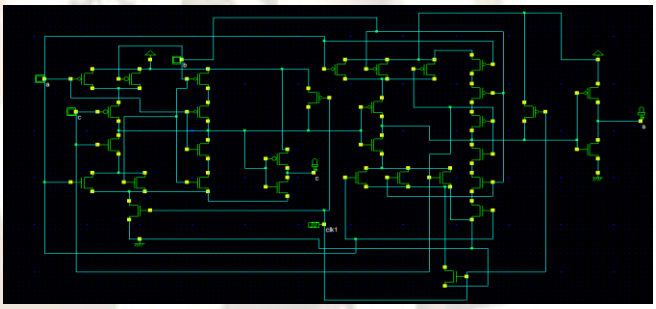
OPL inverter



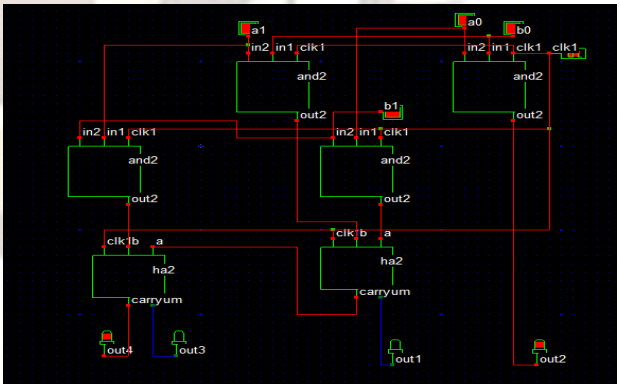
OPL and gate



OPL half adder



OPL full adder

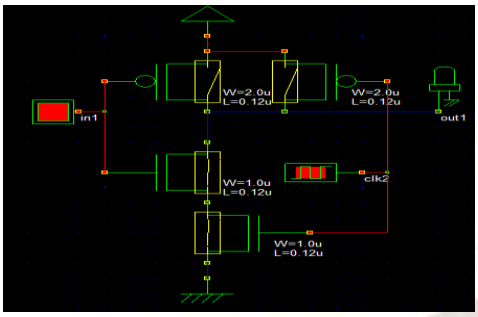


2×2 multiplier using OPL logic

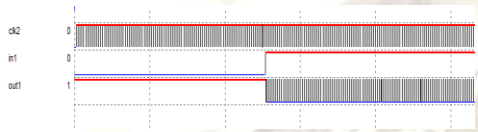
5.CURRENT RESULTS

Below experiment results of implementation of combinational circuits using output prediction using micro wind tool 3.5.

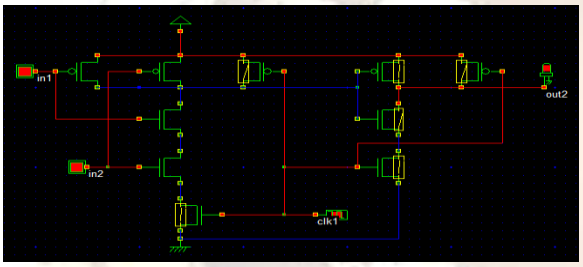
6.SIMULATION RESULTS



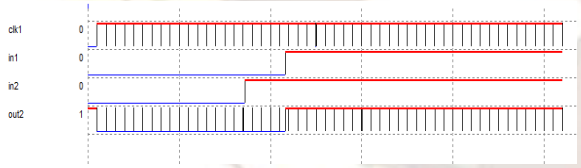
OPL inverter



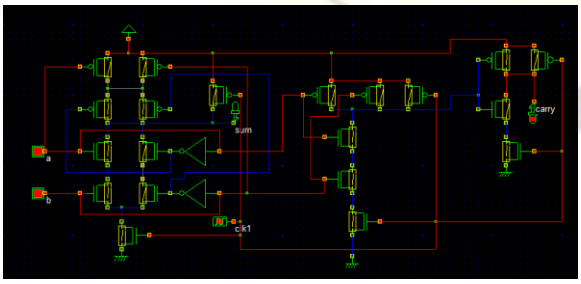
waveform of inverter



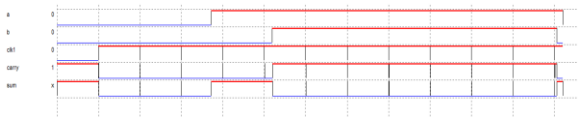
OPL and gate



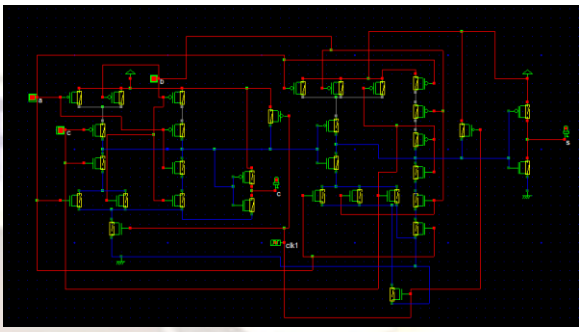
Waveforms of OPL and gate



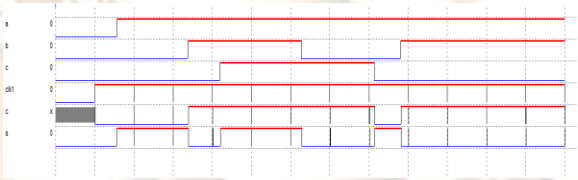
OPL half adder

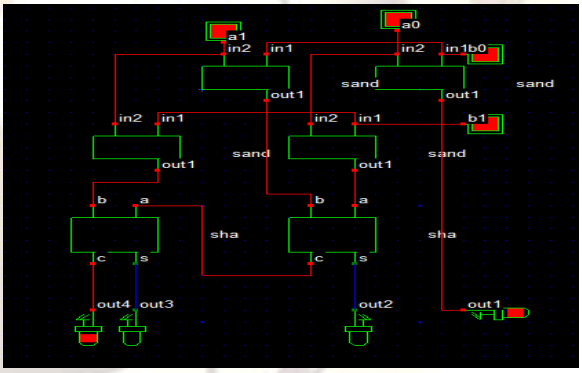


Wave forms of OPL half adder

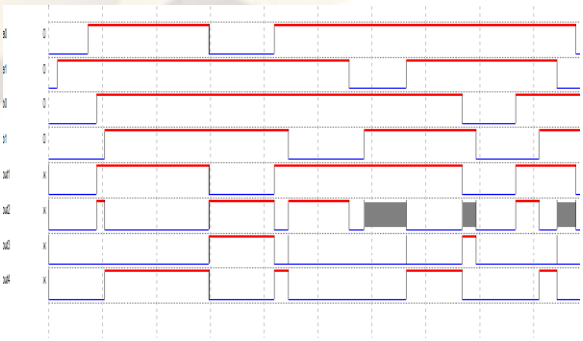


OPL full adder





2×2 multiplier using OPL



Waveforms of 2×2 multiplier

V. CONCLUSION

It has been observed that output prediction logic (OPL) logic design style exhibit better characteristics (speed and power) as compared to other design styles. So, OPL logic style can be used where portability and high speed is the prime aim. Where, OPL consumes the lowest power among the three. a technique that can be applied to conventional CMOS logic families obtain considerable speedups. Speedups of 2X to 3X over conventional static CMOS were demonstrated for a variety of circuits, ranging from chains of gates, to data path circuits, and to random logic benchmarks. Whereas static cmos worst case delay problem, so in this OPL logic can be reduced worst case delay.

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