

Design of a Low Power Operational Amplifier by Compensating the Input Stage

Suparshya Babu Sukhavasi¹, Susrutha Babu Sukhavasi¹, Dr. Habibulla Khan², S R Sastry Kalavakolanu³, Vijaya Bhaskar Madivada³, Lakshmi Narayana Thalluri³

¹ ASSISTANT PROFESSOR, Department of ECE, K L University, Guntur, AP, India

² PROFESSOR & HEAD, Department of ECE, K L University, Guntur, AP, India

³ M.TECH-VLSI STUDENT Department of ECE, K L University, Guntur, AP, India.

ABSTRACT:

The trend towards low voltage low power silicon chip systems has been growing quickly due to the increasing demand of smaller size and longer battery life for portable applications in all marketing segments including telecommunications, medical, computers and consumer electronics. The supply voltage is being scaled down to reduce overall power consumption of the system.

The objective of this project is to implement the full custom design of low voltage and low power operational amplifier for the Biomedical and Telecommunications applications. This project presents the operational amplifier schematic implementation, simulation results and the layout with the 0.18 μ m technology. The operational amplifier is used to implement the ADC circuit.

This project will briefly outline the performance of operational amplifier (input stage compensated).

Keywords - CMRR, MOSFET, OTA, PSRR, Slew Rate, SNR.

1. Introduction:

Improvements in processing have pushed scaling of device dimensions persistently over the past years. The main drive behind this trend is the resulting reduction in IC production cost since more components on a chip are possible. In addition to device scaling, the increase in the portable electronics market is also encouraging low voltage and low power circuitry since this would reduce battery size and weight and enable longer battery life time.

Operational amplifier, which has become one of the most versatile and important building blocks in analog circuit design. There are two operational amplifiers developed. Operational transconductance amplifiers (unbuffered) have the output resistance typically very high. The other one

is the buffered amplifiers (voltage operational amplifier) typically low output resistance.

The differential transconductance stage introduced in the input of the operational amplifier and sometimes provides the differential to single ended conversion. Normally, a good portion of the overall gain is provided by differential input stage, which improves the noise and offset performance.

The second stage is typically an inverter. If the differential input stage does not perform the differential to single ended conversion, then it is accomplished in the second stage inverter. If the operational amplifier must drive a low resistance load, the second stage must be followed by a buffer stage whose objective is to lower the output resistance and maintain a large signal swing.

Bias circuits are provided to establish the operating point for each transistor in its quiescent state. Compensation is required to achieve stable closed loop performance.

In 1934 Harry Black commuted from his home in New York City to work at Bell Labs. In the middle 1960's that Fairchild released the μ A709. This was the first commercially successful IC operational amplifier, and Robert J. Widler designed it.

PARAMETER NAME	PARAMETER SYMBOL	VALUE
Input current	I_{IN}	0
Input offset voltage	V_{OS}	0
Input impedance	Z_{IN}	∞
Output impedance	Z_{OUT}	0
Gain	A	∞

Table 1: List of the basic ideal Operational amplifier assumptions

Operational Amplifier Performance parameters are Input Offset Voltage, Input Offset Current, Input Bias Current, Input Resistance, Output Voltage Swing, Common-Mode Rejection Ratio (CMRR), Power Supply Voltage Rejection Ratio (PSRR), Slew Rate, Settling Time, Phase Margin, Gain Margin, Signal-to-noise ratio.

2. Categorization of Operational amplifier's

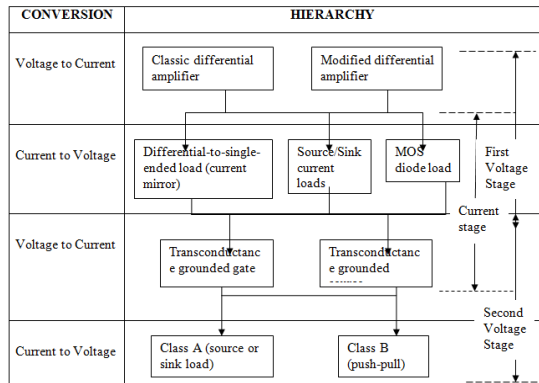


Fig 1: categorization of operational amplifier

3. Architectures of operational amplifier

The operational amplifier are basically divided into two types

1. Single stage operational amplifier
2. Multi stage operational amplifier

Single stage OP-AMP's have the characteristics are of superior frequency response, higher speed, low power, fast settling time and less design complexity. Its drawbacks are less open-loop DC gain and compatible with only low frequency.

Multi-stage OP-AMP's are mainly classified into 3 types; two stage, Folded Cascade and Telescopic.

Two-stage OP-AMP mainly consists of a cascade of Voltage to Current and Current to voltage stages. The first stage consists of a differential amplifier converting the differential input voltage to differential currents. These differential currents are applied to a current mirror load recovering the differential voltage. The second stage consists of common source MOSFET converting the second stage input voltage to current. This transistor is loaded by a current sink load, which converts the current to voltage at the output. The second stage is also nothing more than the current sink inverter.

Folded cascode architecture was developed in part to improve the input common mode range and the power supply rejection of the two stage operational amplifier. One of the advantages of the folded cascode operational amplifier is that it has a push-pull output. The operational amplifier uses cascoding in the output stage combined with an unusual implementation of the differential amplifier to achieve good input common mode range. Thus, the folded cascode operational amplifier offers self-compensation, good input common mode range, and the gain of two stage operational amplifier.

The telescopic architecture consumes less static power and also low-noise OTA. In this architecture, OTA is designed to be fully differential which doubles the effective output swing and the amount of current available for slewing and also effectively attenuate even-order harmonic distortion, substrate noise, supply noise, and common mode disturbances. One drawback in adopting a fully differential amplifier is the need for common-mode feedback.

Comparison of Multi Stage Architectures:

Architecture	Gain	Output Swing	Speed	Power	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded Cascode	Medium	Medium	High	Medium	Medium
Two Stage	High	Highest	Low	Medium	Low

Fig 2: comparison of multi-stage architectures

4. Low Voltage Low Power Structures

4.1 Input Stage:

The input stage of an operational amplifier has the task of sensing the differential input voltage. This process is disturbed by interference the signals such as offset, bias, drift, noise and common mode cross talk. The modeling of these signals has been discussed in different input topologies. The level of these additive inference signals determined the useful sensitivity of the amplifier. The design of the input stage should aim at low values of these interference signals, while the current consumption should be low, and a large portion of rail to rail range should be available for common mode signals.

The different input topologies are

1. P-channel and N-channel input stage
2. CMOS complementary input stage

4.2 Output Stage:

Classification number	Connection of upper output transistor	Connection of lower output transistor
1	VF	VF
2	VF	GA
3	GA	GA

Table 2: classification of all possible push-pull output stages

Output transistors can be generally being connected in three different ways: Firstly, in a general amplifier (GA) connection (common emitter or common source), secondly, in a voltage follower (VF) connection (common collector or common drain) and thirdly, in a current follower (CF) connection (common base or common gate).

5. OP-AMP Specifications and Design

The key criterion of this project is to operate with lower power supply and achieve large signal to noise ratio while maintaining less power consumption, low settling time, and reasonable gain. The table shows the full detailed specifications. The operational amplifier drives the small capacitive loads also.

Input Stage:

To keep the signal-to-noise ratio as large as possible particularly in non-inverting op amp circuits, the common mode input voltage should be kept as wide as possible. This can be accomplished by placing N-type and P-type input pairs in parallel.

By placing two complementary differential pairs in parallel, it is possible to obtain a rail-to-rail input stage. The NMOS pair is in conduction for high input common-mode voltages while the PMOS pair is in conduction for low input common mode voltages and the both differential pairs can operate together for middle values of the input common-mode voltage. In this case, the total trans-conductance of the input stage is not constant

It is also possible to obtain a constant trans-conductance; for low-input common-mode voltages only the PMOS pair is active, where for high ones only the NMOS pair is in conduction. For middle values, both pairs are “ON,” but each with reduced contribution (exactly the half in the “crossing point” condition). The constant-operation with low supply voltages is achieved by designing input transistors with large aspect ratios operating in weak inversion

Since the input transistors are in weak inversion, the input transconductance is the same for low and high-input common-mode voltages. For “middle” values of common-mode input voltages, a reduced value of current flows in both the input pairs which is exactly half of the value

compared to low and high common inputs. Consequently, the input transconductance is always the same.

The input stage mainly comprises of the CMOS complementary stage which consists of an N-differential pair and a P-differential pair to keep the signal-to-noise ratio as large as possible. The current bias transistors are used to keep the current flowing in the differential stage is constant. A much more serious drawback though is the variation of the input stage transconductance, g_m with the common-mode input voltage. So that one to three mirrors have been used with the transistors operating in strong inversion, reducing the variation to about 15%, using a 1.8-V minimum supply voltage.

6. SIMULATION RESULTS

Input Stage:

Name of the Transistor	W/L Ratio's ($\mu\text{m}/\mu\text{m}$)	M
M1, M2	72/1	1
M3, M4	181/1	1
M5	361/1	1
M6	145/1	1
M7, M8	542/1	1
M9, M10	217/1	1
M11, M12	551/1	1
M13, M14	734/1	1
M15, M16	289/1	1
M17, M18	361/1	1

Table 3: W/L ratio's of Input stage transistors

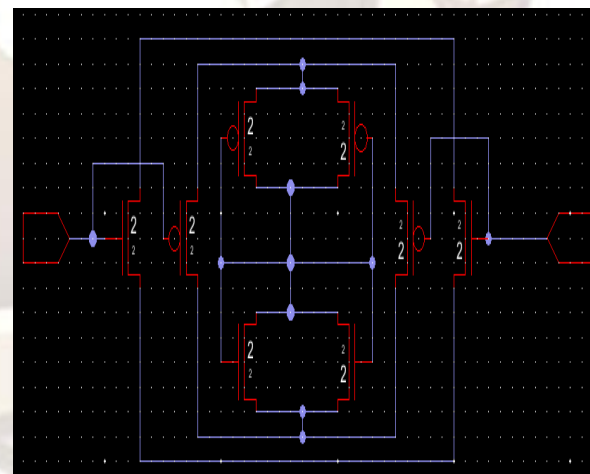


Fig 3: Differential Input Stage

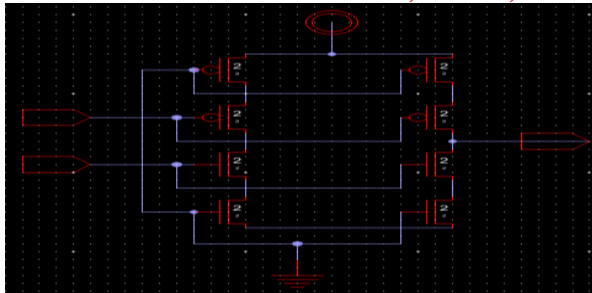


Fig 4: Transconductance Compensation Stage

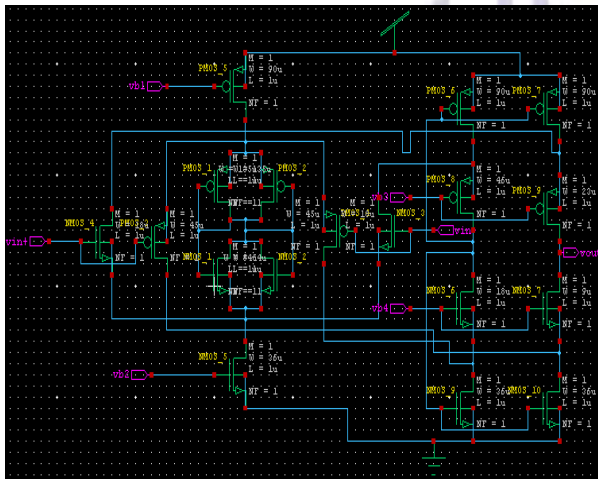


Fig 5: Input stage of the operational amplifier

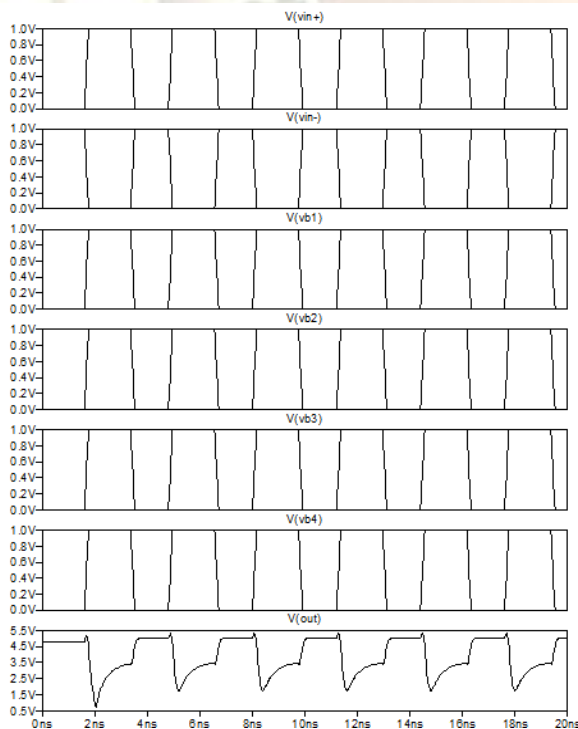


Fig 6: Final Output waveform of Compensated i/p stage

7. CONCLUSION

In this paper, the OP-AMP's input stage was compensated which results the output of the OP-AMP doesn't depends on the Transconductance. It is achieved by using the complementary differential pair transistors in the push pull configuration. Finally Differential input stage and compensation stage was combined to produce the OP-AMP which consumes less power, less settling time and more gain.

REFERENCES

- [1]. Philip E.Allen and Douglas R.Holberg, *CMOS Analog Circuit Design*, second edition, OXFORD UNIVERSITY PRESS, 2002.
- [2]. Paul R. Gray, Paul J.Hurst, Stephen H.Lewis, Robert G.Meyer, *Analysis and Design of Analog Integrated Circuits*, Fourth Edition, JOHN WILEY & SONS, INC, 2001.
- [3]. Johan H.Huijsing, *Operational Amplifiers theory and design*, KLUWER ACADEMIC PUBLISHERS.
- [4]. Willy M. C. Sansen, *Analog Design Essentials*, Published by SPRINGER.
- [5]. Christopher Saint, Judy Saint, *IC layout basics, A practical guide*, MCGraw-Hill.
- [6]. J. H. Botma, R. F. Wassenaar, R. J. Wiegierink, *A low-voltage CMOS Op Amp with a rail-to-rail constant-gm input stage and a class AB rail- to-rail output stage*, IEEE proc. ISCAS 1993, vol.2, pp. 1314-1317, May 1993.
- [7]. Ron Hogervorst, Remco J.Wiegierink, Peter A.L de jong, Jeroen Fonderie, Roelof F. Wassenaar, Johan H.Huijsing, *CMOS low voltage operational amplifiers with constant gm rail to rail input stage*, IEEE proc. pp. 2876-2879, ISCAS 1992.
- [8]. Giuseppe Ferri and Willy Sansen *A Rail-to-Rail Constant-gm Low-Voltage CMOS Operational Transconductance Amplifier*, IEEE journal of solid-state circuits, vol.32, pp 1563-1567, October 1997.
- [9]. Sander I. J. Gierkink, peter j. Holzmann, remco j. Wiegierink and Roelof f. Wassenaar, *Some Design Aspects of a Two-Stage Rail-to-Rail CMOS Op Amp*.
- [10]. Ron Hogervorst, John P. Tero, Ruud G. H. Eschauzier, and Johan H. Huijsing, *A Compact Power-Efficient 3 V CMOS Rail-to-Rail Input/Output Operational Amplifier for VLSI Cell Libraries*, IEEE journal of solid state circuits, vol.29, pp 1505-1513, December 1994.



Suparshya Babu Sukhavasi was born in India, A.P. He received the **B.Tech** degree from JNTU, A.P, and **M.Tech** degree from SRM University, Chennai, Tamil Nadu, and India in 2008 and 2010 respectively. He worked as **Assistant Professor** in Electronics & Communications Engineering in Bapatla Engineering College for academic year 2010-2011 and from 2011 to till date working in **K L University**. He is a member of Indian Society For Technical Education and International Association of Engineers. His research interests include Mixed and Analog VLSI Design, FPGA Implementation, Low Power Design and Wireless communications, VLSI in Robotics.



Susrutha Babu Sukhavasi was born in India, A.P. He received the **B.Tech** degree from JNTU, A.P, and **M.Tech** degree from SRM University, Chennai, Tamil Nadu, India in 2008 and 2010 respectively. He worked as **Assistant Professor** in Electronics & Communications Engineering in Bapatla Engineering College for academic year 2010-2011 and from 2011 to till date working in **K L University**. He is a member of Indian Society For Technical Education and International Association of Engineers. His research interests include Mixed and Analog VLSI Design, FPGA Implementation, Low Power Design and wireless Communications, Digital VLSI.



Dr. Habibulla Khan born in India, 1962. He obtained his B.E. from V R Siddhartha Engineering College, Vijayawada during 1980-84. M.E from C.I.T, Coimbatore during 1985-87 and PhD from Andhra University in the area of antennas in the year 2007. He is having more than 20 years of teaching experience and having more than 20 international, national journals/conference papers in his credit. Prof. Habibulla Khan presently working as **Head of the ECE department at K L University**. He is a fellow of I.E.T.E, Member IE and other bodies like ISTE. His research interested areas includes Antenna system designing, microwave engineering, Electro magnetics and RF system designing.



S R Sastry Kalavakolanu was born in A.P, India. He received the B.Tech degree in Electronics & communications Engineering from Jawaharlal Nehru Technological University in 2010. Presently he is pursuing M.Tech VLSI Design in KL University. His research interests include Low Power VLSI Design.



Vijaya Bhaskar Madivada was born in A.P, India. He received the B.Tech degree in Electronics & communications Engineering from Jawaharlal Nehru Technological University in 2010. Presently he is pursuing M.Tech VLSI Design in KL University. His research interests include FPGA Implementation, Low Power Analog Design.



Lakshmi narayana thalluri was born in A.P, India. He received the B.Tech degree in Electronics & communications Engineering from Jawaharlal Nehru Technological University in 2009. Presently, he is pursuing M.Tech VLSI Design in KL University.