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Simulation Study of Quasi Impedance Source Isolated DC/DC Converter Fed Drives

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ABSTRACT
This paper describes to step up the varying applied voltage, using a new step-up isolated DC/DC converter, which developed for distribution network with better efficiency and simulated through using MATLAB/SIMULINK VERSION 7.9. The main drawback of the conventional methods are drawn from the multistage energy conversion structure, i.e., complicated control and protection algorithms and reduced reliability due to the increased number of switching devices. To overcome this problem, a direct step-up dc/dc converter without input voltage pre-regulation is simpler in control and protection. Due to the reduced number of switching devices, the converter tends to have better efficiency and reliability. Thus, we develop new Quasi-Z-Source-Based Isolated DC/DC Converters for distribution network mainly focuses step-up dc/dc converter with high-frequency isolation for the distributed power generation systems. This is achieved by voltage-fed Q ZSI with continuous input current implemented at the converter input side and it can boost the input voltage by utilizing extra switching state the shoot-through state technique.

Keywords – **Impedance Source Inverter (ZSI), Zero Ripple Filter (ZRF), Voltage Source Converter (VSC).**

I. INTRODUCTION
Quasi Z source isolated Dc/Dc converters have been widely used in medium power applications for distribution system. Due to safety and dynamic performance requirements, the interface converter should be realized within the dc/dc/ac concept. This means that low voltage from the source first passes through the front-end step-up dc/dc converter with the galvanic isolation; subsequently, the output dc voltage

is inverted in the three-phase inverter and filtered to comply with the imposed standards and requirements (second dc/ac stage).

II. BLOCK DIAGRAM OF CONVENTIONAL METHOD
The conventional block diagram are as follows:
1.With Pre-regulator.

2. Without Pre-regulator.

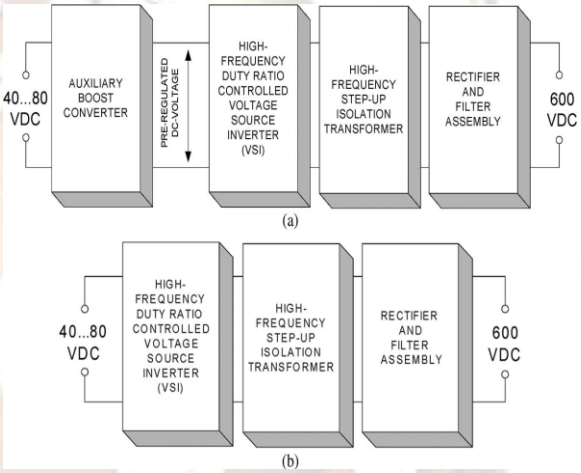

Fig. 2.1(a) With pre-regulator and 2.1(b) without pre-regulator

In the first case Fig. 2.1(a) the auxiliary boost converter steps up the varying souce voltage to a certain constant voltage level (80–100 Vdc) and supplies the input terminals of the isolated dc/dc converter. In that case, the primary inverter within the dc/dc converter operates with a near-constant duty cycle, thus ensuring better utilization of an isolation transformer. Moreover, due to pre-boosted input voltage, the isolation transformer has the moderate turns ratio which exerts a positive impact in terms of leakage inductance and efficiency[3]. A very interesting solution is proposed in where the conventional inductor in an auxiliary boost converter is replaced with a zero ripple filter (ZRF). The ZRF comprises a coupled inductor based filter for minimizing the high-frequency switching ripple and an active power filter for mitigating the low-frequency ripple. Despite evident advantages of the isolated dc/dc

converter with an auxiliary boost converter[2], its main drawbacks are drawn from the multistage energy conversion structure, complicated control and protection algorithms and reduced reliability due to the increased number of switching devices.

The choice of dc/dc converter topology in that case can be broadly categorized as a push–pull or a single-phase full-bridge topology. Because of the symmetrical transformer flux and minimized stress of primary inverter switches, the full-bridge circuit has been found to be most useful in terms of cost and efficiency compare to above model.

Voltage Source Inverter:

The valves are of the IGBT type. The VSC is connected to a symmetric three phase load, which has the impedance R+jωL and the emfs e1(t), e2(t) and e3(t). The neutral point of the star-connected load has the potential V0(t), due to a floating ground. The phase voltages of the VSC are denoted as u1(t), u2(t) and u3(t). The current flowing from the dc link to the converter is denoted.

III. CIRCUIT DIAGRAM OF PROPOSED MODEL:

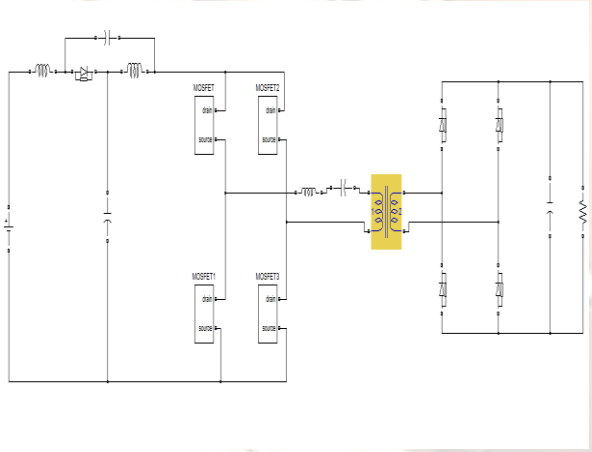

Fig 3.1Circuit diagram of proposed model

The Fig 3.1 shows the basic block diagram of proposed method. The various parts of block diagram are given below.

1. SINGLE PHASE QUASI IMPEDANCE SOURCE.
2. PWM INVERTER
3. ISOLATION TRANSFORMER
4. VOLTAGE DOUBLER RECTIFIER
5. LOAD

3.1 SINGLE PHASE QUASI IMPEDANCE SOURCE:

Figs 3.2 show the traditional voltage fed ZSI and the proposed voltage fed qZSI, respectively. In the same manner as the traditional ZSI, the qZSI has two types of operational states at the dc side: the nonshoot-through states (i.e. the six active states and two conventional zero states of the traditional VSI) and the shoot-through state (i.e. both switches in at least one phase conduct simultaneously). In the non-shoot-through states, the inverter bridge viewed from the dc side is equivalent to a current source.

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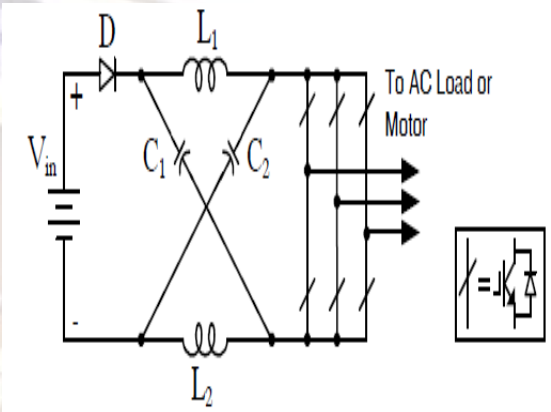


Fig.3.2Voltage fed Z-source inverter

The equivalent circuits of the two states are as shown in fig. The shoot-through state is forbidden in the traditional VSI, because it will cause a short circuit of the voltage source and damage the devices [5]. With the qZSI and ZSI, the unique LC and diode network connected to the inverter bridge modify the operation of the circuit, allowing the shoot-through state. This network will effectively protect the circuit from damage when the shoot-through occurs and by using the shoot-though state, the (quasi-) Z-source network boosts the dc-link voltage [4]. The ZSI has discontinuous input current in the boost mode; while the input current of the qZSI is continuous due to the input inductor *L*1, which will significantly reduce input stress;

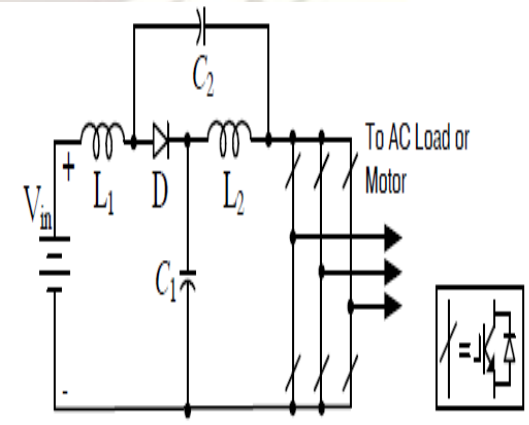


Fig.3.3 Voltage fed quasi-Z-source inverter

The major differences between the ZSI and qZSI are the qZSI draws a continuous constant dc current from the source [1]while the ZSI draws a discontinuous current and the voltage on capacitor C2 is greatly reduced. The continuous and constant dc current drawn from the source with this qZSI make this system.

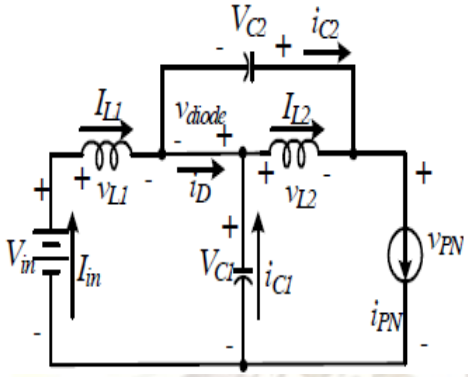


Fig 3.4 Equivalent circuit of the qZSI in non-shoot-through states

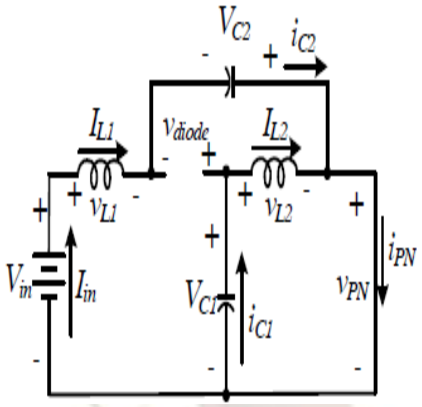


Fig 3.5 Equivalent circuit of the qZSI in shoot-through states

3.2.1 Circuit Analysis:

All the voltages as well as the currents are defined in Figs 3.4 , 3.5 and the polarities are shown with arrows[3]. Assuming that during one switching cycle, *T* , the interval of the shoot through state is *T*0 ; the interval of non-shoot-through states is *T*1 ; thus one has *T* = *T*0 + *T*1 and the shoot-through duty ratio, *D T*0 /*T* = . From Fig 2a which is a representation of the inverter during the interval of the non-shoot-through states, *T*1 , one can get

$$v_{L1} = V_{in} - V_{C1}, \qquad v_{L2} = -V_{C2}, \text{ and} \tag{1}$$

$$v_{PN} = V_{C1} - v_{L2} = V_{C1} + V_{C2} \quad v_{diode} = 0. \tag{2}$$

From Fig 3.4 which is a representation of the system during the interval of the shoot-through states, *T*0 , one can get

$$v_{L1} = V_{C2} + V_{in}, \qquad v_{L2} = V_{C1}, \text{ and} \tag{3}$$

$$v_{PN} = 0 \quad v_{diode} = V_{C1} + V_{C2}. \tag{4}$$

At steady state, the average voltage of the inductors over one switching cycle is zero. From (1), (3), one has

$$\begin{cases} V_{L1} = \bar{v}_{L1} = \dfrac{T_0(V_{C2} + V_{in}) + T_1(V_{in} - V_{C1})}{T} = 0 \\ V_{L2} = \bar{v}_{L2} = \dfrac{T_0(V_{C1}) + T_1(-V_{C2})}{T} = 0 \end{cases}$$

Thus

$$V_{C1} = \frac{T_1}{T_1 - T_0} V_{in} \qquad V_{C2} = \frac{T_0}{T_1 - T_0} V_{in} \tag{5}$$

From (2), (4) and (5), the peak dc-link voltage across the inverter bridge is

$$\hat{v}_{PN} = V_{C1} + V_{C2} = \frac{T}{T_1 - T_0} V_{in} = \frac{1}{1 - 2\dfrac{T_0}{T}} V_{in} = BV_{in} \tag{6}$$

where *B* is the boost factor of the qZSI. This is also the peak voltage across the diode.

The average current of the inductors *L*1 , *L*2 can be calculated by the system power rating *P*

$$I_{L1} = I_{L2} = I_{in} = P / V_{in} \tag{7}$$

According to Kirchhoff's current law and (7), we also can get that

$$I_{C1} = I_{C2} = I_{PN} - I_{L1} \qquad I_D = 2I_{L1} - I_{PN} \tag{8}$$

In summary, the voltage and current stress of the qZSI are shown in Table 1. The stress on the ZSI is shown as well for comparison, where

(1) *M* is the modulation index; ln ˆ *v* is the ac peak phase

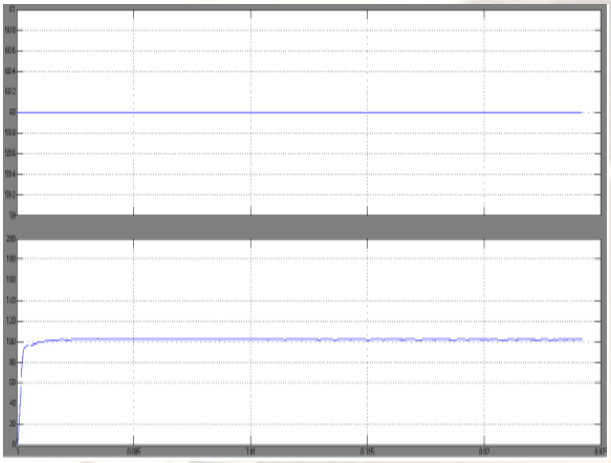
voltage; *P* is the system power rating;

(2) *m* = *T*1 /(*T*1 − *T*0) ; *n* = *T*0 /(*T*1 − *T*0) ; thus *m* >1;*m* − *n* =1;

(3) *B* = *T* /(*T*1 − *T*0) , thus *m* + *n* = *B* , 1< *m* < *B* .

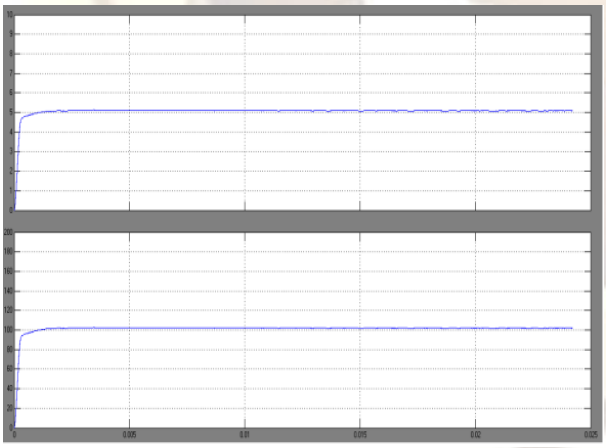
IV. RESULTS AND DISCUSSION

The Supply voltage of converter is 60V and achieved output voltage is 100V in boost mode. And in buck mode the same applied voltage and achieved output voltage is 35V. In normal mode the same supplied voltage is achieved. And the experimental parameters are source inductor=5e-6, capacitor=.54e-6, isolation transformer=1:1 turns ratio, series resonant of series inductor =74e-6, capacitor= 141e-09, 1 is for boost mode, 2 is for buck and normal mode. All the simulations are observed using resistor load and motor load.



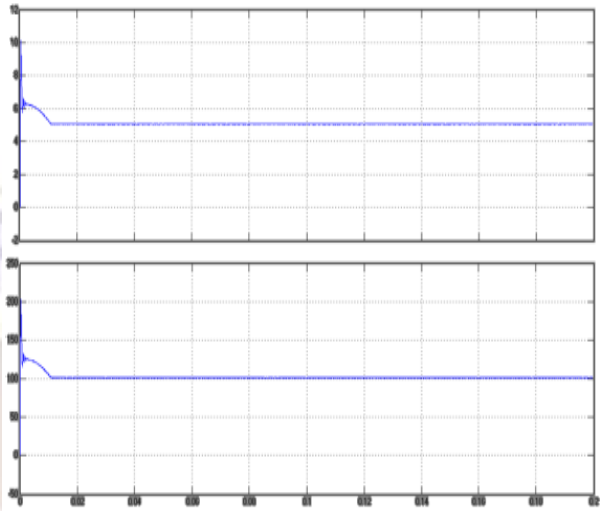
T in µsec

Fig.4.1 Input Voltage and Output Voltage waveform



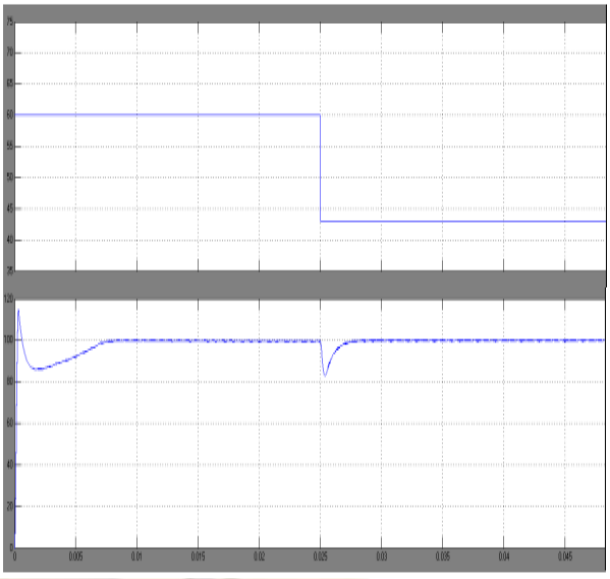
T in µsec

Fig4.2Output current and Output Voltage waveform



T in µsec

Fig.4.3 Output voltage and output current



T in µsec

Fig.4.4 Input Voltage and Output Voltage waveform

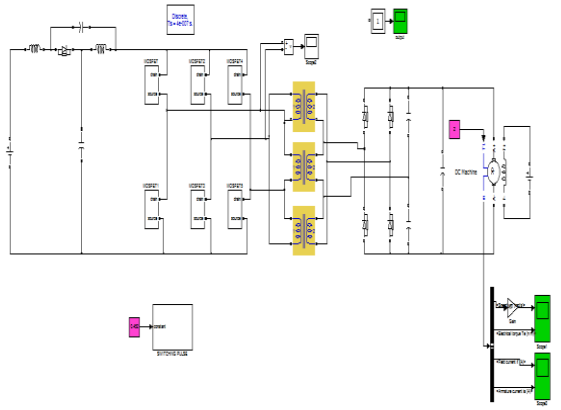
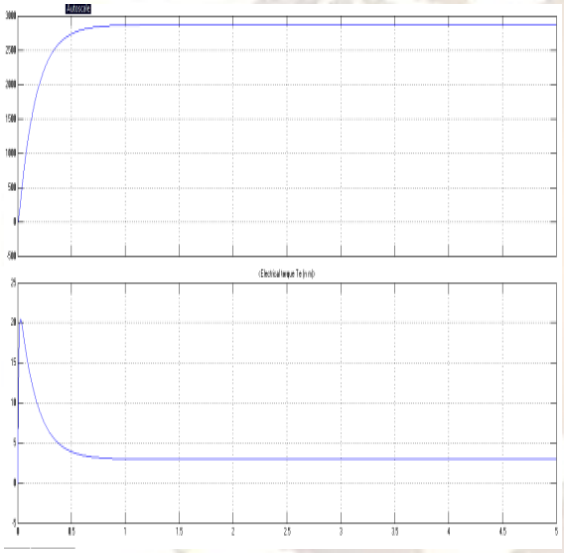


Fig4.5 Three phase qZ source open loop with motor



T in µsec

Fig.4.6 Speed and Torque waveform

V.CONCLUSION

Thus, the two new isolated step-up dc/dc converter topologies with qZSIs. The converters are intended for applications with widely varying input voltage and stabilized output voltage and when the galvanic separation of the input and output sides is required. This paper has focused on an example of the step-up dc/dc converter with high-frequency isolation for the distributed power generation systems. And also series resonant are employed in the primary side of isolation transformer for reducing the components size and soft switching results in zero current switching, zero voltage switching, lower EMI and higher efficiency over a wide operating range. Hence the conduction loss reduced and efficiency, reliability increased. Moreover, to improve the power density and reliability, the updated converter topology with the three-phase auxiliary ac link and the three-phase VDR was proposed and verified.

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