

Simulation Effects of Operating Temperature and Frequency at Performance of Different SRAM Cell Structures at Various Technologies

Sapna Singh, Neha Arora, Neha Gupta, Meenakshi suthar

Faculty of Engineering & Technology (MITS) Lakshmanagarh, India

ABSTRACT

To solve the power dissipation problem, many researchers have proposed different ideas from the device level to the architectural level and above. However, there is no universal way to avoid tradeoffs between power, delay and area, and thus designers are required to choose appropriate techniques that satisfy application and product needs. This paper represents the simulation of different SRAM cells and their comparative analysis on different parameters such as Power, Operating Frequency, Temperature and area efficiency etc. All the simulations have been carried out on EDA tanner at 90nm, 45nm and 32nm technologies for enhancing the cell performance.

Keywords - CMOS Logic, Low power, Speed, SRAM and VLSI.

I. INTRODUCTION

The transistors have been lowered which also contributes to leakage currents, badly. These leakage currents can drain a lot of power and reduce battery life dramatically, a severe curse for the portable multimedia applications. Solutions involving additional transistors, i.e., 7T, 8T, 10T and 11T have been explored to lower power consumption while reducing these adverse effects in the cell performance. This paper look into a couple of these SRAM Cells topologies that allow the analysis and simulations of different parameters at different technologies successfully on the basis of the power dissipation, speed, operating frequency range and their temperature dependence with the area efficiency of the circuit.

II. LITERATURE REVIEW OF DIFFERENT SRAM CELLS

1.1 6T SRAM Cell

In such a case, the SRAM voltage does not scale with technology and could even be increased as variability intensifies. The schematic diagram of 6T SRAM cell is shown in fig.1. (a)[1]. During read, the WL voltage VWL is raised, and the memory cell discharges either BL (bit line true) or BLB (bit line complement), depending on the stored data on nodes Q and BQ. A sense amplifier converts the differential signal to a logic-level output. Then, at the end of the read cycle, the BLs returns to the positive supply rail. During write, VWL is raised and the BLs are forced to either VDD (depending on the data), overpowering the

contents of the memory cell. During hold, VWL is held low and the BLs are left floating or driven to VDD.

1.2 Modified 6T SRAM Cell

The transistors NMOS₃, PMOS₄ and NMOS₂, PMOS₁ form cross coupled inverters. Reduction of leakage power is the effective stacking of transistors in the path from supply voltage to ground. This is based on the observation that “a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path.”[2][4].

1.3 7T SRAM Cell

The 7TSRAM cell uses a novel write mechanism in this fig.1(c) which depends only on one of the 2 bit-lines to perform a write operation, which reduces the activity factor of discharging the bit-line pair. [7].

1.4 8TSRAM Cell

A dual-port cell (8T-cell) is created by adding two transistors; the read can be entirely decoupled from the write operation in an 8T cell by sensing the data through a separate read stack controlled by a separate read wordline (RWL).The remaining 6T portion of the cell is optimized for write, resulting in an overall lower Vmin. Separation of data retention element and data output element means that there will be no correlation between the read SNM Cell and I Cell. Thus, an 8T SRAM design [10] contains a write assist in which a horizontally routed VDD line is collapsed during write. As a result, the bit cell array Vmin is limited by the hold margin.

1.5 9TSRAM Cell

The schematic of the 9T SRAM cell, with transistors sized for CMOS technology, is shown in Fig.1 (e). The upper sub-circuit of the 9T memory circuit is essentially a 6T SRAM cell with minimum sized devices (composed of NMOS₂,NMOS₁,NMOS₄,NMOS₃,PMOS₂, and PMOS₁).The two write access transistors (NMOS₃ and NMOS₄) are controlled by a write signal (WL). The data is stored within this upper memory sub-circuit. The lower sub circuit of the new cell is composed of the bit-line access transistors (NMOS₅ and NMOS₆) and the read access transistor (NMOS₇). The operations of NMOS₅ and NMOS₆ are controlled by the data stored in the cell. NMOS₇ is controlled by a separate read signal (RD) [12].

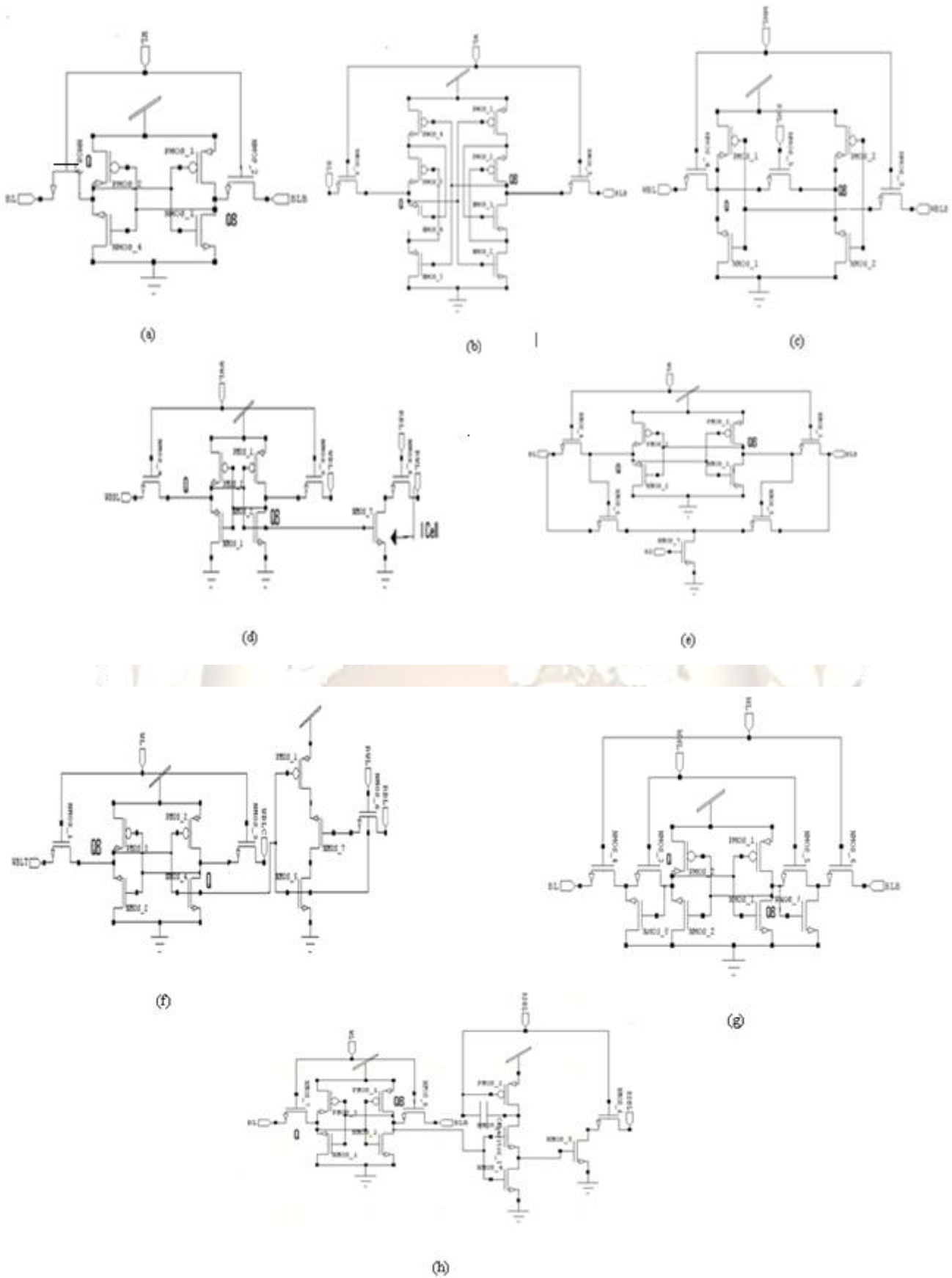


Fig.1:Several SRAM Cell structures :(a) 6T SRAM Cell [1] , (b) Modified 6T SRAM Cell [4] , (c) 7T SRAM Cell [7] ,(d) 8T SRAM Cell , (e) 9T SRAM Cell ,(f) 10T SRAM Cell [15] ,(g) Differential 10T SRAM Cell [15], (h) 11T SRAM Cell [16].

The 9T SRAM cell completely isolates the data from the bit lines during a read operation. The idle 9T SRAM cells are placed into a super cutoff sleep mode, thereby reducing the leakage power consumption.

1.6 10T SRAM Cell

Fig.1 (f) shows the schematic of the 10T sub threshold bit cell. Transistors are identical to a 6T bit cell except that the source of PMOS_3 and PMOS_2 tie to a virtual supply voltage rail Vdd. Write access to the bitcell occurs through the write access transistors, NMOS_1 and NMOS_3, Transistors from the write bitlines, WBLT and WBLC. Transistors NMOS_5 through NMOS_7 implement a buffer used for reading. Read access is single-ended and occurs on a separate bitline, RBL, which is precharged to prior to read access. The wordline for read also is distinct from the write wordline. One key Advantage to separating the read and write wordlines and bitlines is that a memory using this bitcell can have distinct read and write ports.

1.7 Differential 10T SRAM Cell

10T SRAM is as shown in Fig. (g) shows a schematic of a 10T SRAM with differential read bitlines (BL and BLB). Two NMOS transistors (NMOS_4 and NMOS_8) for the RBL and the other additional NMOS transistors (NMOS_6 and NMOS_7) for BLB are appended to the 6T SRAM. The 10T cell permits bit interleaving and exhibits superior sense margin with a differential read path based on a DCVSL (differential cascade voltage-switch-logic level) structure at the column periphery [15]. There is a performance degradation from stacked transistors that requires boosted WL voltages, but BL leakage is reduced at the same time.

1.8 11T SRAM Cell

In Fig.1 (h) the schematic of the 11T-SRAM bitcell is shown. Transistors PMOS_3, PMOS_1, NMOS_7, and NMOS_8 are identical to 6T SRAM, but two transistors NMOS_1 and NMOS_2 are downsized to the same size as the PMOS transistors. Minimum size transistors were used for the added 5T circuitry, except the access transistor that has a larger size. The most important part of the 11T-SRAM is a boost capacitor (CB) that connects source of NMOS_3 to RDWL. [16]

III. SIMULATION AND ANALYSIS

2.1 Simulation Environment

All the circuits have been simulated using BSIM 3V3 90nm, 45nm and 32nm technology on Tanner EDA tool. To make the impartial testing environment all the circuits have been simulated with supply voltage ranging 1v to 1.65v. Fig.2, 4, 5, 8, 9 shows the power consumption Vs. operating frequency and Fig.3, 6, 7, 10, 11 shows power consumption Vs. operating temperature for different SRAM cells circuits at 90nm, 45nm and 32nm technology.

2.2 Simulation analysis at 90 nm technology

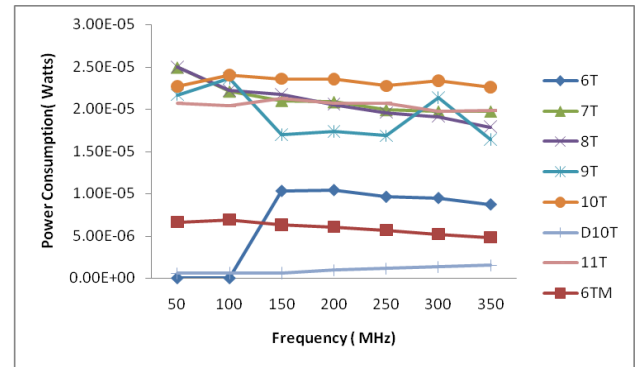


Fig.2 Power Consumption vs. Operating Frequency for different SARM Cells at 90nm technology.

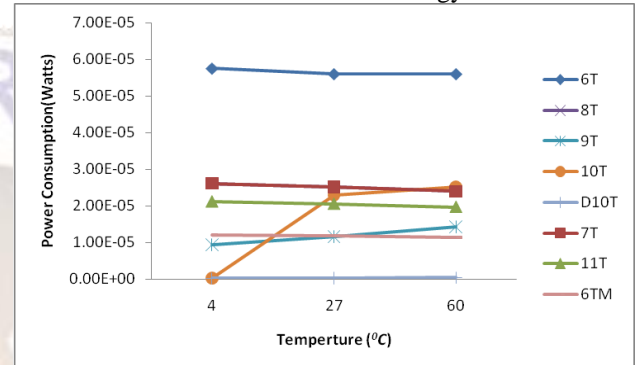


Fig.3 Power Consumption vs. Temperature for different SRAM Cell at 90nm technology

2.3 Simulation analysis at 45 nm technology

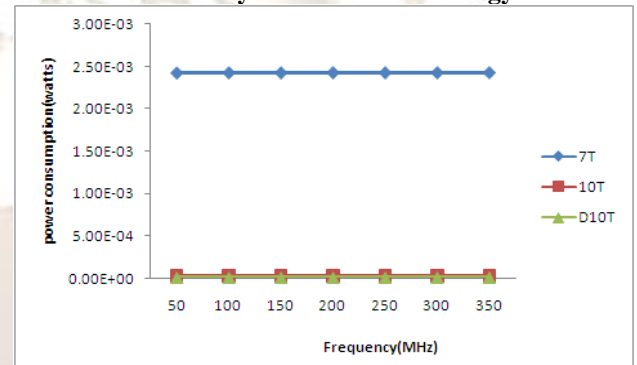


Fig.4 Power Consumption vs. Frequency for 7T, 10T and D10T SRAM Cells at 45nm technology.

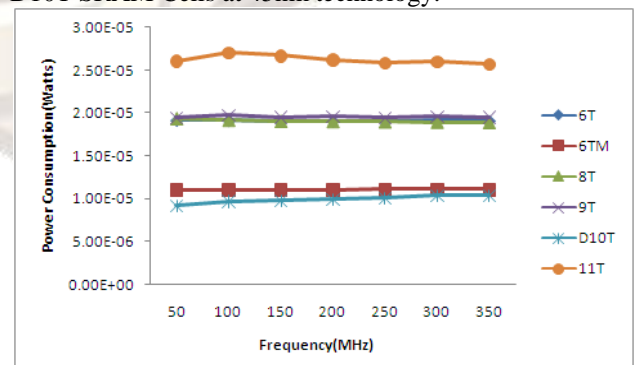


Fig.5 Power Consumption vs. Frequency for different SRAM Cells at 45nm technology.

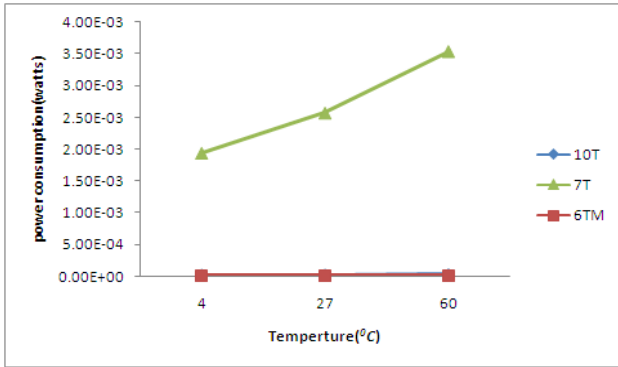


Fig.6 Power Consumption vs. Operating Temperature for 6TM, 7T and 10T SARM Cells at 45nm technology.

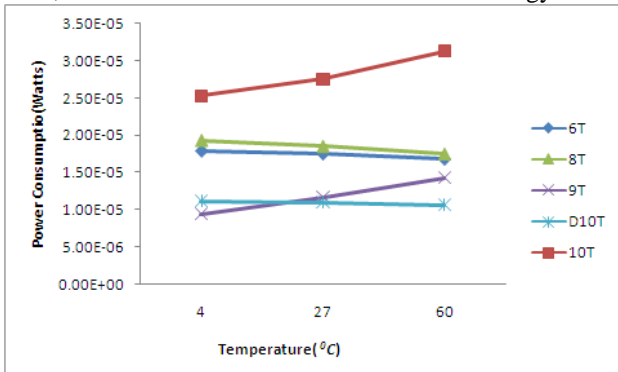


Fig.7 Power Consumption vs. Operating Temperature for different SARM Cells at 45nm technology.

2.4 Simulation analysis at 32 nm technology

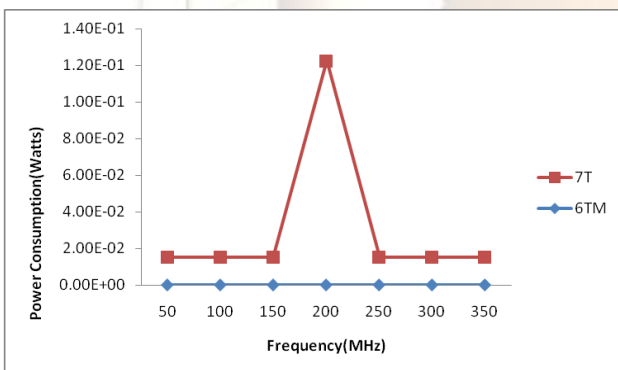


Fig.8 Power Consumption vs. Operating Frequency for 7T and 6TM SARM Cells at 32nm technology.

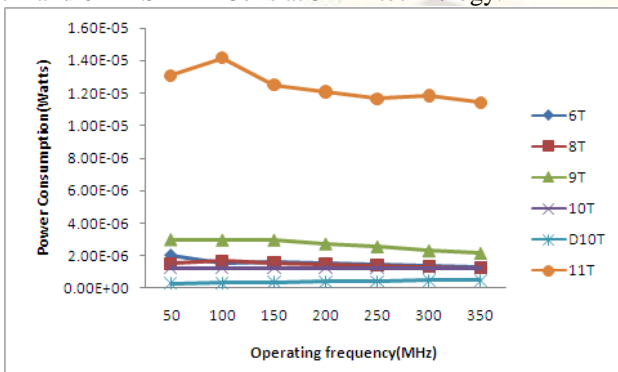


Fig.9 Power Consumption vs. Operating Frequency for different SARM Cells at 32nm technology.

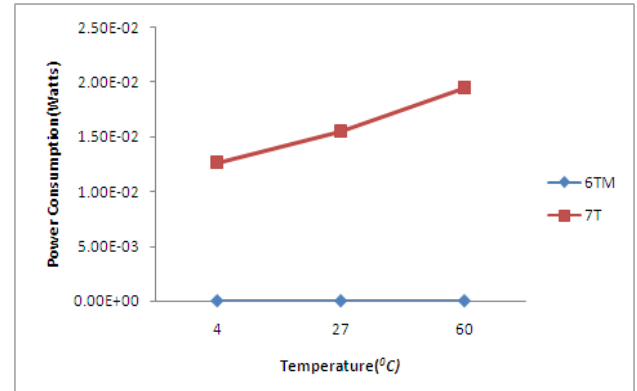


Fig.10 Power Consumption vs. Temperature for 6TM and 7T SRAM Cell at 32nm technology

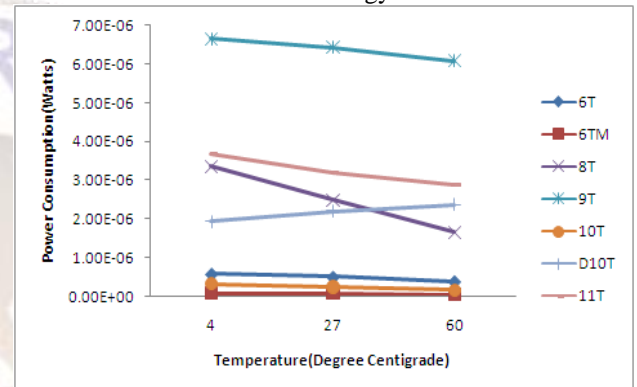


Fig.11 Power Consumption vs. Temperature for different SRAM Cell at 32nm technology

2.5 Simulation Results

By comparing different SRAM cell design, the power consumption of the Differential 10T SRAM cell shows the least power delay product over a range of supply voltages at 90nm and 45nm technology and Modified 6T SRAM cell shows the least power delay product over a range of supply voltages at 32nm technology in terms of power consumption, operating frequency and temperature.

IV. CONCLUSION

The most efficient technique to reduce the power dissipation is the reduction of the supply voltage. Unfortunately, reducing the supply voltage is the main factor of reduction the speed operation of the circuit. This paper tries to find out an efficient SRAM memory cell in both the aspects power consumption and speed in terms of operating frequency and temperature at different technologies for enhancing the cell performance.

V. REFERENCES

- [1] Jawar Singh, Dhiraj.K.Pradhan et al, "A single ended 6T SRAM cell design for ultra low voltage applications", IEICE Electronic Express, 2008, pp-750-755.
- [2] S.S.Rathod,S.Dasgupt,AshokSaxena "Investigation of Stack as a Low Power Design Technique for 6-T SRAM cell.Proc.IEEE TENCON,Nov.18-21,Univ.of Hyderabad, 2008,pp 1-5.

- [3] Kang, Sung-Mo, Leblebici and Yusuf (1999), "CMOS Digital Integrated Circuits Analysis and Design", McGraw-Hill International Editions, Boston, 2nd Edition
- [4] S. Narendra, S. Borkar, V.De, D.Antoniadis, and A.P.Chandrakasan, "Scaling of stack effect and its application for leakage reduction," Proc. IEEE ISLPLED, pp. 195-200, Aug. 2001.
- [5] C-T. Chu, X. Zhang, L. He and T. Jing, "Temperature aware microprocessor floorplanning considering application dependent power load", in *Proc. of ICCAD*, 2007, pp. 586-589.
- [6] Narendra Hanchate and Nagarajan Ranganathan, "LECTOR: A Technique for Leakage Reduction in CMOS Circuits," *IEEE Trans., on VLSI Systems*, vol. 12, No.2, Feb 2004
- [7] Aly, R.E. Bayoumi, M.A., "Low-Power Cache Design Using 7T SRAM Cell" *Circuits and Systems II: Express Briefs, IEEE Transactions*,vol. 54 April 2007, Issue: 4, pp. 318-322
- [8] W. Liao, L. He, and K. Lepak, "Temperature-Aware Performance and Power Modeling", *Technical report UCLA Engineering. 04-250*, 2004.
- [9] Chang, L. Montoye, R.K. Nakamura, Y.Batson, K.A.Eickemeyer, R.J.Dennard, R.H. Haensch, W.Jamsek, D, "An 8T-SRAM for Variability Tolerance and Low-Voltage Operation in High-Performance Caches", *Solid-State Circuits, IEEE Journal*vol. 43, April 2008, Issue 4, pp-956-963.
- [10] Benton H. Calhoun Anantha P. Chandrakasan "A 256-kb 65-nm Sub-threshold SRAM Design for Ultra-Low-Voltage Operation",*Solid- State Circuits, IEEE Journal* vol. 42, March 2007, Issue 3 , pp.680-688.
- [11] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low-power CMOS digital design," *IEEE J. Solid-State Circ.*, vol. 27, no. 4, pp. 473-484, Apr. 1992.
- [12] Rajshekhar Keerthi ,Henry Chen, "Stability and Static Noise margin analysis of low power SRAM"IEEE International Instrumentation & Measurement Technology Conference, Victoria Canada, May 2008,pp-1541-1544.
- [13] Sherif. A.Tawfik, Volkan Kursun, "Stability Enhancement Techniques for Nanoscale SRAM circuits, International SOC design Conference,2008,pp 113-116.
- [14] S. Dutta, S. Nag, K. Roy, "ASAP: A Transistor Sizing tool for speed, area, and power optimization of static CMOS circuits", *IEEE International Symposium on Circuits and Systems*, pp. 61-64, June, 1994.
- [15] Hiroki Noguchi et al., "Which is the best dual port SRAM in 45nm process technology? 8T, 10T single end and 10T differential" Renesas Technology corporation, 2008.
- [16] Farshad Moradi et al. "65nm Sub threshold 11 T SRAM for ultra low voltage Application, IEEE explore, 2008, pp-113-117.
- [17] Koichi Takeda et al, "A Read Static Noise Margin Free SRAM cell for Low Vdd and High Speed Applications", *Solid-State Circuits, IEEE Journal* vol. 41, Jan.2006, Issue 1, pp.113-121.
- [18] Zhiyu Liu, Volkan Kursun, " Characterization of a novel Nine Transistor SRAM cell, IEEE Transactions on Very Large Scale Integration Systems,vol.46, Issue 4, April 2008.pp-488-492.