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# For Power Quality Improvement Three-leg VSC Based DSTATCOM and A T-Connected Transformer

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**Abstract—**

In this paper for power quality improvement, a three leg vsc, and a new three phase four wire DSTATCOM based on a T-connected transformer is proposed. The three leg VSC compensates harmonic current, reactive current, and balances the load. The T-connected transformer connection mitigates the neutral current. Two single phase transformers are connected in T-configuration for interfacing to a three phase four wire power distribution system and the required rating of the VSC is reduced. The DC bus voltage of the VSC is regulated during load conditions. The insulated GATE BIPOLAR TRANSISTOR based VSC is supported by a capacitor is supported by a capacitor and is controlled for the required compensation of the load current. The DSTATCOM is validated using MATLAB software with its simulink and power system block set toolboxes

*Keywords components:- Distribution Static Compensator (DSTATCOM), neutral current compensation, power quality improvement-connected transformer, voltage source converter (VSC)*

## I. INTRODUCTION

Three Phase four wire distribution systems are facing severe power quality problems such as poor voltage regulation, high reactive power, harmonics current burden, load unbalancing, excessive neutral current. Most of the loads in these locations are non linear loads in the distribution system. The synchronous reference theory is used for the control of the proposed DSTATCOM. The DSTATCOM is validated using MATLAB software with its simulink and power system block set toolboxes for power factor correction, voltage regulation along with neutral current compensation, harmonic elimination, and load balancing with linear loads as well as non linear loads.

## II. SYSTEM CONFIGURATION AND DESIGN

Fig. 1(a) shows the single-line diagram of the shunt-connected DSTATCOM-based distribution system. The dc capacitor connected at the dc bus of the converter acts as an energy buffer and establishes a dc voltage for the normal operation of the DSTATCOM system. The DSTATCOM can be operated for reactive power compensation for power factor correction or voltage regulation.

Fig. 1(b) shows the phasor diagram for the unity power

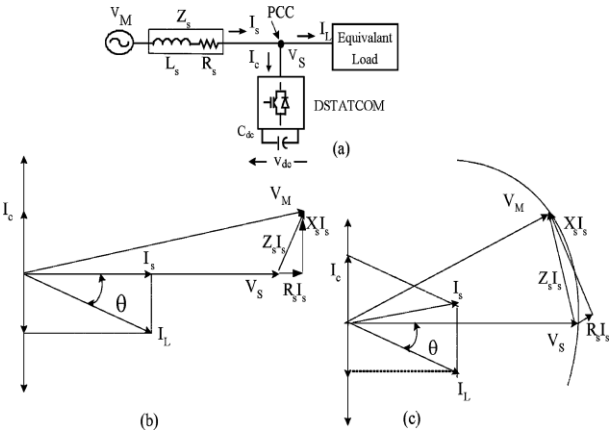


Fig. 1. (a) Single-line diagram of DSTATCOM system. (b) Phasor diagram for UPF operation. (c) ZVR operation.

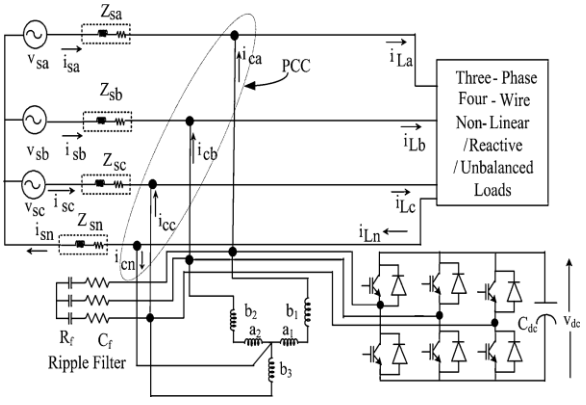

Fig. 2. Schematics of the proposed three-leg VSC with T-connected transformer-based DSTATCOM connected in distribution system factor operation.

The proposed DSTATCOM consisting of a three-leg VSC and a T-connected transformer is shown in Fig. 2, where the T connected transformer is responsible for neutral current compensation. The windings of the T-connected transformer are designed such that the mmf is balanced properly in the transformer. A three-leg VSC is used as an active shunt compensator along with a T-connected transformer, as shown in Fig. 2, and this topology has six IGBTs, three ac inductors, and one dc capacitor. The required compensation to be provided by the DSTATCOM decides the rating of the VSC components.

### A. DC Capacitor Voltage

The minimum dc bus voltage of VSC of DSTATCOM should be greater than twice the peak of the phase voltage of the system[17]. The dc bus voltage is calculated as

$$V\text{dc} = \frac{2\sqrt{2}VLL}{\sqrt{3}m} \quad (1)$$

where $m$ is the modulation index

### B. DC Bus Capacitor

The value of dc capacitor ($C$dc) of VSC of DSTATCOM depends on the instantaneous energy available to the DSTATCOM during transients .The principle of energy conservation is applied as

$$\frac{1}{2}C\text{dc}[\_V2\text{dc}\_ - \_V2\text{dc}1\_] = 3V(aI)\,t \quad (2)$$

where $V$dc is the reference dc voltage and $V$dc1 is the minimum voltage level of dc bus, $a$ is the overloading factor, $V$ is the phase voltage, $I$ is the phase current, and $t$ is the time by which the dc bus voltage is to be recovered.

### C. AC Inductor

The selection of the ac inductance ($Lf$ ) of VSC depends on,the current ripple $i$cr,p-p , switching frequency $fs$ , dc bus voltage ($V$dc), and $Lf$ is given as [17]

$$Lf = \frac{\sqrt{3}mV\text{dc}}{12afs\ i\text{cr(p-p)}} \quad (3)$$

where $m$ is the modulation index and $a$ is the overload factor..

### D. Ripple Filter

A low-pass first-order filter tuned at half the switching frequency is used to filter the high-frequency noise from the voltage at the PCC.

### E. Design of the T-connected Transformer

Fig. 3(a) shows the connection of two single-phase transformers in T-configuration for interfacing with a three-phase four-wire system. The T-connected windings of the transformer not only provide a path for the zero-sequence fundamental current and harmonic currents but also offer a path for the neutral current when connected in shunt at point of common coupling (PCC).

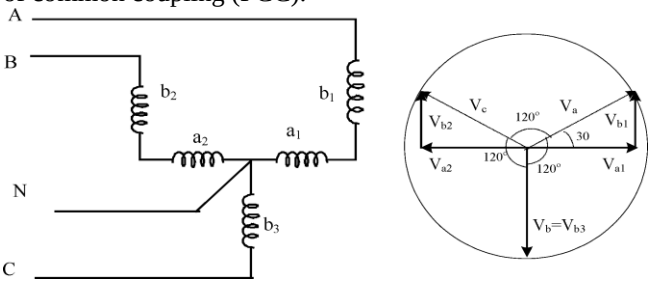


Fig. 3. (a) T-connected transformer and the three-leg VSC. (b) Phasor diagram.

The phasor diagram shown in Fig. 3(b) gives the following relations to find the turn's ratio of windings. If $Va1$ and $Vb1$ are the voltages across each winding and $Va$ is the resultant voltage, then

$$Va1 = K1Va \quad (4)$$

$$Vb1 = K2Va \quad (5)$$

where $K1$ and $K2$ are the fractions of winding in the phases.

## III. CONTROL OF DSTATCOM

A block diagram of the control scheme is shown in Fig. 4. The load currents ($iLa$, $iLb$, $iLc$), the PCC voltages ($vSa$, $vSb$, $vSc$), and dc bus voltage ($v$dc) of DSTATCOM are sensed as feedback signals.

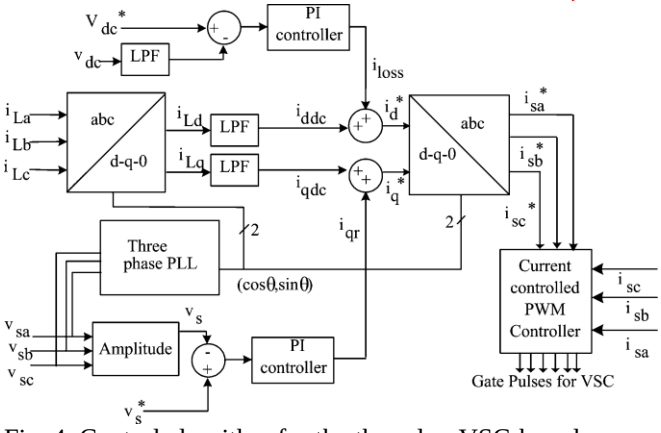


Fig. 4. Control algorithm for the three-leg-VSC-based DSTATCOMin a three phase four-wire system.

The *d*-axis and *q*-axis currents consist of fundamental and harmonic components as

$$iLd = id\,\mathrm{dc} + id\,\mathrm{ac} \quad (9)$$

$$iLq = iq\,\mathrm{dc} + iq\,\mathrm{ac}\,. \quad (10)$$

### A. UPF Operation of DSTATCOM

The output of the proportional-integral (PI) controller at the dc bus voltage of DSTATCOM is considered as the current ($i$loss ) for meeting its losses

$$i\mathrm{loss}(n) = i\mathrm{loss}(n-1) + Kpd(vde(n) - vde(n-1)) + Kidvde(n) \quad (11)$$

The reference source current is therefore

$$i*d = id\,\mathrm{dc} + i\mathrm{loss}\,. \quad (12)$$

The reference source current must be in phasewith the voltage at the PCC but with no zero-sequence component.

### B.Zero-Voltage Regulation (ZVR) Operation of DSTATCOM

The compensating strategy for ZVR operation considers that the source must deliver the same direct-axis component $i*d$, as mentioned in (12) along with the sum of quadrature-axis current ($iq$ dc) and the component obtained from the PI controller ($iqr$ ) used for regulating the voltage at PCC. The amplitude of ac voltage ($VS$ ) at PCC is calculated from the ac voltages ($vsa$, $vsb$, $vsc$) as

$$VS = (2/3)1/2\ (v2sa + v2sb + v2sc\ )1/2\,. \quad (14)$$

Then, a PI controller is used to regulate this voltage to a reference value as

$$iqr(n) = iqr(n-1) + Kpq\ (vte(n) - vte(n-1)) + Kiq\ vte(n) \quad (15)$$

where $vte(n) = V * S - VS(n)$ denotes the error between reference($V * S$ ) and actual ($VS(n)$ ) terminal voltage amplitudes at the $n$th sampling instant. $Kpq$ and $Kiq$ are the proportional and integral gains of the dc bus voltage PI controller. The reference source quadrature-axis current is

$$i*q = iq\,\mathrm{dc} + iqr\,. \quad (16)$$

The reference source current is obtained by reverse Park's transformation using (13) with $i*d$ as in (12) and $i*q$ as in (16) and $i*0$ as zero.

### C. Computation of Controller Gains

The gains of the controllers are obtained using the Ziegler–Nichols step response technique. A step input of amplitude ($U$) is applied and the output response of the dc bus voltage is obtained for the open-loop system. The maximum gradient ($G$) and the point at which the line of maximum gradient crosses the time axis ($T$) are computed.

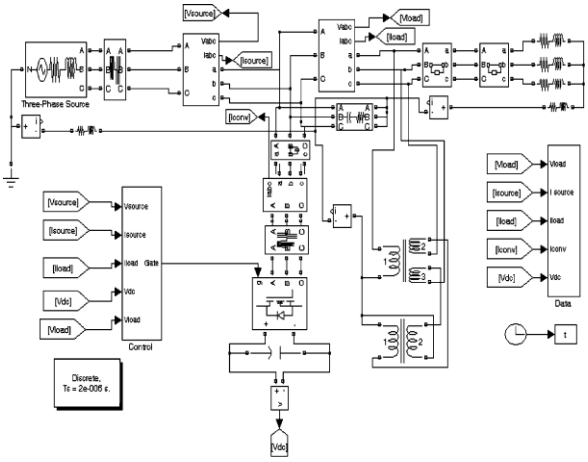


Fig. 5. MATLAB model of the T-connected transformer and the three-leg-VSC-based DSTATCOM-connected system.

The gains of the controller are computed using the following equations:

$$Kp = \frac{1.2U}{GT} \quad (17)$$

$$Ki = \frac{0.6U}{GT2} \quad (18)$$

The gain values for both the PI controllers are computed and are given in the Appendix.

### D. Current-Controlled Pulse widthModulation (PWM) Generator

In a current controller, the sensed and reference source currents are compared and a proportional controller is used for amplifying current error in each phase before comparing with a triangular carrier signal to generate the gating signals for six IGBT switches of VSC of DSTATCOM.

## IV. MODELING AND SIMULATION

The three-leg VSC and the T-connected-transformer-based

DSTATCOM connected to a three-phase four-wire system is modeled and simulated using the MATLAB with its Simulink.

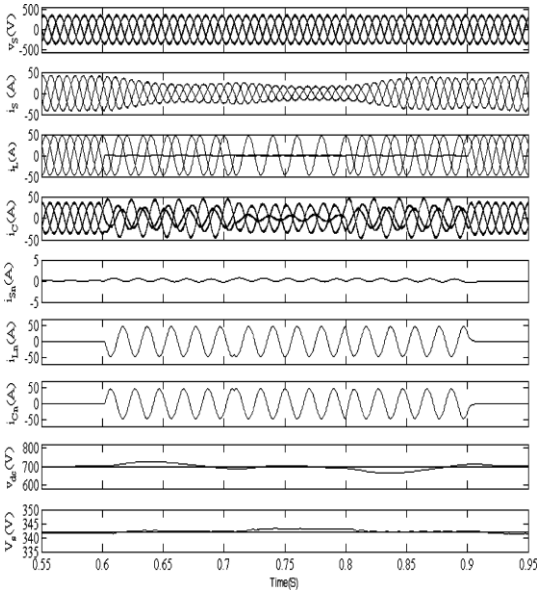


Fig. 6. Performance of a three-phase three-leg VSC and T-connected transformer-based DSTATCOM for neutral current compensation, load balancing, and voltage regulation

## 1. RESULTS AND DISCUSSION

The performance of the T-connected transformer and threeleg-VSC-based three-phase four-wire DSTATCOM is demonstrated for power factor correction and voltage regulation along with harmonic reduction, load balancing, and neutral current compensation. The developed model is analyzed under varying loads and the results are discussed shortly.

### *A. Performance of DSTATCOM With Linear Load for Neutral Current Compensation, Load Balancing, and ZVR Operation*

The dynamic performance of the DSTATCOM under linear lagging power factor unbalanced load condition is shown in Fig. 6. At 0.6 s, the load is changed to two-phase load and to single-phase load at 0.7 s.

### *B. Performance of DSTATCOM With Nonlinear Load forHarmonic Compensation, Load Balancing, and ZVR Operation*

The dynamic performance of the DSTATCOM with nonlinear and unbalanced load is given in Fig. 7.At 0.8 s, the load is changed to two-phase load and to single-phase load at 0.9 s. The loads are applied again at 1.0 and 1.1 s, respectively

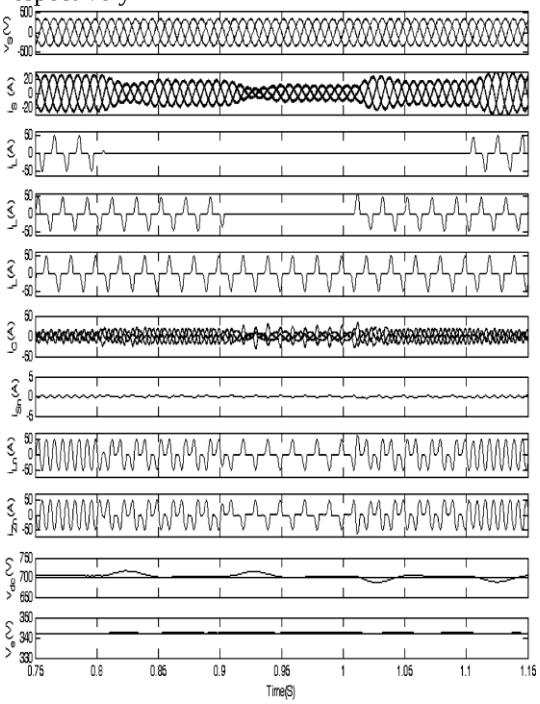


Fig. 7. Performance of a three-phase three-leg VSC and T-connected transformer-based DSTATCOM for neutral current compensation, load balancing, harmonic compensation, and voltage regulation.

### *C. Performance of DSTATCOM With Linear Load for Neutral Current Compensation, Load Balancing, and UPF Operation*

The dynamic performance of the DSTATCOM during linear power-factor-unbalanced load condition is depicted in Fig. 8. At 0.6 s, the load is changed to two-phase load and to single-phase load at 0.7 s. The loads are applied again at 0.8 and 0.9 s, respectively. The PCC voltages (*vS* ), source currents (*iS* ), load currents (*iL* ), compensator currents (*iC* ), source-neutral current (*iSn*), load-neutral current (*iLn*), compensator-neutral current (*iCn*), dc bus voltage (*v*dc), and amplitude of voltage (*VS* ) at PCC are also depicted in Fig. 8. The reactive power is compensated for power factor correction, and the source currents are balanced and sinusoidal.

### *D. Performance of DSTATCOM With Nonlinear Load for Harmonic Compensation, Load Balancing, and UPF Operation*

The dynamic performance of the DSTATCOM during nonlinear unbalanced load condition is shown in Fig. 9.

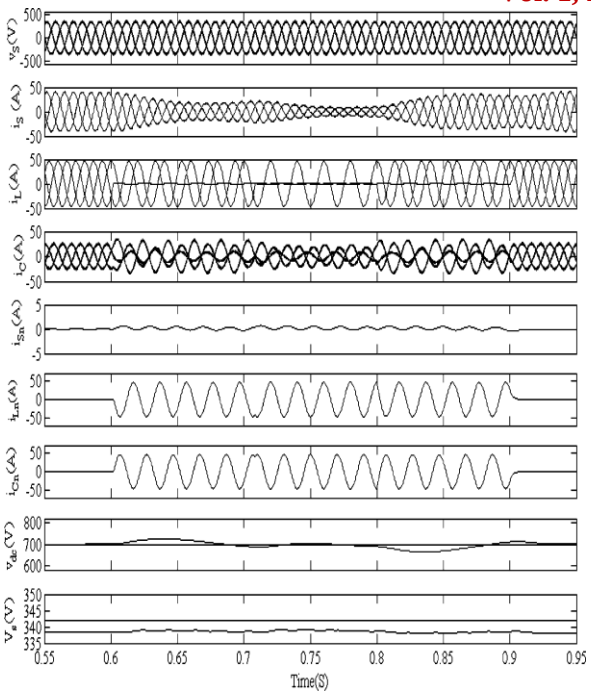


Fig. 8. Performance of a three-phase three-leg VSC and T-connected transformer-based DSTATCOM for neutral current compensation, load balancing, and power factor correction.

The PCC voltages (*vS* ), source currents (*iS* ), load currents (*iLa*, *iLb*, *iLc*), compensator currents (*iC* ), source-neutral current (*iSn*), compensator-neutral current (*iCn*), load-neutral current (*iLn*), dc bus voltage (*v*dc), and amplitude of voltage (*VS* ) at PCC are also depicted in Fig. 9.

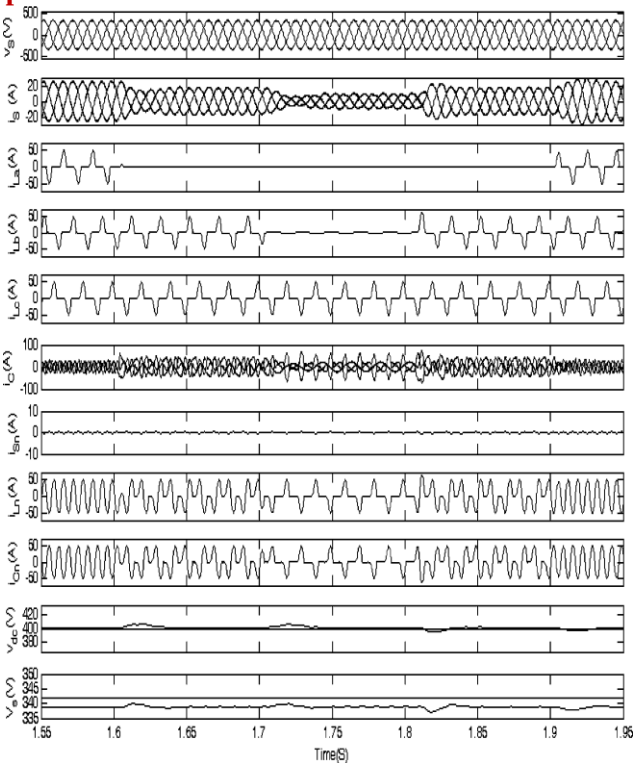


Fig. 9. Performance of a three-phase three-leg VSC and T-connected transformer-based DSTATCOM for neutral current compensation, load balancing, harmonic compensation, and power factor correction.

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